ISSCC 2025 Call for Papers

IEEE International Solid-State Circuits Conference

Sunday-Thursday, February 16-20, 2025

San Francisco Marriott Marquis, San Francisco, CA

ISSCC website: http://isscc.org

IEEE International Solid-State Circuits Conference • Sunday-Thursday, February 16-20, 2025 • San Francisco Marriott Marquis Hotel, San Francisco, CA

ISSCC 2025 CONFERENCE THEME:
The Silicon Engine Driving the AI Revolution

ISSCC is in its 72nd year as a flagship conference for solid-state circuit design. ISSCC promotes and shares new circuit ideas with the potential to advance the state-of-the-art in IC design and provide new system capabilities. This year's conference theme highlights how today's circuit research and development can contribute to the solid-state foundation upon which Artificial Intelligence (AI) is rapidly evolving and pervasively entering people's lives.

Innovative and original papers are solicited in subject areas including (but not limited to) the following:

ANALOG: Circuits with analog-dominated innovation; amplifiers, comparators, oscillators, filters, references; nonlinear analog circuits; digitally assisted analog circuits; sensor interface circuits; MEMS sensor/actuator interfaces, analog circuits in sub-10nm scaled technologies.

DATA CONVERTERS: Nyquist-rate and oversampling A/D and D/A converters; embedded and application-specific A/D and D/A converters; time-to-digital converters; innovative and emerging converter architectures.

DIGITAL CIRCUITS, ARCHITECTURES & SYSTEMS*: Digital circuits, architectures, building blocks, and complete systems (monolithic, chiplets, 2.5D, and 3D) for microprocessors, micro-controllers, application processors, graphics processors, automotive processors, processors for machine learning (ML) and artificial intelligence (AI), and system-on-chip (SoC) processors. Digital systems and accelerators for communications, video and multimedia, annealing, optimization problem solving, reconfigurable systems, near- and sub-threshold systems, and emerging applications. Digital circuits for intra-chip communication, clock distribution, soft-error and variation-tolerant design, power management (e.g., voltage regulators, adaptive digital circuits, digital sensors), and digital clocking circuits (e.g., PLLs, DLLs) for processors. Digital ML/AI systems and circuits, including near-memory and in-memory computation and hardware optimizations for new ML models such as transformers, graph and spiking neural networks, and hyper-dimensional computing.

IMAGERS, MEDICAL, & DISPLAY: Image sensors; vision sensors and event-based vision sensors; automotive, LIDAR; ultrasound and medical imaging; wearable, implantable, ingestible devices; biomedical sensors and SoCs, neural interfaces and closed-loop systems; medical devices; microarrays; body area networks and body coupled communication; machine learning and edge computing for medical and imaging applications; display drivers, touch sensing; haptic displays; interactive display and sensing technologies for AR/VR.

MEMORY: Static, dynamic, and non-volatile memories for stand-alone and embedded applications; memory/SSD controllers; high-bandwidth I/O interfaces for memories; memories based on phase-change, magnetic, spin-transfer-torque, ferroelectric, and resistive materials; array architectures and circuits to improve low-voltage operation, power reduction, reliability, performance improvement and fault tolerance; application-specific circuit enhancements within the memory subsystem, in-memory-computing or near-memory-computing macros for AI or other applications.

POWER MANAGEMENT: Power management, power delivery, and control circuits; switched-mode power converter ICs using inductive, capacitive, and hybrid techniques; LDO/linear regulators; gate drivers; wide-bandgap (GaN/SiC); isolated and wireless power converters; envelope supply modulators; energy harvesting circuits and systems; robust power management circuits for automotive and other harsh environments; LED drivers.

RF CIRCUITS and WIRELESS SYSTEMS:** Complete solutions and building blocks at RF, mm-Wave and THz frequencies for receivers, transmitters, frequency synthesizers, RF filters, transceivers, SoCs, and wireless SiPs incorporating multiple chiplets. Innovative circuits, systems, design techniques, heterogeneous packaging solutions, etc. for established wireless standards as well as future systems or novel applications, such as sensing, radar, and imaging, and those improving spectral and energy efficiency.

SECURITY: Chips demonstrating cryptographic accelerators (e.g., encryption, light-weight crypto, post-quantum crypto, privacy-preserving compute, blockchain), smart card security, trusted/confidential computing, security circuits (e.g., PUFs, TRNGs, side-channel and fault attack countermeasures, circuits and sensors for attack detection and prevention), security for resource-constrained systems, secure micro-processors, secure memories, analog/mixed-signal circuit security (e.g., secure ADC/DAC, RF, sensors), secure supply chains (e.g., hardware trojan countermeasures, trusted microelectronics), security for/with emerging technologies, and core circuit-level techniques for logical/physical-level security.

TECHNOLOGY DIRECTIONS: Emerging and novel IC, system, and device solutions in various areas such as integrated photonics, silicon electronics-photonics integration; quantum devices for metrology, sensing, computing, etc.; flexible, stretchable, foldable, printable, and 3D electronic systems; biomedical sensors for cellular and molecular targets; wireless power transfer at-distance (e.g., RF and mm-wave, optical, ultrasonic); ICs for space applications and other harsh environments; novel platforms for non-CMOS computing and machine learning; integrated meta-materials, circuits in alternative device platforms (e.g., carbon, organic, superconductor, spin, etc.).

WIRELINE: Receivers/transmitters/transceivers for wireline systems, including backplane transceivers, copper-cable links, chip-to-chip communications, 2.5/3D interconnect, on-chip/on-package links, high-speed interfaces for memory; optical links, and silicon photonics; exploratory I/O circuits for advancing data rates, bandwidth density, power efficiency, equalization, robustness, adaptation capability, and design methodology; building blocks for wireline transceivers (including but not limited to AGCs, analog frontends, ADC/DAC/DSPs, TIAs, equalizers, clock generation and distribution circuits including PLLs/DLLs, clock recovery, line drivers, and hybrids).

*This category will be reviewed by either the Digital Circuits or Digital Architectures & Systems Subcommittee.

**This category will be reviewed by either the RF or Wireless Subcommittee.

Deadline for Electronic Submission of Papers:
Wednesday, September 4, 2024 • 3:00 PM Eastern Daylight Time (19:00 GMT)

Please Review Important New Changes in Submission Details Below.

IEEE

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STUDENT ACTIVITIES

Student-Research Preview (SRP): This session provides students with the opportunity to showcase their work and interact with students and researchers from academia and industry. SRP is organized as an Evening Session consisting of short presentations followed by a poster session. **The abstract submission deadline for SRP is October 19, 2024**. Refer to the ISSCC Website for more information.

Student Travel Grant Awards: Students who are members of the Solid-State Circuits Society and in a Ph.D. program can apply for partial travel support to attend ISSCC. Visit the SSCS website https://sscs.ieee.org/membership/awards/student-travel-grants for more information.

Silkroad Award: The winner(s) are selected from first-time student-presenting authors at ISSCC whose research is conducted in an emerging region in the Far East.

DEMONSTRATION SESSIONS:

Selected authors of accepted, regular papers will be invited to demonstrate their working circuit or system in the ISSCC Demonstration Sessions. The demonstrations will be held during the Conference social hours on Monday and Tuesday. The selected authors will also provide a poster to augment their demonstration.

EXHIBIT PROGRAM

Semiconductor design and technology is evolving rapidly – to succeed in the future, you must understand your customers and have a clear vision of what's ahead. As the flagship conference of the IEEE Solid-State Circuits Society, ISSCC will feature over 2500 participants including top designers and technologists from leading corporate and academic institutions around the world. ISSCC's expanding exhibit program offers access and networking opportunities with decision-makers and technical influencers at all levels of the semiconductor design ecosystem. Connect with the unique and visionary conference attendees at ISSCC to share and discuss the latest advances in your technology, design automation and products. Contact the ISSCC Exhibit Team at isscc.exhibits@gmail.com to reserve your space for 2025.

INNOVATIVE SUBMISSIONS

More than ever, ISSCC attendees want to see innovative contributions (e.g., novel circuit and system architectures) in both established and emerging fields of IC and SoC designs. Although some innovative works may not have a best-in-class metric, these contributions explore new circuit and system architectures that may approach problems from a unique perspective, challenge fundamental tradeoffs, or even open up new directions for future research and products. The ISSCC committee of expert technical reviewers are seeking excellent examples of innovation in IC and SoC designs to form the ISSCC technical program.

ELECTRONIC SUBMISSION OF ABSTRACT, DRAFT MANUSCRIPT, AND PRE-PUBLICATION MATERIAL:

Authors should submit 2 items for review: 1) An informative and quantitative **Abstract; 2)** A **Draft Manuscript** including figures for the Digest of Technical Papers. Be sure to read the Pre-Publication Guidelines (summarized below) carefully.

The Submissions Website will be available starting July 1, 2024. You may consult the Website for instructions at any time after this date. To submit a paper, go to https://submissions.mirasmart.com/ISSCC2025 to upload the manuscript and provide the requested additional information. **The abstract and manuscript must be submitted by September 4, 2024 at 3pm EDT.** During the submission process you will be asked for a suggested subcommittee (by subject area) to review your submission, however this subcommittee may be changed by the ISSCC organization to ensure the best review quality. A sample abstract and draft Digest paper can be found at the ISSCC submissions Website (single-column double-spaced format is required for the paper-review process).

ADDITIONAL SUBMISSION DETAILS (new changes):

The submission **Title** must be concise (target ≤12-14 words) and clearly describe the topic of the paper. It should not include more than one or two key metrics or techniques from the described work. If multiple key metrics are included in the title, they should be mutually consistent (e.g. the title should not claim performance for one test configuration and power for another test configuration).

The **Abstract** must be uploaded to the **Submissions Website**. It must not exceed 500 characters (including spaces). The Abstract must be factual and provide as complete and quantitative a description as possible, including specific and concrete performance data. Claims such as "new", "advanced", "novel", "high-performance", and "high-speed" are not acceptable in the title or abstract. Please refer to the sample abstract on the ISSCC Website. **Note that ISSCC reserves the right to modify the paper title and abstract when technically appropriate.**

The **Manuscript** consists of **two** PDFs uploaded to the Submissions Website. The first, for the draft manuscript text, is limited to 4 pages in single-column double-spaced format, using 12pt Arial Narrow font with fewer than 10,000 characters (including spaces). The second, for the figures, must be no more than two pages, using the template found on the ISSCC submissions website. The template mimics the digest publication and has six slots for figures per page. Your submitted figure template should be readable if printed out on standard-size paper, because the figure clarity directly impacts the paper review.

The first seven figures, including a die photo, must be referred to in the text. In addition, up to three optional supplementary figures can be included for review purposes. Tables should be included in the figures, not in the text.

If a die-photo and/or comparison table is available, they can be included as part of the 7-figure limit. Supplementary figures will **NOT** be part of the final manuscript and should **NOT** be referred to in the text of the paper but serve **ONLY** as additional material for the reviewers. These 3 figures should labeled as "Fig. S1, S2, S3".

References are to be entered individually into the submission website. Up to 30 references are allowed. Should your paper be accepted, references in the final manuscript will be placed on the 3rd page. Make sure that ALL related work is sufficiently referenced, including your own. In addition, the website will allow you to provide a hyperlink to the reference, per the guidelines provided on the submission website to ensure it is properly blinded. **Do not include your references in your manuscript.** For further details, see the ISSCC submission site. Papers exceeding the length limit will be immediately rejected.

Double-Blind Review. The paper selection will follow a double-blind review process, meaning that both the authors and reviewers will remain anonymous during the paper selection process. All authors **MUST** adhere to the following guidelines to conceal their identity: (1) Eliminate author names, contact information, and affiliations from the entire manuscript (including **PDF metadata, logos on die photos, logos on printed circuit board photos,** etc.). Author names can appear in the cited references (see item 2). The submission site allows authors to modify the title ("Paper Title (blinded)") if the intended title would reveal the authors or their affiliation. (2) Cite all relevant prior work (including your own) in the third person (for example, "It has been shown that… [1]"; do not use the words "my" or "our"). Work that is substantially related to the submission and has been submitted to another Conference/Journal, but has not been published yet, **must be cited in an anonymized format*** and **must be uploaded as supplementary material**. This supplementary material does not need to be anonymous, as it will be checked only after paper selection. Do not cite patents. (3) Eliminate acknowledgements and references to funding sources. These can be added later if the paper is accepted. (4) Do not contact the program committee members outside of your own organization to solicit input on your manuscript. The identity of authors is only known to the program chair/vice-chair and the subcommittee chairs. You may contact them for questions. Manuscripts that are not properly anonymized cannot be considered for review. To ensure your submission complies with these rules please carefully review the sample manuscript, the FAQ on Double-Blind Review, and the guidelines on how to write a good submission at the ISSCC Website. The review process will include a software-based plagiarism check. After paper selection, a final pre-publication check (using the authors' names and any supplemental material provided) is applied using the guidelines summarized below. ISSCC may withdraw any paper that violates the pre-publication guidelines.

*Citation for related work by the authors that is submitted to another conference/journal but not yet published: [1] Details withheld in accordance with double-blind review process (paper attached as supplementary document).

Review Process and Criteria: Submitted manuscripts are reviewed by an ISSCC subcommittee that covers the topic of the manuscript. The author's suggested subcommittees are strongly considered when assigning each manuscript to a subcommittee. Submissions are rated by the subcommittee members based on (i) design novelty, (ii) significance in its field, and (iii) technical quality. Authors should provide clear evidence of what is novel in their work and/or the extent to which it advances the state-of-the-art. Many submissions will be stronger in novelty or significance, so both are equally weighted by the subcommittee. A high level of technical quality and clarity is a requirement for all submissions. Successful submissions contain specific new results, sufficient technical detail and data to be understood, circuit schematics, measured results to support claims, and tabulated comparisons with recently published work, where appropriate.

For further details on manuscript preparation, check the ISSCC Website or send an email with your questions to the Director of Publications: Laura Fujino, Email: lcfujino@aol.com. All information regarding submission is also available at the Submissions Website.

Notification of Acceptance: Authors will be notified of acceptance by October 14, 2024. A submission may be accepted as either a regular or short paper. A regular paper is allowed 30 minutes (23 minutes presentation time). A short paper is allowed 15 minutes (12 minutes presentation time). Regular and short papers must meet the same submission and quality standards. They differ only in the determination by the Program Committee of the time required to present their key ideas.

Authors of accepted papers will have an opportunity to modify their manuscript, except the reported key performance indicators. All information removed/anonymized following the Double-Blind Review guidelines (logo on-die photo, etc.) may be added back to the final paper upon acceptance. The Program Committee may require specific additional revisions. There will be further formatting requirements for the final Digest manuscript. The presenting author is required to register for the Conference in advance.

Conference Pre-Publication Policy: As the premier global forum for the debut of technical innovations in integrated circuits and systems, ISSCC cannot accept papers whose key innovative ideas and results have already been disclosed to the public. To assess the novelty of a paper, the program committee evaluates its content against all background or baseline information that was pre-published by the authors. Disclosures considered as pre-publication include: (1) Publicly available data in articles, manuals, data sheets, trade journals, application notes, other conferences, and press releases, which contain substantial technical information such as schematics, principles of operation, architectures, and algorithms. (2) Some previously, publicly-copyrighted material, such as in an IEEE publication. (3) Material submitted for which publication decision is still pending. (4) Material accepted for publication elsewhere. (5) Material available on a public website at any time up to the first day of the next ISSCC. Disclosures not considered pre-publication include: (1) Electronic copies of articles posted by authors on publicly accessible websites or preprint servers such as arXiv.org. IEEE policy regarding sharing and posting of articles is described in the IEEE Author Center. (2) Preliminary datasheets or a product announcement with no technical details. (3) Presentation at a limited-attendance workshop with no proceedings. A key element here involves the ability to find any handouts via electronic means or in a printed catalog. For example, if handouts are available to attendees of a workshop, but are not subsequently downloadable or orderable, this is acceptable. (4) Information from an advance program or information from IEEE-sponsored press meetings after publication or formal press release. (5) Information provided under non-disclosure agreements (NDA) to customers, partners, or other parties, (6) Final, signed versions of Master's or Ph.D. theses available in open repositories, either printed or online. A thesis published for profit is an exception and is considered prepublication. (7) Grant reports available in open repositories, either printed or online. (8) Published patents and patent applications. Authors must disclose all material that may fall into the pre-publication category as part of the submission process.

Acceptable Terminology: Please refer to the ISSCC website (https://www.isscc.org/call-for-papers-overview) for suggestions to replace historical terms that some may find objectionable.

For further details on Pre-Publication Policy, Double-Blind Review or assistance in assigning a subject area, contact the Program Chair: Tom Burd, Email: tom.burd@amd.com

POLICY REGARDING PAPER-SUBMISSION DEADLINE

Due to the timing constraints associated with the paper review process, Paper Submissions must be received by the deadlines shown below to be considered by the Program Committee.

DEADLINE FOR ELECTRONIC SUBMISSION OF PAPERS:

Wednesday, September 4, 2024 • 3:00 PM Eastern Daylight Time (19:00 GMT)

ISSCC 2025

SUNDAY-THURSDAY — FEBRUARY 16-20, 2025

SAN FRANCISCO MARRIOTT MARQUIS HOTEL, SAN FRANCISCO, CA

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ISSCC 2025 will be an in-person conference along with an option for remote attendees. Speakers are expected to present in person at ISSCC. The safety of our speakers and audience remains a paramount concern.
We will monitor global pandemic conditions and make adjustments to the conference format if needed.

ISSCC 2025 CALL FOR PAPERS

PLEASE CIRCULATE/POST ON BULLETIN BOARDS

SAN FRANCISCO MARRIOTT MARQUIS, SAN FRANCISCO, CA / FEBRUARY 16-20, 2025

**IF YOU NEED TECHNICAL ASSISTANCE,
PLEASE CONTACT THE APPROPRIATE SUBCOMMITTEE CHAIR OR REGIONAL CHAIR**

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**FOR FURTHER DETAILS ON PRE-PUBLICATION POLICY,
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