Criteria for Good JSSC Submissions on Digital Circuits and Systems

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The Journal of Solid-State Circuits is the premier publication outlet on integrated circuit design. Per the journal description, the topics relevant to the journal are: “The broad area of solid-state circuits with particular emphasis on transistor-level design of integrated circuits.” Submissions on digital designs, architectures, and systems have been featured prominently in JSSC for decades, including some of the most-cited work ever published in the Journal [1]. However, in recent years, an increasing number of submissions on digital circuits and systems have included little or no content related to the circuits focus of the journal, a trend exacerbated by the dramatic increase in submissions on machine learning accelerators. Though such submissions include a test chip, they may focus primarily on topics such as machine learning algorithms and high-level hardware architectures, with little content related to integrated circuit design, and as such are not well-aligned with the interest areas of the JSSC readership. This document is intended to provide clarity to authors, reviewers, and editors on common criteria for a good JSSC submission on digital circuit topics that is in line with the purpose of the Journal.

While a submission to the Journal can highlight algorithmic and digital architecture innovations (and should do so when relevant), it should also include substantial content related to the following topics in digital integrated circuit design:

1) Low-level microarchitecture or gate-level design, such as clock/data/power gating, pipelining, memory design or selection, hardware synchronization, or gate-level design of arithmetic blocks. Diagrams that include transistors or logic gates are typically necessary to describe this level of detail.
2) VLSI design topics, such as how and why a particular frequency target was selected, where the critical paths are located, how the floorplan was designed or optimized, how macros were placed, and which synthesis and place-and-route settings were chosen.
3) Implementation details of voltage and clock generation and distribution, including descriptions of clock and voltage domains, asynchronous crossings, power supply network optimization, timing optimization, packaging/IO interface design, and power management features.
4) Silicon measurement results that would be difficult to gather from pre-silicon simulation, such as performance data from long-running or system-level tests, power traces, energy measurements, captured traces of critical run-time signals, leakage power data, DVFS, or characterization of process variation impacts. As with any JSSC submission, measurements must be accompanied by a clear description of the bench measurement setup explaining what is included or excluded from performance and power measurements, what is executed on-chip, and how the system interfaces with external memory or other system components. For example, any measurement claims about end-to-end DNN execution should clearly state what is measured, what is estimated, and how the estimated portions are calculated.

Even a “pure digital” chip designer must necessarily grapple with these issues in implementing and testing a silicon prototype, and it is these topics that are best aligned with the Journal’s focus and the interests of its readers. It is certainly not the case that every digital submission must address *all* of these topics, but a submission that addresses *none* of them is not a good candidate for publication in the Journal, and can find a more suitable venue for publication. Note that submissions that are pre-published in a relevant circuits conference will still be evaluated on the above criteria, and such pre-publication is no guarantee that the higher standards for JSSC submission have been satisfied.

Papers that include substantial content on a preponderance of the topics noted above will be considered for inclusion in JSSC through the regular review process. Papers that do not meet these criteria should not be submitted as they are out of scope for this journal, and if submitted they will be rejected without review.

[1] Y. -H. Chen, T. Krishna, J. S. Emer and V. Sze, "Eyeriss: An Energy-Efficient Reconfigurable Accelerator for Deep Convolutional Neural Networks," in IEEE Journal of Solid-State Circuits, vol. 52, no. 1, pp. 127-138, Jan. 2017, doi: 10.1109/JSSC.2016.2616357.