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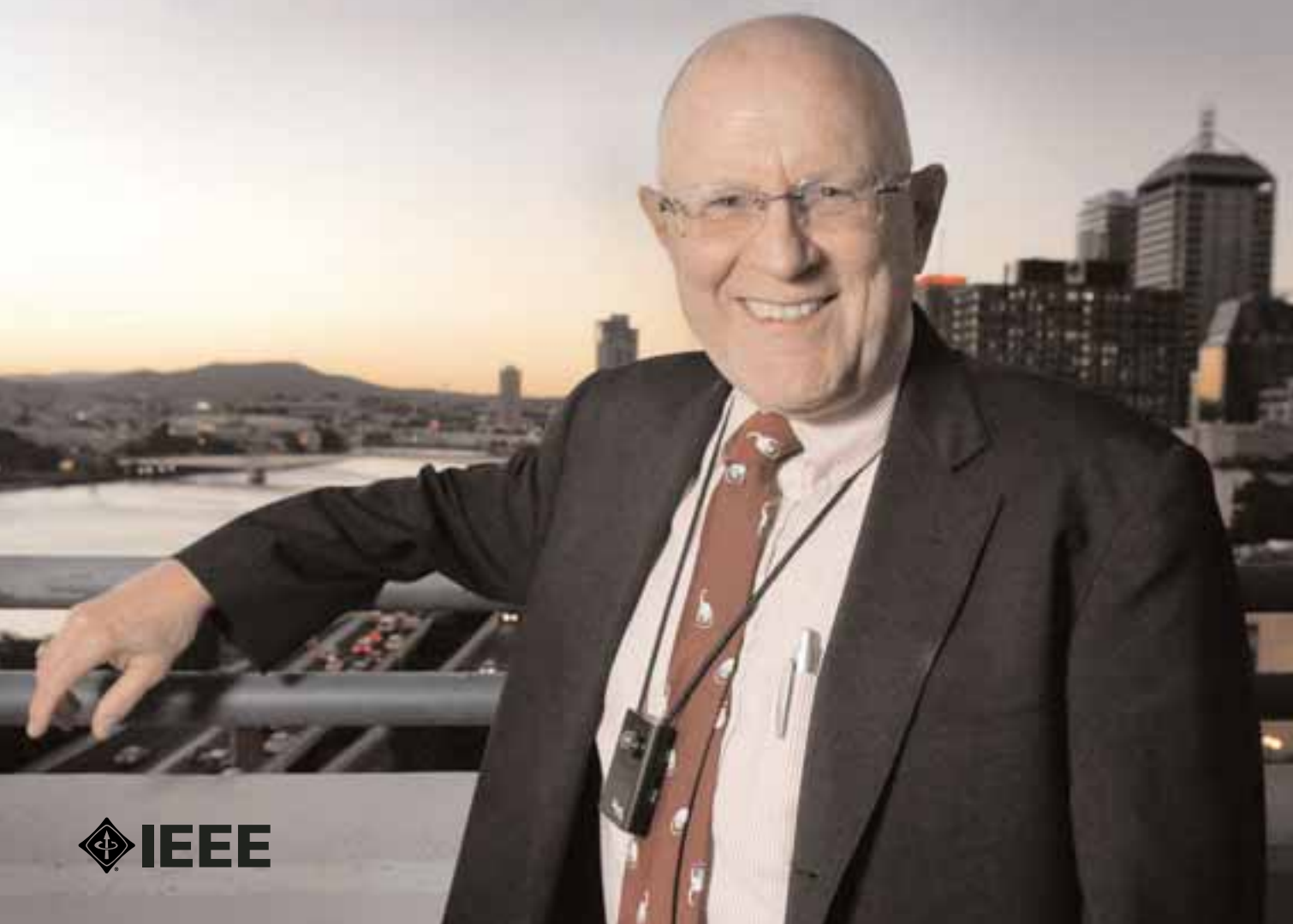
Gordon Bell

Bell's Law for the Birth and Death of Computer Classes



IEEE

Editor's Column

Mary Y. Lanzerotti, IBM, myl@us.ibm.com

As in the past, the goal of this issue is to be a self-contained resource, with original sources and new contributions by experts describing the current state of affairs in technology in view of the influence of the original papers and/or patents.

Since launching the redesign of the Newsletter in 2006, it has been our vision to provide the Society's 11,000 members with a publication that celebrates not only their technical accomplishments but also their personal achievements by reporting awards and publishing photographs, personal commentary, and special historical and business articles to provide coverage depth and breadth.

Throughout the past two years, Paul Doto of the IEEE Newsletter team has been on board with us every step of the way to convey our vision to SSCS members through the use of specially-requested design elements that he took the time to incorporate into each issue on our behalf.

Thanks to Paul, the layout of each issue has uniquely highlighted technical articles by and about our feature author, members' accomplishments and work-in-progress, educational outreach and our Distinguished Lecturer Program, Society news, and key activities of our conferences and chapters throughout the world.

To forward our vision, Paul went above and beyond to personally design full-color full-portrait covers based on author-supplied photographs and creative twists on our society's red and black theme. The distinguishing elements of our publication are its cover portraits, red-and-black cover theme and straightforward red title, black cover background, and interior section color highlights. We have personally promised all Feature Authors that their photos will appear on the cover, and Paul's efforts have elegantly fulfilled these agreements.

Thank you, Paul!! It has truly been a pleasure working with you.

Please consider sending a thank you to Paul for all of his hard work and commitment to our society's mission. His email address is p.doto@ieee.org; his webpage is http://www.pauldoto.com.

In this final issue of the SSCS News, we feature Gordon Bell, who has contributed an extensive new Feature Article entitled "Bell's Law for the Birth and Death of Computer Classes: A Theory of the Computer's Evolution." Dr. Bell is a principal researcher at Microsoft Research in Silicon Valley, working in the San Francisco Laboratory. His home page is: http://research.microsoft.com/~GBell. We are delighted to have the opportunity to present Dr. Bell and his work.

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IEEE Solid-State Circuits Society

SSCS News

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For questions regarding Society business, contact the SSCS Executive Office. Contributions for the Winter 2009 issue of the SSCS Magazine must be received by 8 November 2008 at the SSCS Executive Office. A complete media kit for advertisers is available at www.spectrum.ieee.org/mc_print. Scroll down to find SSCS.

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SSCS NEWS

President's Message

Willy Sansen, K. U. Leuven, willy.sansen@esat.kuleuven.be

Vision 2020

Some level of happiness and satisfaction was reached around the table at our AdCom meeting in San Francisco on August 18th because of the conversion of the Newsletter into a Magazine.

Although this may seem trivial, it is not. -- The Magazine will have much better quality in appearance and editing and, most important of all, will be saved from obsolescence, since it may be consulted through IEEE *Xplore*.

The Solid-State Circuits Society has worked hard to make this happen. -- It has been in the minds and on the table of Anne O'Neill, Katherine Olstein, and, of course, Mary Lanzerotti. They deserve to be complimented for their achievement.

Discussions that peered further into our future, however, about the breathtaking recommendations of an ad hoc committee formed last year to explore how ISSCC might look in 2020 were overwhelming.

According to the final report of ISSCC's Vision 2020 Task Force presented in San Francisco six times in three days by Dennis Monticelli, the conference may go virtual, and e-papers, an e-digest, and complementary materials such as an e-journal (whatever that means) may all have to be defined for a more efficient conference. [What is a more efficient conference? -- Will networking prevail over technical data transfer, or vice-versa? What is the common content between a conference paper and a journal paper? What is the most efficient way to put together a paper in terms of information transfer? Can the reproducibility of the results be enhanced? What can be done today rather than in 2020?]

Task Force actions taken already will result in four experimental satellite conferences that will be held next year in the Far East, within three weeks of the ISSCC. They will use the audio/video recorded sessions of the ISSCC and duplicate some of them within two to three days for local engineering communities. The same audio/video recorded sessions are currently available under ISSCC's "Replay-on-Demand" program four months after the Conference. Its success is slowly rising. Whether this product will reduce conference attendance is an open question. Everybody is also anxious to see how successful the satellite conferences can be, and also whether they will reduce attendance at the ISSCC in February.

The Vision 2020 Task Force report was heard in San Francisco by the Task Force itself, the ISSCC Long Range Planning Committee and ISSCC executive committees, the SSCS Meetings Committee chaired by Bill Bidermann and the SSCS Publications committee chaired by Glenn Gulak and, finally, by the AdCom itself. Dennis must be complimented for this task. His set of 27 slides not only addresses the future of the ISSCC but of all SSCS conferences, and even conferences in general. This set of slides will be used as a blueprint for a number of action committees within the Society. Obviously, they will also be used to tune results with recommendations generated by other Societies.

Exciting times, indeed, as noted several times by Dick Jaeger, Past-president of the SSCS.

Willy Sansen
President

Editor's Column *continued from page 2*

We also print an original paper by Dr. Eric Vittoz, who was the Feature Author of our Summer '08 issue, and two additional articles about his work:

(1) "Advances in Ultra-Low-Voltage Design," by Joyce Kwong and Anantha Chandrakasan (MIT);
(2) "Gigasensors for an Attoscope," by Erik H. M. Heijne (CERN).
(3) E. Vittoz, "Microwatt Switched Capacitor Circuit Design," Summer Course on Switched Capacitor Circuits, June 9-12, 1981, ESAT, Katholieke Universiteit Leuven, Heverlee, Belgium.

With this issue I would also like to welcome Pengfei Zhang as our new Associate Editor for the Far East. Please take this opportunity to read his first column, which appears in this issue. Dr. Zhang received his Ph.D. degree from Tsinghua University in Beijing, China, and was a post-doctoral scientist in the UCLA Electrical Engineering Department from 1994 to 1996. In 2005, Dr. Zhang co-founded Beken Corporation in Shanghai.

Thank you for reading the SSCS News! Please send comments and feedback to myl@us.ibm.com.

A Returnee from the US Becomes Entrepreneur in China

Beken Corporation Founder Muses about the IC Community in Shanghai

Pengfei Zhang, Beken Corporation, Shanghai pengfei@bekencorp.com

As I walked out of that conference room in the Shanghai Riverfront Business Hotel on 23 June, 2008, I was so impressed by the enthusiasm of the audience of 300 or more, and by the quality of their questions, that I turned to Prof. Ping Ko, the world's authority on device modeling and a pioneer in China IC venture investment, who said smilingly, "Rather encouraging indeed!"

That was not just another day. On June 23rd, most if not all analog IC designers, students and engineers had gathered in Shanghai to attend a seminar on "A New Transceiver Architecture for the 60-GHz Band," by Prof. Behzad Razavi, a real celebrity to the Chinese IC design community.

Held at Shanghai's Zhangjiang Hi-tech Park, one of the best technology incubators in China, the seminar was co-sponsored by the Shanghai Association for Science and Technology (SAST), the Shanghai Integrated Circuit Industry Association (SICA), and Beken Corporation (www.bekencorp.com), an IC design house I founded three years ago after moving back to Shanghai from the States.

More than 300 engineers -- virtually the entire analog IC design community in Shanghai – gathered in June to hear SSCS DL Behzad Razavi speak on "A New Transceiver Architecture for the 60-GHz Band."

When I started Beken, recruiting seemed to be a daunting task, as the talent pool was small at best and was hunted by an unprecedented number of design houses in the country. Three years had passed and, judging from the size and caliber of the audience in Prof. Razavi's seminar, I had no doubt that industry and academia had both been productive in spawning a new generation of analog IC designers.

June 23, 2008 was a special day to me for yet another reason, as Beken was celebrating the shipment of the 10,000,000th piece of its very first product -- a 5.8-GHz CMOS transceiver for wireless voice applications. Beken's 30-people team had good reason to be proud of what it had achieved within three years.

As a returnee entrepreneur leading one of the 500-and-more IC design houses in China, needless to say, I encountered challenges and

From left, Prof. Zi Xue, Vice General Secretary of Shanghai's Integrated Circuit Association, Prof. Ping Ko, Prof. Behzad Razavi, and Pengfei Zhang.

The author at Beken Corporation.

difficulties constantly, and tastes of success, too, sometimes with a bit of luck. It has been an exciting journey that I am happy that I made the decision to start. Nothing can compare to the excitement of seeing one's own design go into millions of products that could indeed make people's lives easier; this of course is on top of the sense of fulfillment that a great team has been built and trained.

So that's me. After graduating from Tsinghua University in Beijing, China with a Ph. D. in microelectronics in 1994, I luckily had the opportunity to work on shallow junction formation and SOI device modeling as a post doctoral fellow in Prof. Jason Woo's group at UCLA for two years before I joined the industry, working for Rockwell Semiconductor Systems, Fujitsu Microelectronics Inc., and later Resonext Communications, a startup in San Jose striving to deliver the most cost effective CMOS solution for then newly emerged IEEE 802.11a WLAN standard. That's where I began my RFIC design career, which led to a design engineering manager's job at RF Micro Devices after its acquisition of Resonext in 2002. Pursuing the dream of being part of the rapid development of China's IC industry, I returned to Shanghai with a group of friends after more than ten years in the United States.

Deeply submerged in the world's largest consumer market, inside a fast-growing design community with intensive semiconductor supply chain contacts and an extremely active capital market, I plan to report my first hand observations in my column for readers of the IEEE SSCS News.

In the winter issue of 2009, I will be looking at various exit options for IC Investment in China, especially the prospect of a China domestic stock market and, more interestingly, a Taiwan stock market (if opened to the mainland – a progressively greater possibility, as the newly elected leader in Taiwan seems to have more practical views). One of the corner stones of the prosperity of China's IC business is the unique ecosystem in China's Pearl River Delta -- a topic which will be the focus of my attention in the 2009 Spring issue.

In the Summer of 2009, I plan to share some observations on product definition and marketing strategies for an IC design house by focusing on platforms.

In the Fall 2009 issue, I will be examining the current IC design industry in China and its competitive dynamics, as well as the prospects of the China IC design business.

So stay tuned to the east side of the globe!

Solid-State Circuits Magazine and Redesigned Website to Launch in 2009

Anne O'Neill, SSCS Executive Director, a.oneill@ieee.org

The SSCS Newsletter will morph into the IEEE Solid-State Circuits Magazine with the winter issue of 2009, along with a revamped website that will debut in early December, 2008.

New Magazine to Prioritize Education

According to a survey in 2002, Society members want more educational material. The IEEE Solid-State Circuits Magazine will be the delivery vehicle for achieving that goal.

As the successor of the quarterly SSCS Newsletter, each issue of the Magazine will continue to be a self-contained resource for fundamental theories and practical advances within the field of Integrated Circuits (ICs); thanks to Newsletter Editor-in–Chief, Mary Lanzerotti, the founding fathers of IC fundamentals have been telling us how it all started. Mary was the driving force behind the evolution of the SSCS News into a full-color, magazine-style publication and will become Editor-in-Chief of the Magazine.

Written at a tutorial level and ideally in narrative style, it will feature articles by leaders from industry, academia and government that explain historical milestones, current trends and future developments to provide technical information to practitioners in the field who otherwise may have insufficient resources for keeping up to date.

Exceeding the format of the Newsletter, the Magazine will offer tutorials, special interest pieces, bibliographies, and distillations of cutting-edge work from scholarly publications and technical conference papers under the direction of Associate Editors Dick Jaeger and Rakesh Kumar. Newly appointed Associate Editor Pengfei Zhang will provide local news from the Far East and Australia (IEEE Region 10), while Associate Editor Tony Harker will continue to represent Europe, the Middle East and Africa (IEEE Region 8). Katherine Olstein will maintain coverage of SSCS chapter, membership and conference news.

First Issue to be Mailed in February

To maximize readability and reader interest in content we've already come to appreciate, the award winning IEEE Magazine staff has been engaged to design and produce our new publication. The print quarterly Magazine will continue to be mailed to SSCS members at no cost. The first issue will be mailed in early February, just in time for the ISSCC.

The Magazine will also be hosted in IEEE Xplore to provide readers the advantages of searchability, RSS feeds, and email alerts when issues are posted.

Non-member subscriptions in 2009 will cost $25 for the print publication, $10 for the electronic magazine in Xplore, and $30 for both.

Website Redesign Aims at Cutting Edge

The Society's new homepage will carry scrollable windows listing the contents of the current issue of the Society's flagship Journal of Solid-State Circuits and the new Solid-State Circuits Magazine. Best of all, it will be linkable to any recent article a user selects from either publication.

One-Stop Shopping for Sponsored-Conference Information

The Society's revamped website will offer a comprehensive list of SSCS-sponsored meetings. Derived from the IEEE conference database on a regular basis, it will ensure consistent reporting and provide a "one-stop shop" for conference dates and locations, manuscript (or abstract) submission deadlines, and links to conference home pages and conference homepages in Xplore. Information for conference organizers will include instructions for applying for SSCS technical co-sponsorship and how to use SSCS for publicity.

Platform for the Latest News

The revamped SSCS website will also feature breaking news about chapters, distinguished lectures, and IEEE conference and field awards, as well as new IEEE member programs like Expert Now and IEEE.tv, which offer content by SSCS experts that can be challenging for members and potential members to find. Additional web pages will provide useful "How to" instructions for acquiring SSCS products such as ISSCC Replay on Demand DVD's and other published conference articles on disk. After the launch of the new website, sscs.org will be redirected to a new host at IEEE headquarters but will retain its name.

Quarterly Email Blasts

The SSCS membership email blast will continue to provide announcements about important upcoming conferences, application deadlines, and member activities on a schedule that will be revised to maximize their timeliness, apart from the Magazine's print calendar. More information will be announced in an email blast in January.

Feedback

SSCS is interested in feedback from the IC community about our Magazine and website plans. Please discuss the changes we have described with any AdCom member, or send email to the Executive Director, a.oneill@ieee.org.

Parallel Processors are the Future Because Smaller Isn't Cool

Just as CPUs are becoming more parallel instead of smaller, so is news for the IC community. With the launch of our new Magazine and website, everyone will be able to receive email alerts for the Society and print versions of the JSSC and Solid-State Circuits Magazine. Or they can simply check-out the Society website for links to it all.

Bell's Law for the Birth and Death of Computer Classes: A theory of the Computer's Evolution[1]

Gordon Bell, Microsoft Research, Silicon Valley

Introduction

In 1951, a person could walk inside a computer and by 2010 a single computer (or "cluster') with millions of processors has expanded to building size. More importantly, computers are beginning to "walk" inside of us . These ends illustrate the vast dynamic range in computing power, size, cost, etc. for early 21st century computer classes.

A computer class is a set of computers in a particular price range with unique or similar programming environments (e.g. Linux, OS/360, Palm, Symbian, Windows) that support a variety of applications that communicate with people and/or other systems. A new computer class forms roughly each decade establishing a new industry. A class may be the consequence and combination of a new platform with a new programming environment, a new network, and new interface with people and/or other information processing systems.

Bell's Law accounts for the *formation, evolution, and death of computer classes* based on logic technology evolution beginning with the invention of the computer and the computer industry in the first generation, *vacuum tube computers* (1950-1960), second generation, *transistor computers* (1958-1970), through the invention and evolutions of the third generation *TTL and ECL bipolar Integrated Circuits* (1965-1985), and the fourth generation *bipolar, MOS and CMOS ICs enabling the microprocessor*, (1971) represents a "break point" in the theory because it eliminated the other early, more slowly evolving technologies. Moore's Law (Moore 1965, revised in 1975) is an observation about integrated circuit semiconductor process improvements or evolution since the first IC chips, and in 2007 Moore extended the prediction for 10-15 more years:

Transistors per chip = $2^{(t-1959)}$ for $1959 \le t \le 1975$; $2^{16} \times 2^{(t-1975)/1.5}$ for $t \ge 1975$.

In 2007, Moore predicted another 10-15 years of density evolution. The evolutionary characteristics of disks, networks, display, and other user interface technologies will not be discussed. However for classes to form and evolve, all technologies need to evolve in scale, size, and performance, (Gray, 2000) though at comparable, but their own rates!

In the first period, the mainframe, followed by minimal computers, smaller mainframes, supercomputers, and minicomputers established themselves as classes in the first and second generations and evolved with the 3rd generation integrated circuits c1965-1990. In the second or current period, with the 4th generation, marked by the single processor-on-a-chip, evolving large scale integrated circuits (1971-present) *CMOS became the single, determinant technology for establishing all computer classes*. By 2010, scalable CMOS microprocessors combined into powerful, multiple processor clusters of up to a million independent computing streams will certainly exist. Beginning in the mid 1980s, scalable systems have eliminated and replaced the previously established, more slowly evolving classes of the first period that used interconnected bipolar and ECL ICs. Simultaneously *smaller*, CMOS system-on-a-chip computer evolution has enabled low cost, small form factor or cell phone sized devices; PDA, cell phone, personal audio (and video) device (PAD, PA/VD), GPS and camera convergence into a single platform has become the worldwide personal computer, c2010. Dust sized chips with a relatively small numbers of transistors enable the creation of ubiquitous, radio networked, implantable, sensing platforms to be part of everything and everybody as a wireless sensor network class. Field Programmable Logic Array chips with 10s-100s of million cells exist as truly universal devices for building "anything".

Bell's Law Origin & Motivation—The Computer History Museum, a By-product

In 1966, after six years as a computer engineer at Digital Equipment Corporation, designing the first computers that established the minicomputer industry and the first timesharing computers, I joined the faculty of Carnegie Mellon University. While mentoring me for six years, Allen Newell and I wrote Computer Structures: Readings and Examples (Bell & Newell, 1971) which posited notations to describe computers, their behavior, and a taxonomy of computers including their constituent components. Working with Newell stimulated a deep concern about the origin of computers, classifying them (e.g. size, function, price, performance), and especially their evolution. Several of us wrote a paper (Bell et al, 1972) that showed computers were falling into several different price bands over time, similar to other manufactured goods e.g. cars, planes and in addition, new computers were being introduced in lower price bands afforded by the logic and memory technology.

On returning to Digital in 1972 as its VP of Engineering, I started collecting computer logic and memory technology in my office. Simultaneously, Ken Olsen, acquired two historically important MIT computers: Whirlwind (c1951), and TX-0 (c1956) that

[1] An abridged version of this paper has appeared in the Communications of the ACM, Vol. 51, No. 1, January 2008.

should be preserved for history, and that might be part of some eventual display. In 1975, I curated an exhibit of logic and memory in a converted coat closet of Digital's main office building, Maynard, MA that eventually moved and occupied the lobby of at Marlboro MA. Maurice Wilkes opened the Digital Computer Museum there in 1979.

As head of engineering and curator of a potential Computer Museum, I first spoke at MIT and elsewhere (Bell, 1972) about the future of computing based on logic technology. It also became clear that once established, a class stays roughly constant price. I used this basic idea to look back in time to create early generations: manual (1600-1800), mechanical (1800-1890), electro-mechanical (1890-1930, vacuum tube (1930-1960), transistor (1959-1966), integrated circuit 1966-1990), microprocessor (1971-present). In 1980 I gave a talk at Stanford's First Forsythe Lecture, "Generating Computer Generations" describing my theory on computer classes based on structure, technology, need, and actual use that has since been refined as I describe.

The museum became a public 501c(3) institution when it opened in Boston in 1983. In 1995 the artifacts moved to Silicon Valley, as the Computer History Museum, Mountain View, CA.

Bell's Law

A *computer class* is a set of computers in a particular price range defined by: a programming environment e.g. Linux, Windows to support a variety of applications including embedded apps; a network; and user interface for communication with other information processing systems including people and other information processing systems. A class establishes a horizontally structured industry composed of hardware components through operating systems, languages, application programs and unique content e.g. databases, games, pictures, songs, video that serves a market through various distribution channels.

The universal nature of stored program computers is such that a computer may be programmed to replicate function from another class. Hence, over time, one class may subsume or kill off another class. Computers are generally created for one or more basic information processing functions– storage, computation, communication, or control (see Figure1 Taxonomy). Market demand for a class and among all classes is fairly elastic. In 2010, the number of units sold in classes vary from 10s, for computers costing around $100 million to billions for small form factor devices e.g. cell phones selling for under $100. Costs decline by increasing volume through manufacturing learning curves (i.e. doubling the total number of units produced result in cost reduction of 10-15%). Finally, computing resources including processing, memory, and network are fungible and can be traded off at various levels of a computing hierarchy e.g. data can be held personally or provided globally and held on the web.

Figure 1. Taxonomy of computer functions (applications) taxonomy divided into personal and non-personal, i.e. institutional infrastructure computers that carry out calculation, record keeping and transaction processing, networking and personal communication (e.g. word processing, email, web), control, personal health, and entertainment functions. Note the convergences: personal media device, PDA, camera, cell phone become the Smart Phone; Entertainment devices of TV, Media Centers & Servers.

The class creation, evolution, and dissolution process can be seen in the three design styles and price trajectories and one resulting performance trajectory that threatens higher priced classes: an established class tends to be re-implemented to maintain its price, providing increasing performance; minis or minimal cost computer designs are created by using the technology improvements to create smaller computers used in more special ways; supercomputer design, i.e. the largest computers at a given time, come into existence by competing and "pushing technology to the limit" to meet the unending demand for capability; and the inherent increases in performance at every class, including just constant price, threaten and often subsume higher priced classes.

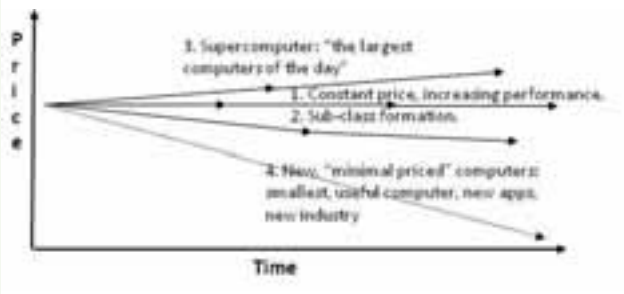

Figure 2. evolving computer classes based on technology and design styles: 1. constant price, INcreasing Performance; 2. sub-class, lower price and performance to extend range; 3. supercomputer – largest computers that can be built that extend performance; and 4. new, minimal, order of magnitude lowe priced class formations every decade.

All of the classes taken together that form the computer and communications industry shown in Figure 2, behave generally as follows:

1. *Computers are born* i.e. classes come into existence through intense, competitive, entrepreneurial action over a period of 2-3 years to occupy a price range, through the confluence of new hardware, programming environments,

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networks, interfaces, applications, and distribution channels. During the formation period, 10s to 100s of companies compete to establish a market position. After this formative and rapid growth period, 2 or 3, or a dozen primary companies remain as a class reaches maturity depending on the class volume.

2. *A computer class, determined by a unique price range evolves in functionality and gradually expanding price range of 10* maintains a stable market. This is *followed by a similar lower priced sub-class that expands the range another factor of 5 to 10*. Evolution is similar to Newton's First Law (i.e. bodies maintain their motion and direction unless acted on externally). For example, the "mainframe" class was established in the early 1950s using vacuum tube technology by Univac and IBM and functionally bifurcated into commercial and scientific applications. Constant price evolution follows directly from Moore's Law whereby a given collection of chips provide more transistors and hence more performance.

   A lower entry price, similar characteristics sub-class often follows to increase the class's price range by another factor of 5 to 10, attracting more usage and extending the market. For example, smaller "mainframes" existed within 5 years after the first larger computers as subclasses.

3. *Semiconductor density and packaging inherently enable performance increase to support a trajectory of increasing price and function*

   3.1 *Moore's Law single chip evolution, or microprocessor computer evolution after 1971 enabled new, higher performing and more expensive classes*. The initial introduction of the microprocessor at a substantially lower cost accounted for formation of the initial microcomputer that was programmed to be a calculator. This was followed by more powerful, more expensive classes forming including the home computer, personal computer, workstation, the shared microcomputer, and eventually every higher class.

   3.2 *The supercomputer class c1960 was established as the highest performance computer of the day*— however, since the mid-1990s supercomputers are formed by combining the largest number of high performance computers to form a single, clustered computer system in a single facility. In 2010 over a million processors will likely constitute a cluster. Geographically coupled computers including GRID computing e.g. SETI@home are outside the scope.

4. *Approximately every decade a new computer class forms as a new "minimal" computer either through using fewer components or use of a small fractional part of the state-of-the-art chips*. For example, the 100 fold increase in component density per decade enables smaller chips, disks, screens, etc. at the same functionality of the previous decade especially since powerful microprocessor cores e.g. the ARM use only a few <100,000 transistors versus over a billion for the largest Itanium derivatives.

   Minimal computers design. Building the smallest possible computer accounts for the creation of computers that were used by one person at a time and were forerunners of the workstation e.g. Bendix G-15 and LGP 30 in 1955, but the first truly personal computer was the 1962 Laboratory Instrument Computer (LINC). LINC was a self-contained computer for an individual's sole use with appropriate interfacial hardware (e.g. keyboards, displays), program/data filing system, with interactive program creation and execution software. Digital Equipment's PDP-1 (1961), followed by its more "minimal" PDP-5 & 8 established the minicomputer class that were predominately designed for embedded applications.

   System-on-a-Chip (SOCs) use a fraction of a chip for the microprocessor(s) portion or "cores" to create classes and are the basis of fixed function devices and appliances beginning in the mid 1990s. These include cameras, cell phones, PDAs, PAD (personal audio & video devices) and their convergence into a single cell phone sized device (CPSD) or small form factor (SFF) package. This accounts for the PC's rapidly evolving microprocessor's ability to directly subsume the 1980's workstation class by 1990.

5. *Computer classes die or are overtaken by lower priced, more rapidly evolving general purpose computers* as the less expensive alternatives operating alone, combined into multiple shared memory micro-processors, and multiple computer clusters. Lower priced platforms result in more use and substantially higher volume manufacture thereby decreasing cost while simultaneously increasing performance more rapidly than higher priced classes.

   5.1 Computers can be combined to form a single, shared memory computer. A "multi" or multiple CMOS microprocessor, shared memory computer displaced bipolar minicomputers c1990 and mainframes c1995, and formed a component for supercomputers.

   5.2 Scalable, multiple computers can be networked into arbitrary large computer to form "clusters "that replace custom ECL and CMOS vector supercomputers beginning mid 1990s simply because arbitrarily large computers can be created. Clusters of multiprocessors were called constellations; clusters using low latency and proprietary networks are

MPPs (massively parallel processors).

5.3 *Generality ALWAYS Wins! A computers created for a particular, specialized function e.g. word processing, interpreting a language, used for a particular application is almost certain to be taken over by a faster evolving, general purpose computer.* The computer's universality property allows any computer to take on the function of another, given sufficient memory and interfaces.

5.4 Small form factor devices subsume a personal computing functionality as they take on the communications functions of the PC (e.g. email and web browsing), given sufficient memory and interfaces. Small form factor devices or television sets or kiosks accessing supercomputers with large stores, subsume personal computing functionality. The large central stores retain personal information, photos, music, and video.

The paper will describe how these characteristics of the classes account for the birth, growth, diminution, and demise of various parts of the computers and communications industry.

Overview of the Birth and Death of the Computer Classes 1951-2010

Figure 1 is a computer function taxonomy based: first on buyers/users and second, by application. The information processing elements i.e. application functions are: memory or storage for record keeping that was the province of IBM and other card tabulation equipment makers prior to the computer's invention; computation or calculation characterizing science and engineering use; networking and communication that provide the interconnection infrastructure; control of other systems (e.g. process control); and interface with humans and other information processing entities.

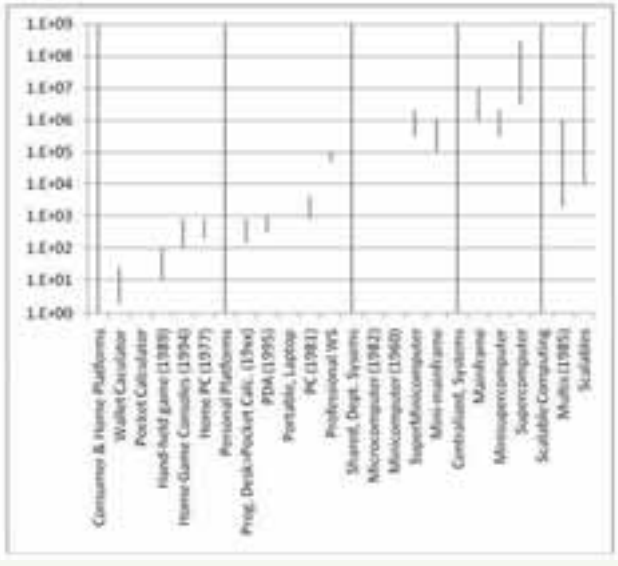

Figure 3. Computer Classes and their Price Range 2005

The taxonomy is divided first into personal and non-personal or invisible and shared, institutional infrastructure systems that would be operated within or for a company, government or institution as a service. This dichotomy of personal versus shared; invisible versus institutional determines characteristics of price and scale, programming environment, user interface, and network. Function though critical, will be neglected.

The named classes and their price range c2010 is given in Figure 3. David Nelson, founder of Apollo. and I (Nelson, Bell 1986) posited that the price of a computer was roughly $200 per pound. Figure 4 gives the introduction price and date of the first or defining computer of a class. Table 1 gives the defining constituent technologies, operating systems, languages, networks, and interfaces of the various classes.

The discussion will use the aspects of Bell's Law described above and follow a timeline of the class formations beginning with the establishment of the first computer classes (mainframe, supercomputer, shared personal professional computers or workstations, and minicomputers) using vacuum tubes, transistors, and bipolar integrated circuits that continue through the mid 1990s. The MOS microprocessor introduced in 1971 ultimately overtook bipolar by 1990 to establish a single line based on CMOS technology.

The section is followed by the three direct and indirect effects of Moore's Law to determine classes:

1 Microprocessor transistor/chip evolution c1971-1985 establish: calculators, home computers, personal computers and workstations, and lower (than minicomputer) priced computers.

2 "Minimal" designs establish new classes c1990 that use a "fraction" of the Moore number. Microsystems evolution using fractional Moore's Law sized SOCs enable small, lower performing, minimal personal computer and communication systems including PDAs, cameras, cell phones, personal audio/video devices.

3 Rapidly evolving microprocessors using CMOS and a simpler RISC architecture appear as the "killer micro" c1985 to have the same performance as supercomputers, mainframes, mini-supercomputers, super-minicomputers, and minicomputers built from slowly evolving, low density, custom ECL and bipolar integrated circuits. ECL survived in supercomputers the longest because of its speed and ability to drive the long transmission lines, inherent in large systems. In the end, CMOS density and faster system clock overtook ECL as shown in Figure 5.

The "killer micro" enabled by fast floating point arithmetic, first subsumed the workstation followed by the minicomputer especially when combined to form the "multi" or multiple microprocessor shared memory computer c1985. "Multis" became the component for scalable clusters when interconnected by high speed, low latency networks. Clusters allow

Table 1. The Computer classes, hardware and software enablers, network, and use.

Class & Lifetime	Hardware Platform (logic, memories)	User Interface & control, Operating System, Languages	Network infrastructure	Use
Mainframes: Commercial & Science. Industry Formation 1951	Inventing **'the computer",** vacuum tube totransistor, core, drum & mag tape to disk, card, paper tape. **Drum;**	direct user control evolving to batch operating systems (O/S) 1960: COBOL & FORTRAN	computers operated as independent stand-alone entities	Accounting & Records, Scientific Calculations
Small, shared,personal computers for work (1956-				
Interactive timesharing replaces Batch (1965)	IBM RJE, DEC PDP-10	**glass teletype** & glass keypunch, command language control	POTS using **modem,** and proprietary nets using WAN	Service centers;
Minicomputers 1965-90; Super-minicomputers (1980-1990)	integrated circuit (IC), disk , minicomputer; multiprogramming			Real time for process control & lab; network switch, departmental timeshared "mainframe"
Supercomputers 1965-1995 The largest scientific computer.	**Transistor discrete to ECL small scale ICs**	**FORTRAN**	Batch and remote batch from terminals and card equipment	Science & engineering; design, simulation
Mini-Supercomputers	Cray-ettes. CMOS implementation of Cray vector multiprocesso	FORTRAN		
Scalables: MPPs, Clusters, and Constellations				
Calculators, Home Personal Computers based on 1st microprocessor: 1971-1975	Microprocessor		**Stand-alone use**	
PCs, Workstations, and LANs (1981)	**microprocessor** PCs & workstations, floppy, small disk, dist'd O/S	**WIMP (windows, icons, mouse, pull-down menus)**	**WAN, LAN**	
World-Wide Web. Access via PCs and Workstations (1994)	Evolutionary PCs and workstations, servers everywhere, Web O/S	Browser	**fiber optics backbone, www, http**	
Convergence: Cell Phone, Personal Digital Assistant (PDA), Digital A/V Player (DAP) , Camera …SmartPhone.				
Web Computers: Network-, Tele-, TV- computers (1998)	client software from server using JAVA, Active X, etc.	telephone, simple videophone, television access to the web	**xSDL** for POTS or cable access for hi speed data; 3 separate networks	
SNAP: Scalable Network & Platforms (1998)	PC uni- or multi-processor commodity platform	server provisioning	SAN (System Area Network) for clusters	All computers
Convergence: Ubiquitous IP: phone, TV, data, & videophone (2010)	Video capable devices of all types;	video as a primary data-type	Single high speed network access; Home Net	
Wireless Sensor Nets (2005) Connecting all "things"				
Embedding of speech & vision functions (2020)	$1-10 of chip area for: books, pictures, papers, that identify themselves		**Body Net** , Home Net, other nets	
Body Net: vision, hearing, monitoring, control, comm., location (2015)	artificial retina, cochlea, glasses for display,	implanted sensors and effectors for virtually every part of a body	Body Network, gateway to local IR or radio nets everywhere	

arbitrarily large computers that are limited only by customer budgets. Thus scalability allows every computer structure from a few thousand dollars to several hundred million dollars to be arranged into clusters built from the same components.

In the same fashion that killer micros subsumed all the computer classes by combining, it can be speculated that much higher volume, hundreds of millions, of small form factor devices, may evolve more rapidly to subsume a large fraction of personal computing. Finally tens of billions of dust sized, embeddable wirelessly connected platforms that connect everything are likely to be the largest class of all enabling the state of everything to be sensed, effected, and communicated with.

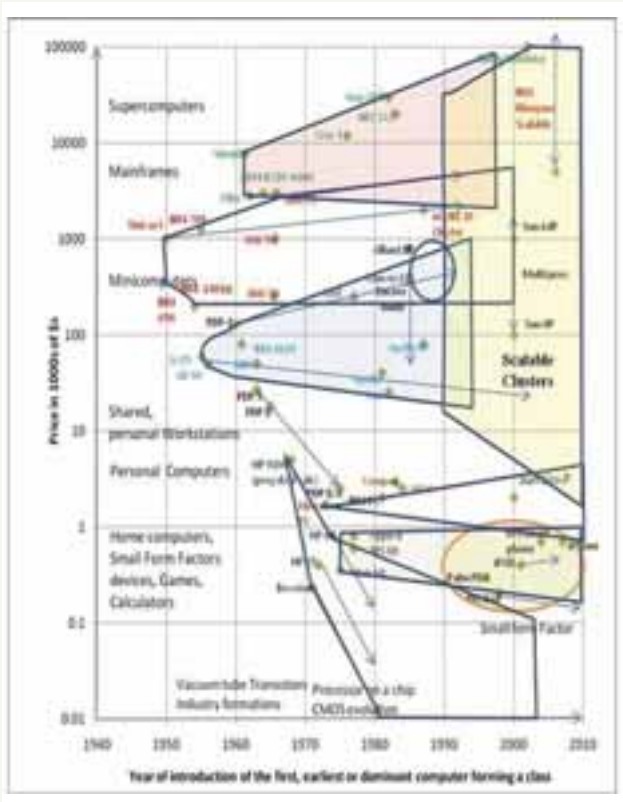

Figure 4. Introduction price versus date of the first or early platforms to establish a computer class or lower priced sub-class orginating from the same company or industry.

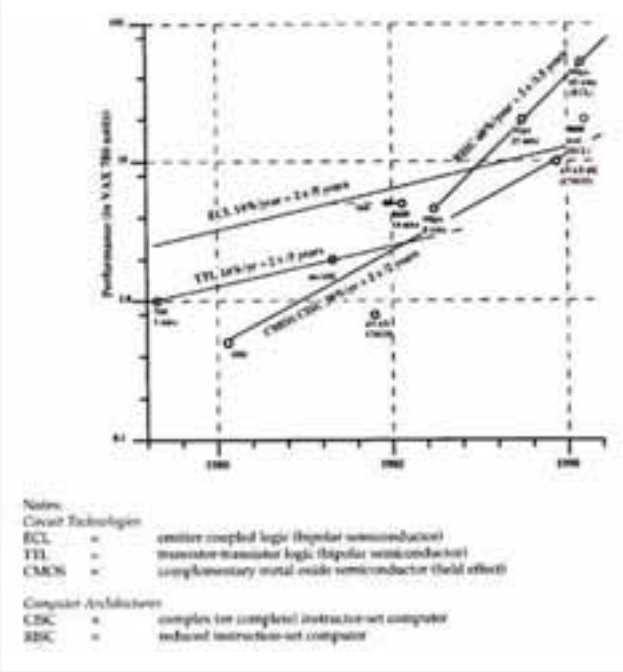

Figure 5. Faster evolving CMOS microprocessors are able to overtake and eliminate slowly evolving TTL and ECL bipolar integrated circuit based computer classes including minicomputers, superminicomputers, mini-supercomputers, mainframes, and supercomputers. A number of companies built one or more Too many ECL computers including CDC, Cray, DEC, Fujitsu, Hitachi, and IBM before switching to ECL.

The Past: How we got here

The Beginning (1951-1990): mainframe, supercomputer, shared personal workstation, and minicomputer classes

By 1970, vacuum tube (50s), transistor (60s), and small scale integrated circuit (late 60s) technologies enabled the establishment of four classes of computers that continued almost without change until the 80s:

1. Mainframes for commercial, record keeping, etc. and mainframes for Scientific and Engineering Computation were the very first computers; a sub-class of smaller computers formed that were used in the same fashion.
2. Minimal design, small, shared computers that were used directly as personal workstations
3. Minimal computers for process and machine control, communication, and embedded apps
4. Supercomputers constructed at the limits of circuit, interconnect, and architectural complexity utilizing clock speed and parallelism

Eckert and Mauchly, operating as the UNIVAC division of Remington Rand delivered the UNIVAC 1 as the earliest commercial computer in 1951, roughly concurrent with the British LEO (Lyons Electronic Office) computer, and followed two years later by the IBM 701 (1953) for scientific applications. These first computers with delay line and electrostatic (Williams Tube) memories of only a few thousand words were priced at $1 million or more ($8.5 million in 2007 dollars) to establish the mainframe class. By 1955, IBM had introduced both scientific (701, 704) and commercial (702, 705) computers that were differentiated by their ability to deal with floating point data of high precision versus the predominately alphanumeric and decimal arithmetic operations typifying data processing. From the graph, the mainframe increased to $4 million and continued to maintain the price range. A set of smaller computers were introduced in the price $0.1- 1 million range e.g. IBM 1401 and 650 for departmental and smaller organization use. These could be classified as subclass of mainframes or super-minicomputers. During the mainframe's formation, eight US and five? European companies competed to establish the class. The US Group was known as Snow White and the Seven Dwarfs or BUNCH (Burroughs, Univac now Unisys, NCR, CDC, Honeywell)+ GE & RCA. With IBM's introduction of System 360 on April 7, 1964, the dominant architecture was established and will doubtlessly remain to run legacy applications "forever" – given the trillions of dollars of software and data that this ecosystem hosts.

Small or minimal computers priced between $60,000 to $120,000 that a person signed up for and used directly for calculation or personal computing at work were introduced beginning in the mid 1950s (Bendix G-15, Librascope LGP-30), as well as the transistorized IBM 1620 that dominated the class. In 1961, the DEC PDP-1 was applied to telegraph line message switching as a prelude to computer net-

working, peripheral computers for mainframes (like the 1401 or CDC 160), and were used as prototypes for timesharing system.

The PDP-8, introduced in 1965 at a price of $18K is the first "minicomputer." It was minimal, designed as both the smallest computer that could be built and as a component to be used for controlling other devices e.g. process control, lab instruments, terminal concentrators. On occasion it was used as a workstation on a personal basis with an operating system that was a pre-cursor to DOS. The PDP-8 had a dozen implementations following a minimal cost trajectory with single chip versions beginning in 1975 to both define and increase its marketability including its use as a dedicated word processor to the early 1980s. During the minicomputer class formation period, 92 companies formed to establish the minicomputer class with only IBM and HP remaining by 2000 to make computers in this class albeit with substantially changed architectures. Including DEC VAX in this class, the price range increased to cover a range of $10,000 to $1,000,000 servers and covering the entire potential application space of the day. The most expensive VAXen, and VAX clusters competed with IBM smaller System/360 class and sub-mainframes.

The reliable and fast transistor circuitry c1960 enabled a substantially larger number of components to be integrated into a unified system, limited mostly by the maximum feasible selling price, architectural complexity, and interconnection density. Early on, vying for the title of world's fastest computer, were the Manchester Atlas I and the IBM 7030 ("Stretch"), both introduced in 1961. Five years later, the CDC 6600 supercomputer was introduced as the culmination of several years of effort by a small team led by Seymour Cray. It used about 500,000 densely packaged silicon transistors and stunned the world with its performance—easily an order of magnitude faster than any computer shipping at the time or even being contemplated. "Cray sytle" computers based on parallelism functional units, followed by vector processors continued relatively unchallenged for 30 years. In the mid-90s, things had changed somewhat architecturally but bipolar technology still reigned. The fastest machines were shared memory, vector processors using small scale ECL ICs. Successful challengers at Fujitsu and NEC uses the "Cray" formula to build even faster machines with the NEC Earth Simulator holding the title from 2002-2005.

Why Computer Classes Evolve at Constant Price, Increasing Performance

Once a computer class forms, several factors determine the price of the "next" evolutionary model. Building the next model in 3-5 years with chips that have 4 to 6 times more transistors is the natural predicted progression of Moore's Law.

Increases in processing power and memory size are essential for the new data-types such as music, photos, and data-bases. The number of pixels per camera evolve about as rapidly as Moore's Law, requiring more memory and speed to handle the images with constant response. Similarly, disk memories have to evolve rapidly to store the higher resolution photos, higher quality videos, etc.

Nathan's Law, also attributed to Bill Gates, explains software's increasing demand for resources:

1. Software is a gas. It expands to fill the container it is in.
2. Software grows until it becomes limited by Moore's Law.
3. Software growth makes Moore's Law possible through the demand it creates; and
4. Software is only limited by human ambition and expectation.

"Marketing" nominally fueled by user feedback for more functionality, forms the critical link in support of Nathan's Law that minimalist refer to as featuritis, bloat, etc. enabling upgrades to support periodic obsolescence.

We might expect to buy a new computer in three years at 1/4 the price of today's computer using chips that are 1/4 the size of an earlier model perhaps from the same manufacturer. Why not? New microprocessors sell at the same or even a price premium because they have 4x the transistors, faster clock speed and deliver more performance. For example, Intel and AMD are not inclined to build microprocessors with less transistors and lower cost because they don't see such a market – and as such do not participate in establishing the new, lower price classes. Also, a computer is made of other parts e.g. metal and power supplies that may increase in price and act to hold the system price constant with only system manufacturing learning curves left to decrease price.

The "numbers" support a next generation product of constant price and increasing performance, not one of decreasing prices and constant performance. Assume the total cost of ownership is at least 3x the computer's sales price, and for a computer of performance = 4.

performance/total cost = 4/4

Assume a new, constant price, double performance computer performs at 4 x 2 or 8, then

Performance/total cost = 8/4 or 2. Contrast this with a constant performance computer of 4, whose price is just 3/4, giving a total cost of 3.75

Performance/Total cost = 4/3.75 or 1.07

The final and most important incentive to hold price constant and provide more capability is to retain a user's substantial investment in legacy applications and data that have been created together with the implied user and organizational learning. The value of data is most likely to be 10-100 times the hardware cost. A user retains an old computer unless it is unreliable, or there is a substantial increase in functionality – as long as the new model accepts legacy apps and data. The cost to switch to another computer, even with the same capability is so high that the incentive must result in a significant

benefit as the above numbers show.

Finally, most goods e.g. cars, construction material, energy, and food not subject to CMOS integration, increase in price with inflation (Table 2). However, computers have defied inflation -- the 1984, 9" monochrome 128 Kbyte, single floppy, integrated $2495, Apple Macintosh costs $1500; in 2007, the same, as a 13" color portable with 1 GB memory and 80 GB disk.

Table 2. Consumer Price Index showing Buying Power since the introduction of computers in 1951 Versus $1 in 2007.

1950	1960	1970	1980	1990	2000	2007
8.5	6.9	5.3	2.5	1.6	1.2	1

Microprocessors 1971: The Technological Force for New Classes in the Second Period

Figure 6 shows the microprocessors derived directly from the growth of transistors/chip beginning in 1971. It shows the trajectory of microprocessors from a 4-bit data path through, 8-, 16-, 32-, and 64-bit data paths and address sizes. The figure shows a second path – the establishment of "minimal" computers that use less than 50 thousand transistors for the processor, leaving the remainder of the chip for memory and other functions e.g. radio, sensors, analog I/O enabling the complete SOC. Increased performance, not shown in the figure, is a third aspect of Moore's Law that allows the "killer micro" formation to subsume all the other, high performance classes that used more slowly evolving bipolar TTL and ECL ICs (Figure 5). The final section will discuss the challenge of having a single chip with billions of computing elements (functional units, processors, computers, wireless links and other I/O).

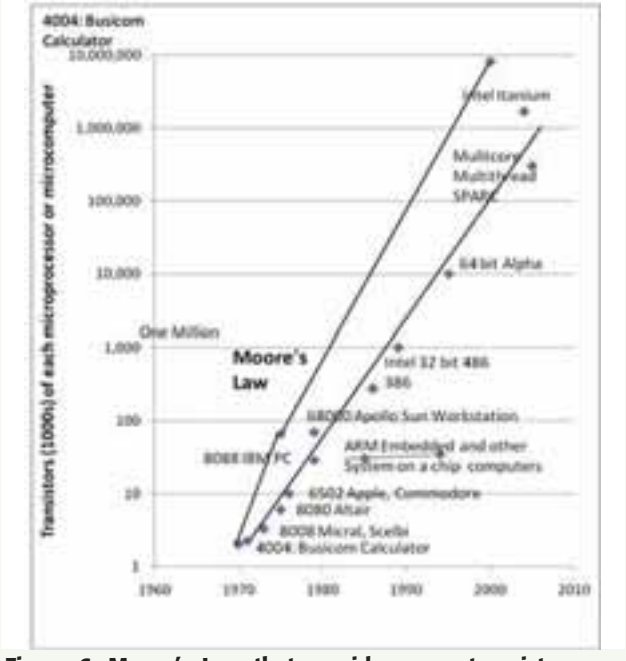

Figure 6. Moore's Law that provides more transistors per chip, has resulted in creating the following computer classes: calcultaors, home computers, personal computers, workstations, "multis" to overtake minicomputers, and clusters using multiple core, multi-threading to ovetake mainframes and supercomputers.

Microprocessor Evolution c1971-1985: Personal Computing (Calculators, Home Computers, Personal Computers, Workstations, and Game Console Platforms)

Calculators, home computers, personal computers, and workstations were established as classes as the processor on a chip evolved to have more transistors with wide data paths and large address spaces as shown in Figure 6.

In 1971, Intel's 4004 with 4 bit data path and ability to address 4KB was developed and programmed to be the Busicom Calculator; instead of developing a special chip as had been customary to implement calculators, a program was written for the 4004 for it to "behave" as or "emulate" a calculator. The 4004 with a 4 bit data path was not suited for storing text and larger numbers other than in a serial fashion, although it was used for numerous applications and to spawn an "embedded computer" market just as the minicomputer had done a decade earlier.

In 1972, Intel introduced the 8008 microprocessor coming from the Datapoint terminal requirement, with 8 bit data path and ability to access 16 KB that allowed R2E's Micral computer (France) and Scelbi to build limited, programmable computers followed by more powerful 8080-based systems that M.I.T.S. used to introduce its "Atltair" personal computer kit in 1975, that incidentally stimulated Gates and Allen to start Microsoft. The more powerful and upward compatible Zilog Z80 was useful in helping to establish a personal computing platform. In 1977, the 16-bit 6502 microprocessor and higher-capacity memory chips enabled personal computers for use in the home or classroom built by Apple, Commodore and Radio Shack—computers that sold in the tens of millions because people bought them to use at home versus corporate buyers. By 1979, the VisiCalc spreadsheet ran on the Apple II establishing it as a "killer app" for personal computers in a work environment. Thus the trajectory went from a 4-bit data path and limited address space to a 16-bit data path with the ability to access 64KB of memory. This also demonstrates the importance of physical address as an architectural limit. In the paper on DEC's VAX (Bell, Strecker 1975), we described the importance of address size on architecture: "There is only one mistake that can be made in a computer design that is difficult to recover from – not providing enough address bits for memory addressing and memory management…" The 8086/8088 of the first IBM PCs had a 20-bit, or 1MB address space, the operating system using the remaining 384KB.

Concurrent with the introduction of the IBM PC, professional workstations were being created that used the Motorola 68000 CPU with its 32-bit data and address paths (4GB of maximum possible memory). Apple Computer used the Motorola "68K" in its Lisa and Macintosh machines. IBM's decision to use the Intel architecture with limited addressing, undoubtedly had the effect of impeding the personal computer by a decade as the industry waited for Intel to evolve architecture to support a larger address and virtual memory space. Hundreds of companies start-

ed up to build Personal Computers ("PC-clones") based on the IBM PC reference design c1981. Dozens of companies also started to build workstations based on a 68K CPU running the UNIX operating system. This was the era of "JAWS" (Just Another WorkStation) to describe efforts at Apollo, HP, IBM, SGI, SUN and others based on 32-bit versus 16-bit microprocessors and including specialized systems for Word Processing (Wang, Xerox), Market Analysis (Metaphor), CAD (Intergraph, Daisy, Valid), and high-level programming (Lisp Machines and Symbolics). Virtually all of these "workstations" were eliminated by simple economics as the Personal Computer--based on massive economies of scale and commoditization of both the operating system and all constituent hardware elements) evolved to have sufficient power and pixels.

"Minimal" CMOS Microsystems on a Chip c1990 Establish New Classes Using Smaller, Less Expensive, Chips

In 2007, many systems are composed of microprocessor components or "cores" with less than 50,000 transistors per microprocessor core at a time when the leading edge microprocessors chips have a billion or more transistors cf Figure 6. Such cores using lower cost, less than the state-of-the-art chips and highly-effective, rapid design tools allow new, minimal classes to emerge allow new, minimal classes to form. PDAs, cameras, cell phones, and personal audio & video devices have all been established using this "minimal" computer design style based on small "cores". In 1990, the Advanced RISC Machine (ARM) formed from a collaboration between Acorn and Apple as the basis for embedded systems that are used as computing platforms and achieve two billion units per year in 2006. Other higher volume microsystem platforms using 4-, 8-…64-bit architectures including MIPS exist as core architectures for building such systems as part of the very large "embedded" market.

Rapidly Evolving "Killer CMOS Micros" c1985 Overtake Bipolar ICs to Eliminate Established Classes

In the early 1980s, the phrase "killer micro" was introduced by the technical computing community as they saw how the more rapidly evolving CMOS micro would overtake bipolar based minis, mainframes, and supers if they could be harnessed to operate as a single system and operate on a single program or workload.

In the Innovator's Dilemma, Christensen describes the death aspect basis of Bell's Law by contrasting two kinds of technologies. *Sustaining* technology provides increasing performance enabling improved products at the same price as previous models using slowly evolving technology; disruptive, rapidly evolving technology provides lower priced, products that are non-competitive with higher priced sustaining class to create a unique market space. Over time, the performance of lesser performing, faster evolving products eventually overtake the established, slowly evolving classes served by sustaining technology.

From the mid 1980s till 2000, over 40 companies were established and wiped out attempting to exploit the rapidly evolving CMOS microprocessors by interconnecting them in various ways. Only Cray, HP, IBM, SGI and SUN remain in 2007 to exploit massive parallelism through running a single program on a large number of computing nodes.

Let's look at two potentially disruptive technologies, establishing new classes:

The OLPC (One Laptop Per Child) project of Nicholas Negroponte aimed at a $100 PC (costing about $188 in 2007) is quite likely disruptive as a "minimal" PC platform that relies on the internet for storage of programs and data. Cost reduction is achieved by substituting 500 MB of flash memory for disk, reduced screen size, small main memory, and built in mesh networking to reduce infrastructure cost. An expected selling price of $200 with a $188 cost that is about half the price of the least expensive PCs in 2007, is characteristic of a new sub-class. OLPC will be an interesting development since Microsoft's Vista requires almost an order of magnitude more system resources.

The evolving small form factor devices such as cell phones are likely to have the greatest impact on personal computing, effectively creating a class. For perhaps most of the 4 billion non-PC users, it becomes their personal computer and communicator, wallet... map, etc. since the most common and often only use is of personal computers is for email and web browsing – both stateless applications.

Application of Bell's Law-- Planning VAX and the VAX Strategy

In 1975 when VAX was in the planning stage, I used the theory of classes to posit a compatible line of computers that had the same instruction set and programming environment that could be used in a range of uses including personal computers, process control , departmental timesharing, and clusters for large scale apps. The planning was based on the different sized memories resulting in different prices according to the following pricing model:

System Price = 5 x 3 x .04 x memory size/ 1.26 (t-1972) K$

Where 5x: Memory is 20% of cost; 3x: DEC markup; .04x: $ per byte; 26%: price change

Figure 7 shows the prices for systems of various sized memories. The large price declines were in fact one of the root causes of the demise of Digital in the late 90s. In effect, the large memories required to maintain pricing in a price band required larger amounts of processing that were served by clusters of microprocessor based computers connected as clusters. Another cause at DEC was continuing with ECL at a time when CMOS overtook it in speed and especially exorbitant cost when nearly zero cost, microprocessors were outperforming ECL.

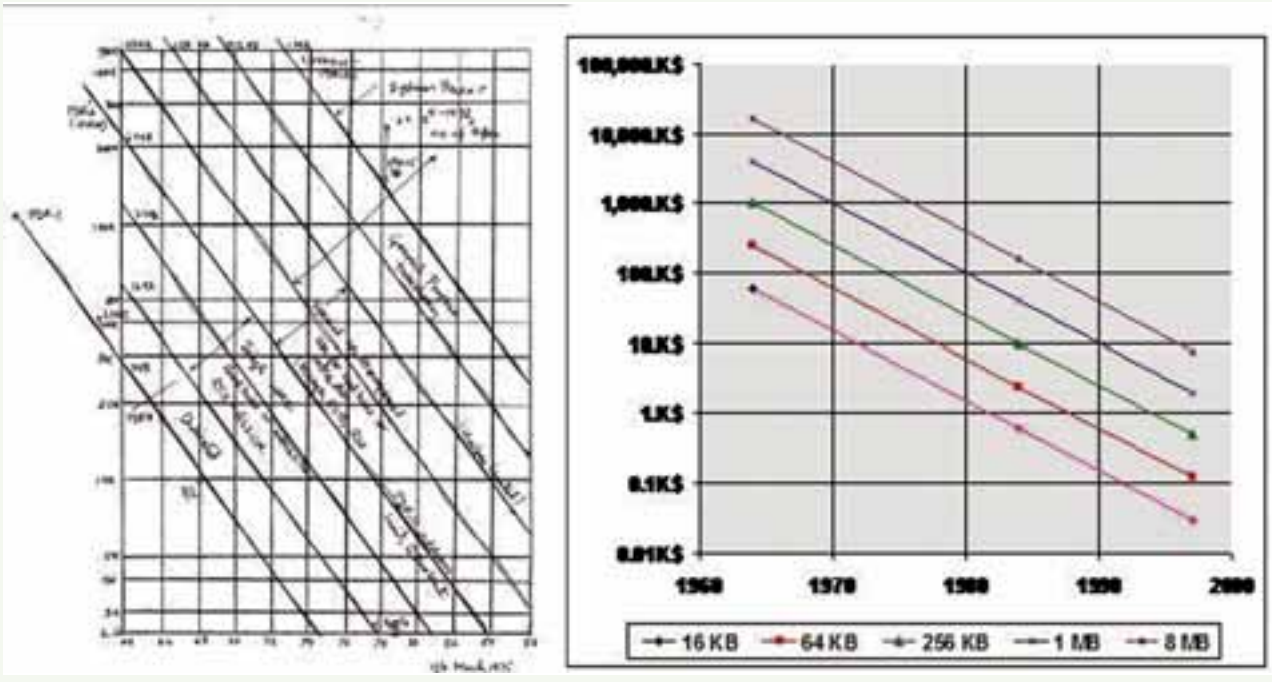

Figure 7. Original VAX Planing model Computer Prices versus time from 1975 showing different memory sizes and resulting prices 1964-1986. In 1998, the model was reviewed retrospecively. The price changes, though accurate, were so rapid to be unbelievable and hardly actionable.

The Challenge of Constant Price, 10-100 Billion Transistors per Chip, Multi-threaded, Multi-processors, for General Purpose Computing

The future is not at all clear how such large, leading edge chips will be used in general purpose computers as used at the desk top. As ever, the resilient and creative supercomputing and large scale service center communities will exploit the largest multi-core, multi-threaded chips. There seems to be no upper bound these systems can utilize!

However, without high volume manufacturing, the virtuous cycle is stopped -- in order to get the cost and benefit for clusters, a high volume personal computer market must drive demand to reduce cost. In 2007, the degree of parallelism for personal computing in non-gamer desktop systems such as Linux and Vista is nil either reflecting the impossibility of the task or our lack of creativity.

Several approaches for very large transistor count i.e. 10 billion transistor chips with more than a few (e.g. 2-10) processors could be, in order of difficulty:

1. Small chips with only as many processors that can be gainfully employed e.g. 2-4 processors system with primary memory on a chip for substantially reduced lower priced systems and greater demands that either require or imply proportionally lower cost software
2. Graphics processing, currently handled by specialized chips is perhaps the only well-defined application that is clearly able to exploit or absorb unlimited parallelism in a scalable fashion for the most expensive PCs e.g. gaming, graphical design. In effect, this just cost reduces the system by eliminating graphics chips.
3. Dedicated functional processing for networking, improved user interface including speech processing for text to speech and spoken commands
4. Multi-core and multi-threaded processor evolution for large, high performance scientific systems that are carefully programmed using FORTRAN-MPI, as FORTRAN turns 50.Remodel the desktop architectures at the language level to be able to highly parallelize apps using the vectorization and parallelization that has proven applicability in the multi-vector processor machines, betting on the need
5. Develop image processing enabling "computers to see" and be controlled by motion and emotion using hands and face. The Nintendo Wii seems to have something here.
6. A BKA or "BIG KILLER APP" that exploits these structures, EVERYONE needs, and compatible with our PC environment.
7. Something BIG, based on a dramatic new way to program e.g. Transactional Memories, Functional Programming, block structured dataflow requiring changes in language, tools, training, and new applications. Systems are being introduced such as Microsoft's F# to test this approach, and if successful imply a change akin to the introduction of objects. Software objects, requiring new application architectures may be alternative way of thinking versus the FORTRAN-MPI model.
8. Abandoning general purposeness using FPGAs that are programmed using inherently parallel hardware design languages like parallel C or Verilog that could provide universality that we have never before seen, and

Independent of how the chips are programmed, the biggest question is whether the high volume per-

sonal computer market can exploit anything other than the first three paths, and even those require careful programming beyond 2007 operating systems.

Let's apply the Carver Mead 11 year rule – the time from discovery and demonstration till use. Perhaps the introduction of a few transactional memory systems have started the clock using a programming methodology that claims to be more easily understood. A simpler methodology that can yield reliable designs by more programmers is essential in order to utilize these multiprocessor chips.

In a way, the opportunity or rather need for parallelism is reminiscent of the 1982 Japanese Fifth Generation research effort based on parallelization, AI, and PROLOG. (The Denelcor HEP was also installed then.) This time, it's not research. The problem needs a tractable solution. Without it, Moore's Law slows.

Will Small Form Factor Devices Impact Personal Computing?

Users are likely to switch classes when the performance and functionality of a lesser priced class is able to satisfy their needs and still increase functionality. Since the majority of PC use is for communication and web access, evolving a small form factor device as a single communicator for voice, email, and web access is quite natural. Two things will happen to accelerate the development of the class: people who have never used or are without PCs will use the smaller, simpler devices and avoid the PC's complexity; and existing PC users will adopt them for simplicity, mobility, and functionality e.g. wallet for cash, GPS, single device. We clearly see these small personal devices with annual volumes of several hundred million units becoming the single universal device evolving from the phone, PDA, camera, personal audio/video device, web browser, GPS and map, wallet, personal identification, and surrogate memory.

With every TV, becoming a computer display, a coupled SFF becomes the personal computer for the remaining applications requiring large screens. Cable companies will also provide access via this channel as TV is delivered digitally.

Ubiquitous Wireless. WiFi, Cellular Services, and Wireless Sensor Nets

Unwiring the connection around the computer and peripherals, TV set, etc. by high speed radio links is useful but the app is unwiring, and not platform creation. Near Field Communication (NFC) using RF or magnetic coupling offers a new interface that can be used to communicate a person's identity that could form a new class for wallets and identity. However, most likely the communication channel and biometric technology taken together just increase the functionality of small devices.

Wireless Sensor Nets: New Platform, Network, and Applications

Ubiquity: combining the platform, *wireless* network and interface into one to integrate with other systems by sensing and effecting is clearly a new class that has been forming since 2002 with a number of new companies that are offering – "un wiring", and hence reduced cost for existing apps e.g. process, building, home automation and control. Standards surrounding the 802.15.4 link that competes in the existing unlicensed RF bands with 802.11xyz, Bluetooth, and phone are being established.

New applications will be needed for wireless sensor nets to become a true class versus just unwiring the world. If, for example, these chips become part of everything that needs to communicate in the whole IT hierarchy, a class will be established. They carry out three functions when part of a fixed environment or a moving object: sense/effect; recording of the state of a person or object (things such as scales, appliances, switches, thermometers and thermostats) including its location and physical characteristics; and communication to the WiFi or other special infrastructure network for reporting. RFID is part of this potentially very large class of trillions. Just as "billions of clients needed millions of servers" a trillion dust wireless sensing devices will be coupled to a billion other computers.

Summary

Bell's Law explains the history of the computing industry based on the properties of computer classes and their determinants. The paper posits a general theory for the creation, evolution, and death of various priced-based computer classes that have come about through circuit and semiconductor technology evolution from 1951. The exponential transistor density increases forecast by Moore's Law (1965,1975) being the principle basis for the rise, dominance, and death of computer classes after the 1971 microprocessor introduction. Classes evolve along three paths: constant price and increasing performance of an established class; supercomputers – a race to build the largest computer of the day; and novel, lower priced "minimal computers". A class can be subsumed by a more rapidly evolving, powerful, less expensive class given an interface and functionality. In 2010, the powerful microprocessor will be the basis for nearly all classes from personal computers and servers costing a few thousand dollars to scalable servers costing a few hundred million dollars. Coming rapidly are billions of cell phones for personal computing and the tens of billions of wireless sensor nets to unwire and interconnect everything. In 1951, a man could walk inside a computer and by 2010 a computer cluster with millions of processors has expanded to building size. More importantly, computers are beginning to "walk" inside of us[2].

Acknowledgements

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About the Author

Gordon Bell has been a principal researcher at Microsoft Research, since 1995, researching the lifetime capture and storage of everything for an individual. Previous roles include VP of R&D, Digital Equipment Corp. (1960-1983); professor, Carnegie-Mellon University (1966-72); founding assistant director of NSF's Computing and Information Sciences and Engineering (CISE) Directorate (1986-1988); chairman, cross agency committee (FCCSET) for creating the Internet(1987-1988); advisor /investor in 100+ start-up companies; and a founding trustee of the Computer History Museum, Mountain View, CA.

Since 1987 he has sponsored the Association for Computing Machinery's (ACM) Gordon Bell Prizes for parallelism awarded annually at Supercomputing. He has bachelor and master of science degrees from MIT (1956-57), is a University of New South Wales Fulbright Scholar (1957-58), has an honorary doctorate in Engineering from Worchester Polytechnic Institute (WPI) (1993), and is a fellow of the American Academy of Arts and Sciences (AMACAD), Assoc. for Computing Machinery (ACM), the Institute of Electrical and Electronics Engineers (IEEE), and the National Academies of Engineering (NAE) and Science (NAS). Awards include: ACM-IEEE Eckert-Mauchly Award; the IEEE's Computer Pioneer and McDowell Awards; the IEEE's Von Neumann Medal; the Computer History Museum Fellow Awards; the American Electronics Association (AEA) Inventor Award for the economic contribution to New England; the IEEE 2001 Karapetoff Eminent Member's Award of Eta Kappa Nu; and the 1991 National Medal of Technology "for his continuing intellectual and industrial achievements in the field of computer design and for his leading role in establishing…computers that serve as a significant tool for engineering, science, and industry."

Advances in Ultra-Low-Voltage Design

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Ultra-Low-Power Electronics and Sub-threshold Operation

In the near future, a number of systems will be powered using energy scavenging technologies, enabling exciting new applications such as medical monitoring, toxic gas sensors and next-generation portable video gadgets. Energy harvesters typically provide output power in the range of 10 – 100μW, setting a constraint on the average power that can be consumed by the load circuitry for self-powered operation. This will require the electronic circuits to operate with utmost energy efficiency while performing the required functionality. Energy minimization requires a system-level approach optimizing not only the signal processing and interface circuits but also the energy processing function. A major opportunity to reduce the energy consumption of digital circuits is to scale supply voltages below 0.5V driving them to sub-threshold operation.

The idea of exploiting weak-inversion operation for low power circuits was pioneered by Dr. Eric Vittoz in the 1960's and some history associated with the development of these circuits is featured in the Summer 2008 issue. Weak-inversion circuits as proposed by Dr. Vittoz [1] have had a major impact on the design of micro-power integrated circuits and systems. This includes not only wristwatch circuits and calculators, but also a number of mixed-signal applications such medical electronics and sensors. The special MOS models developed by Dr. Vittoz and his colleagues were crucial for ultra-low-voltage operation and weak inversion analog circuits. The early work was later extended to the well-known EKV model [2] specifically designed for low-voltage and low-current analog circuit analysis. Based on this model, Dr. Vittoz developed expressions for static and dynamic behavior of sub-threshold logic in [3]. Another critical early development was the work of Swanson and Meindl [4], which derived the minimum supply voltage at which CMOS digital circuits can function, and demonstrated inverter VTC down to 0.2V.

Today, sub-threshold operation provides a compelling solution for a number of emerging energy-constrained systems implemented in scaled CMOS technologies. This article outlines some of the recent advances and challenges associated with sub-threshold circuit design. This includes the design of new logic and memory circuits, support circuitry (e.g., DC-DC converters) and the use of redundancy.

Minimum Energy Digital Logic

The concept of aggressive V_{DD} scaling has been explored to minimize energy dissipation. An important question involves finding the optimal V_{DD} and threshold voltage (V_t) which minimize the energy consumed by a digital circuit. To this end, authors in [5] examined energy and performance contours of a characterization circuit as V_{DD} and V_t are varied. The contours showed the existence of an optimum V_{DD} and V_t which minimizes energy. Importantly, the optimum V_{DD} does not necessarily occur at the lowest voltage at which the circuit functions. For circuits that require higher performance than is possible at the minimum energy point, the contours give the (V_{DD}, V_t) which lead to the lowest energy consumption at the required performance. Effects of varying the circuit activity factor and temperature were also investigated.

For a system where V_t is fixed (i.e. no body biasing), Figure 1 shows how energy varies with V_{DD} scaling, using a 65nm ALU as an example. As V_{DD} decreases from 1.2V, the energy per clock cycle first reduces, then reaches a minimum at around 0.3V, and finally increases again. This trend occurs because of a trade-off between the active switching and leakage components of energy. At high supply voltages, active switching energy ($E_{ACT} = CV_{DD}^2$) dominates. Therefore, as V_{DD} decreases, the circuit energy is reduced quadratically, as shown in Figure 1 for $V_{DD} > 0.5V$.

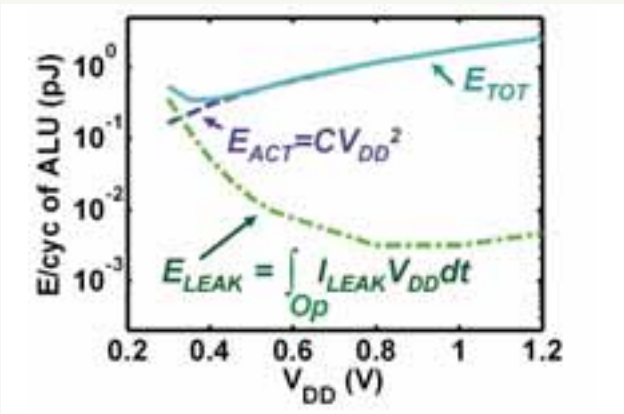

Figure 1: Energy versus V_{DD} curve of 65nm ALU, showing trends in active, leakage, and total energy.

However, as V_{DD} is lowered to sub-threshold levels the propagation delay increases exponentially, since device currents depend exponentially on both V_{DD} and V_t in weak inversion. Now, the leakage energy per clock cycle (E_{LEAK}), which equals the leakage power integrated over one clock period, also goes up exponentially and eventually dominates the total energy. This is seen in Figure 1 for $V_{DD} < 0.3V$.

$$E_{LEAK} = \int_{OP} I_{LEAK} V_{DD} dt$$

These two opposing trends imply that the total energy ($E_{TOT} = E_{ACT} + E_{LEAK}$) reaches a minimum

point. The V_{DD} which minimizes energy (minimum energy point, or MEP) depends on the relative contributions of active and leakage energy components [5], [6], [7]. If a circuit has high activity factor (i.e. a large portion of the circuit switches in any given cycle) and relatively large proportion of E_{ACT}, then the decreasing trend in E_{ACT} dominates until V_{DD} becomes very small. In this case, the MEP occurs at a low supply voltage. Conversely, if a circuit has low activity factor or a relatively large E_{LEAK} component, then the MEP occurs at a higher voltage. For most systems, the MEP occurs in or near the sub-threshold region, since E_{LEAK} begins to increase rapidly when V_{DD} decreases and approaches V_t.

Process technology scaling provides smaller switching capacitance. However, leakage current in recent technology generations have increased substantially, in part due to decreasing threshold voltages to maintain performance while the nominal supply voltage is scaled down. Figure 2 examines the net effect of these trends on the energy of a 32-bit adder simulated with predictive models [8] and interconnect parasitics. The W/L of devices in the adder is kept constant as the lengths are scaled to the 65nm, 32nm, and 22nm nodes. At nominal V_{DD} (0.8V-1V), the reduction in active energy with process scaling is apparent. Importantly, the MEP occurs at a higher voltage at the deeply scaled nodes, due to the larger relative contribution of leakage energy. Nevertheless, for this particular circuit, the MEP still occurs in the sub-threshold region.

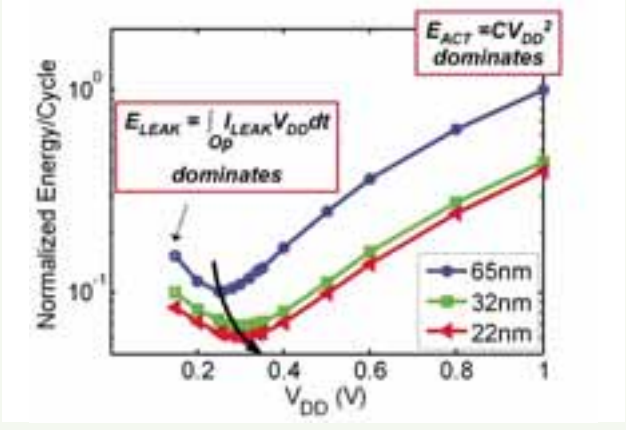

Figure 2: Trend in minimum energy point of 32b adder with technology scaling using predictive models [8].

Challenges in the Ultra-Low-Voltage Regime

Reduced I_{ON}/I_{OFF}

We have seen that aggressive voltage scaling affords significant energy benefits. However, ultra-low-voltage design must address two key challenges which impact circuit functionality. In sub-threshold, drive current of the *on* devices (I_{ON}) is several orders of magnitude lower than in strong inversion. Correspondingly, the ratio of active to idle leakage currents (I_{ON}/I_{OFF}) is much reduced. In digital logic, this implies that the idle leakage in the *off* devices counteract the *on* devices, such that the *on* devices may not pull the output of a logic gate fully to V_{DD} or ground. This is especially apparent in circuits where many parallel leaking devices fight one or several active devices in series, for example in the tiny XOR gate [9] or in register files [10]. To address this, [10] derived analytical models for the output voltages and input requirements of such circuits, as well as their minimum operating voltage.

Process Variation

Process variation can further skew the relative strengths of devices to adversely affect the functionality of logic gates. Global variation affects all devices on a chip equally and causes device characteristics to vary from one chip to the next. In sub-threshold logic, its main effect is seen at skewed P/N corners with strong PMOS and weak NMOS, or vice versa [9]. In deeply scaled technology nodes, local variation, which affects devices on the same chip differently, has become a significant concern. In sub-threshold, the dominant source of local variation is random dopant fluctuation (RDF) [11], in which placement and number of dopant atoms in the device channel cause random shifts in V_t. Correspondingly, both I_{ON} and I_{OFF} in sub-threshold are exponentially affected by these V_t shifts. In 65nm, for example, a $\pm 4\sigma$ V_t shift from RDF can cause the drain current to change by three orders of magnitude.

The compound effects of reduced I_{ON}/I_{OFF} and process variation are illustrated by the voltage transfer curve (VTC) of a two-input NAND in Figure 3. At the strong-PMOS weak-NMOS global corner, the VTC is shifted towards the right. Additionally, local variation causes random perturbations in the VTC, in some cases significantly degrading the output logic levels. This implies that even the static CMOS logic style does not provide guaranteed functionality. To design robust sub-threshold circuits, it is no longer sufficient to consider only the nominal case or the global corners; we should also account for the statistical effects of local variation.

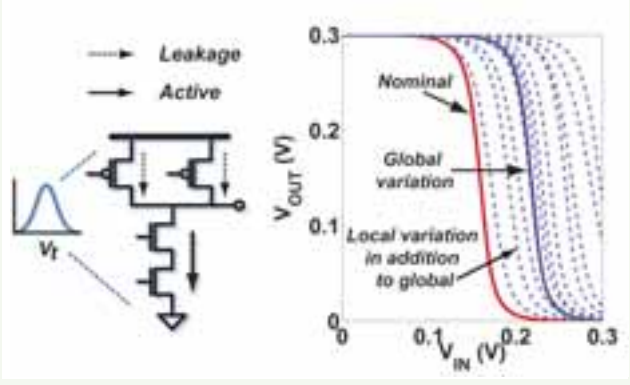

Figure 3: Impact of global and local variation on NAND gate VTC.

In addition to affecting functionality, process variation increases uncertainty in circuit delays. At low voltages, increased sensitivity to local variation causes the delay distribution to widen. Figure 4(a) shows the

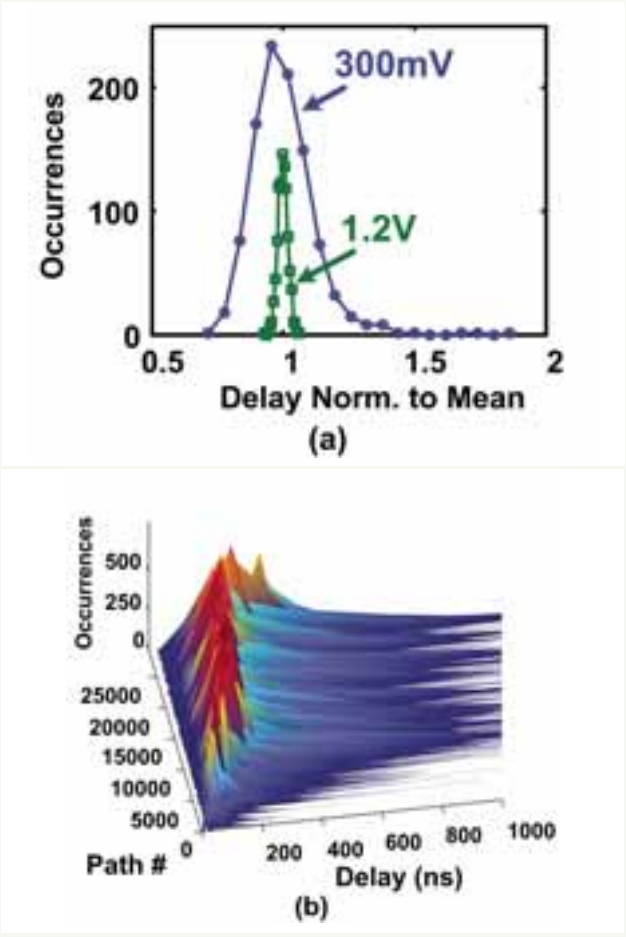

Figure 4: (a) Delay distribution of timing path at 1.2V and 0.3V under local variation. Both histograms contain 1k samples. (b) Delay distributions of 30k microcontroller timing paths [12] at 0.3V, fast global corner. Each horizontal cross-section represents distribution of one path.

delay distribution of a 65nm logic timing path at 0.3V (sub-threshold) and 1.2V (nominal). To compare the dispersion around the mean, both distributions are normalized to their sample means, highlighting the order-of-magnitude larger variability at 0.3V. This is similarly illustrated in Figure 4(b), by the comprehensive simulation of 30000 timing paths in a 0.3V microcontroller under local variation [12]. Each horizontal cross section represents the delay distribution of one timing path. Note that adjacent paths with similar means can exhibit substantially different variances, as reflected by the lengths of the distribution tails.

Conventionally, methodologies to verify setup/hold time constraints in a logic circuit treat logic gate delays as deterministic, taking points at the tails of the delay distribution to represent the maximum and minimum delays under process variation. However, very few gates exhibit delays found at the tails and most of the gates lie in the middle of the distribution. Consequently, conventional approaches give unrealistic results when applied to sub-threshold circuits. As with logic gate design, statistical methodologies such as those described in [13] are necessary for robust ultra-low-voltage operation.

SRAM Design

SRAMs typically form a dominant portion of the area and power of a system. Therefore, energy and leakage power reduction through low-voltage operation is highly desirable. However, the traditional 6-transistor (6T) SRAM cell relies on ratioed device sizing to set the relative device strengths required for reading and writing. Since sizing changes current linearly while V_t variation has an exponential impact in sub-threshold, variation can easily overwhelm the effect of sizing to cause bit-cell failures.

Data retention in a 6T SRAM bit-cell is determined by the cross-coupled inverters M1-M4 shown in Figure 5(a). By superimposing VTC of one inverter on the inverse VTC of the other, we form a butterfly plot which can be used to determine if a bit-cell is bi-stable (i.e. if it can hold data). The presence of two bi-stable intersection points in the butterfly plot indicates that the bit-cell can support "0" and "1" logic levels, and thus proper data retention. The static noise margin (SNM) indicates the maximum amount of noise that can be applied to the storage nodes of the bit-cell before the state of the cell is destroyed. The SNM is measured as the edge length of the smaller of the two

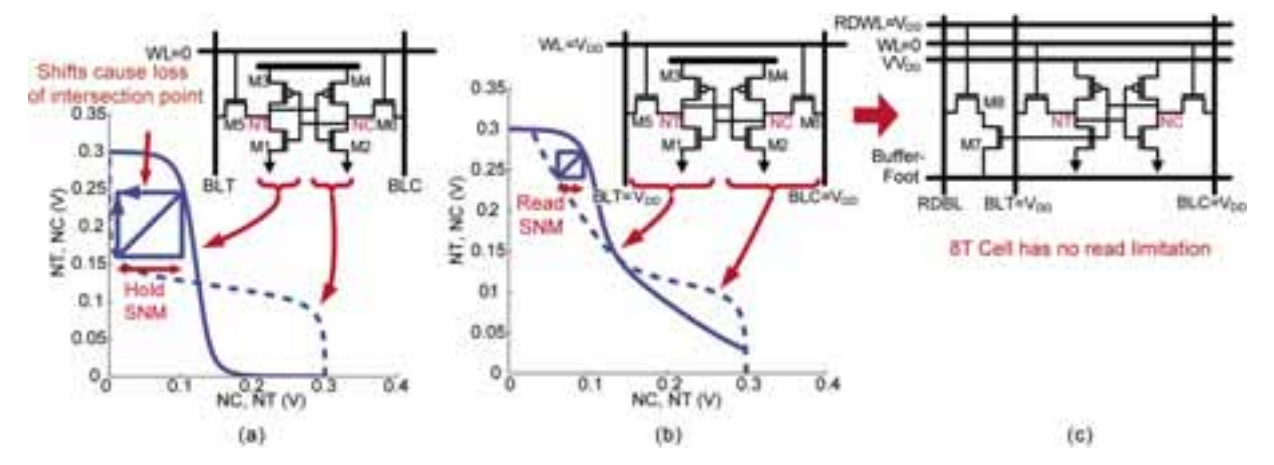

Figure 5: (a) Hold SNM and (b) read SNM of 6T SRAM cell. (c) 8T cell with two-transistor read buffer. (Courtesy of N. Verma)

inscribed square in the butterfly plot [14]. If variation causes both VTCs to be shifted by more than this amount, the butterfly plot would no longer have bi-stable intersection points, indicating failure of the bit-cell to hold a required data state.

In the 6T cell, the read operation is performed by precharging the bit-lines (BLC/BLT in Figure 5(b)) and then asserting the word line (WL) to turn on the access transistors M5 and M6. The storage node which stores a "0", for instance NT, causes the bit-line BLT to discharge. However, since the bit-line is initially precharged, M5 tends to pull NT high while M1 attempts to pull it low. The fight between M1 and M5 raises the voltage at NT. Accordingly, the butterfly plot for a 6T cell during read is squashed on one end, as illustrated in Figure 5(b).

As V_{DD} is decreased, both read and hold SNM correspondingly become smaller. Further, process variation can shift the VTCs in the butterfly plot to cause bit-cell instability. As is apparent from Figure 5, the read SNM is considerably smaller than hold SNM, and thus limits low-voltage operation.

An alternative 8T bit-cell avoids the read SNM limitation with the use of a two-transistor read buffer. Shown in Figure 5(c), this read buffer M7-M8 isolates the internal storage node from the read bitline (RDBL) so that it is not disturbed during a read. Since data retention in the 8T cell now depends on the larger hold SNM, V_{DD} can be lowered further down to sub-threshold. This bit-cell, along with other peripheral circuitry to assist sub-threshold writing and to improve bit-line integration, was demonstrated in a 65nm, 256kb SRAM functional down to 350mV [15].

Redundancy is another powerful technique for managing variation in ultra-low-voltage systems. In designing SRAM sense amplifiers, we are faced with a trade-off between their statistical offset and area. The offsets of sense amplifiers exhibit a distribution due to process variation, whose standard deviation relates inversely to the areas of the input devices. However, instead of upsizing the input devices to reduce offset, consider putting N redundant sense amplifiers within the same area as one full-size circuit, and then selecting the one with the smallest offset. Although each copy has smaller devices and thus larger individual probability of error (defined as |offset| > 25mV in Figure 6), the error probability in the sensing network is now the chance that all N sense amplifiers fail. Therefore, $P_{ERR,\ total} = (P_{ERR,\ N})^N$, *where* $P_{ERR,\ N}$ is the error probability of one of the N redundant sense amplifiers. As shown in Figure 6, even a small amount of redundancy (N=2) significantly improves the error probability [15].

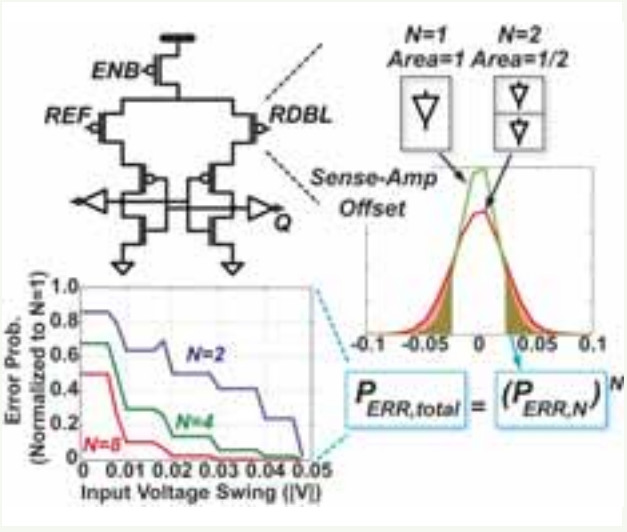

Figure 6: Redundancy significantly reduces overall error probability in SRAM sensing network [15].

Tracking Circuits and DC-DC Converters

Minimum Energy Tracking Loop

Powering sub-threshold memory and logic circuits requires energy delivery circuitry that can efficiently convert a battery supply to sub-threshold voltages at microwatt load power levels. Moreover, since the minimum energy point (MEP) of a circuit changes with workload, temperature, and other environmental conditions, the ability to track the MEP is crucial to maximize energy savings. Figure 7 shows the architecture of such a tracking loop [16] which automatically adjusts its output voltage to the minimum energy point of the load circuit. The energy sensor circuit and the energy minimization algorithm set the reference voltage (V_{ref}) of the DC-DC converter. The DC-DC converter, in turn, will adjust its output (V_{DD}) to match V_{ref}, thereby enabling the load circuit to operate at its MEP.

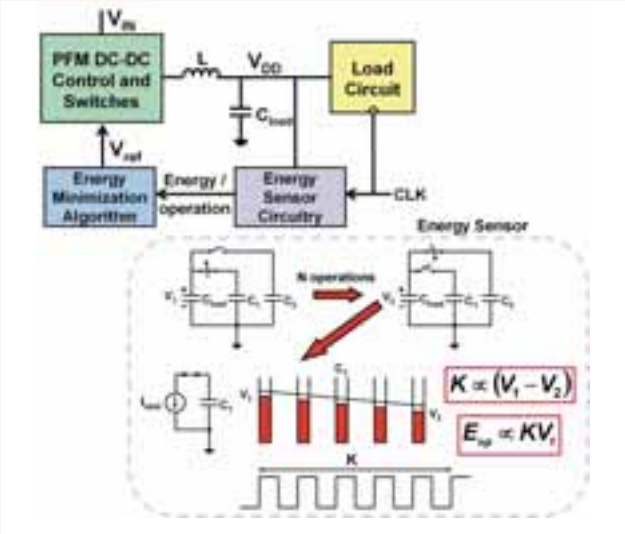

Figure 7: Architecture of minimum energy tracking loop and energy sensor circuitry [16].

The energy sensor circuitry senses the energy per clock cycle consumed by the load circuit in a digital manner. By avoiding high-gain amplifiers and analog blocks, this scheme significantly reduces the overhead power. As illustrated in Figure 7, the voltage on the storage capacitor C_{load} is first stored on C_1. During energy sensing, the DC-DC converter is disabled. Therefore, voltage on C_{load} droops to V_2 after N operations of the load circuit, and is subsequently stored

on C_2. The energy per operation of the load circuit is given by $E_{op} = C_{load}(V_1^2-V_2^2)/2N$. Further, if V_2 is sufficiently close to V_1, $(V_1 + V_2) \approx 2V_1$, and hence E_{op} is approximately proportional to $V_1 (V_1 - V_2)$. V_1 is the reference voltage to the DC-DC converter and is known digitally. (V_1-V_2) can also be found digitally by discharging C_1 using a current sink while a fixed frequency clock drives a counter. The fixed frequency clock, together with the constant current sink that drains C_1, quantizes voltage into time steps. The number of fixed frequency clock cycles required for C_1 to droop down to V_2 is directly proportional to (V_1-V_2). From this, the digital representation of E_{op} is calculated and is then used by a slope descent algorithm to arrive at the MEP.

Since the MEP usually lies in sub-V_t where load power demands are very low, the DC-DC converter in the MEP tracking loop is designed to supply low voltages (0.25V-0.7V) at microwatt power levels. The converter employs a synchronous rectifier buck converter design with external passives. The all-digital control circuitry is optimized for minimal power overhead, enabling the DC-DC converter to achieve >80% efficiency down to 1µW load power levels.

Switched Capacitor DC-DC Converter

Minimizing the number of external components is highly desirable in embedded applications such as biomedical implants. For micro-power applications, a switched capacitor DC-DC converter design is attractive since the power conversion circuitry can be completely integrated on-chip. Figure 8 shows a switched capacitor converter [17] which can provide *variable* supply voltages and achieve >70% efficiency while supplying from 1µW up to 1mW load power. The converter uses an all-digital pulse frequency modulation (PFM) mode of control to regulate the output voltage. In this type of control, the converter stays idle until the load voltage V_L falls below the reference voltage (V_{REF}), at which point a clocked comparator enables the switch matrix to transfer one charge packet to the load. The PFM mode of control is essential to achieving high efficiency while providing extremely low power levels to the load circuits.

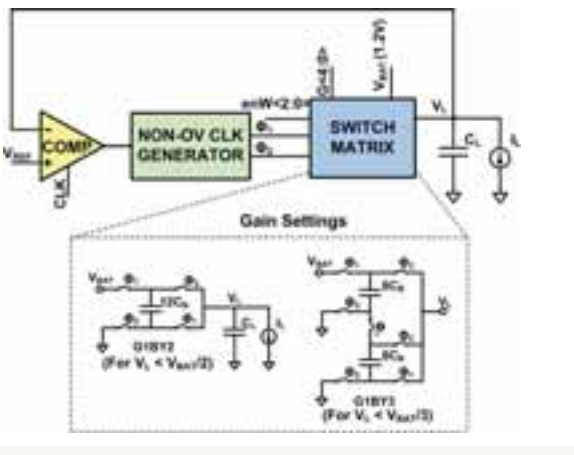

Figure 8: Switched capacitor DC-DC converter architecture [17], [12].

The switch matrix partially shown in the inset of Figure 8 contains the charge transfer switches and the charge transfer capacitors. Importantly, the total charge transfer capacitance can be arranged in five different gain settings to help minimize linear conduction loss, which is a major efficiency-limiting mechanism in switched capacitor converters [17]. Generally the maximum efficiency is limited by the ratio of the voltage supplied to the load circuit (V_L) to the output voltage of the converter with no load ($V_{no-load}$). Accordingly, the converter contains multiple gain settings to provide different levels of $V_{no-load}$. When we wish to supply very low V_L (e.g. 0.3V to a sub-V_t SRAM), we can choose the suitable gain setting with a small $V_{no-load}$ to maximize the achievable efficiency. The two gain settings shown in Figure 8, for instance, are suitable for supplying $V_L < V_{BAT}/2$ and $V_L < V_{BAT}/3$.

Demonstration Systems

Emerging micro-power applications have generated much interest in sub-threshold circuits. In the past few years, researchers have demonstrated a variety of systems functioning at very low voltages. For example, a sub-threshold DLMS filter was designed for a hearing-aid application, and an 8x8 carry save array multiplier test-chip was fabricated in 0.35µm [18]. This test-chip published in 2003 explored adaptive body biasing and operated down to 0.3V. In 2004, an 180mV FFT processor in 0.18µm was demonstrated in [9]. The processor, pictured in Figure 9, featured an energy-aware scalable architecture supporting variable bit precision and FFT length. Device sizing strategies for logic gates accounted for global process variation, and the register file design employed a multiplexer-based hierarchical-read-bitline scheme to address weak I_{ON}/I_{OFF}. Combining the energy benefits of sub-V_t operation with Dynamic Voltage Scaling (DVS), [19] presented an Ultra-Dynamic Voltage Scaling test-chip with a 32b Kogge-Stone adder in 90nm. In this technique, we can operate the circuit at its MEP during periods of very little activity, and dynamically raise V_{DD} when short bursts of high performance are needed. The test-chip showed 6800X performance scaling as V_{DD} is varied from the MEP of 330mV to 1.1V, and provided 9X energy savings over single-V_{DD} operation.

Systems with constant throughput constraints can also benefit from substantial V_{DD} reduction by leveraging extreme parallelism to compensate for speed decrease. For example, a 400mV baseband radio processor [20] was able to support 500M samples/s throughput by distributing computations to many parallel hardware blocks.

A 200mV, 0.13µm sub-threshold sensor processor was demonstrated in [21] and features an 8b ALU, 32b accumulator, and 2kb SRAM. The standard cell library to implement the processor was carefully selected to exclude cells with a fan-in more than 2 as well as pass-transistor logic. Another sub-200mV processor in 0.13µm examined the effectiveness of body biasing in

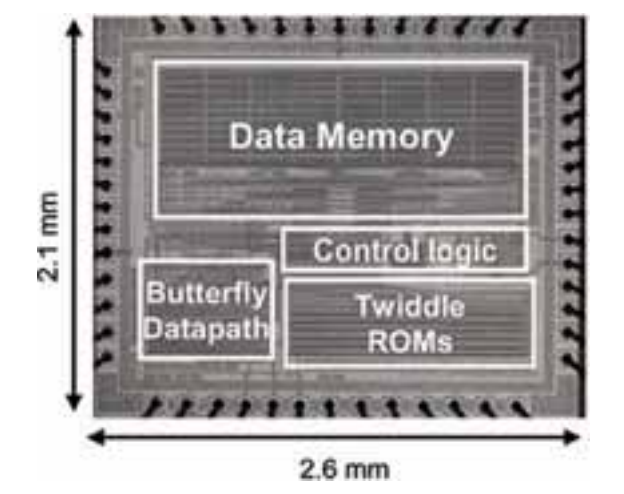

Figure 9: Die micrograph of 180mV FFT Processor [9].

mitigating variation and several logic gate sizing strategies for performance tuning [22].

Looking forward, technology scaling enables reduced CV_{DD}^2 energy and increased density, but presents heightened process variation. Most recently in 2008, a 320mV 411GOPS/Watt motion estimation accelerator in 65nm [23] employed optimized datapath circuits to address variation and weak I_{ON}/I_{OFF}, as well as to improve performance. [12] presented a 65nm system-on-a-chip which features a 16b microcontroller, a 128kb 8T SRAM, and an on-chip switched capacitor DC-DC converter (Figure 10). The system demonstrated approaches for library design and timing analysis, as well as circuit techniques to enable sub-threshold operation down to 300mV.

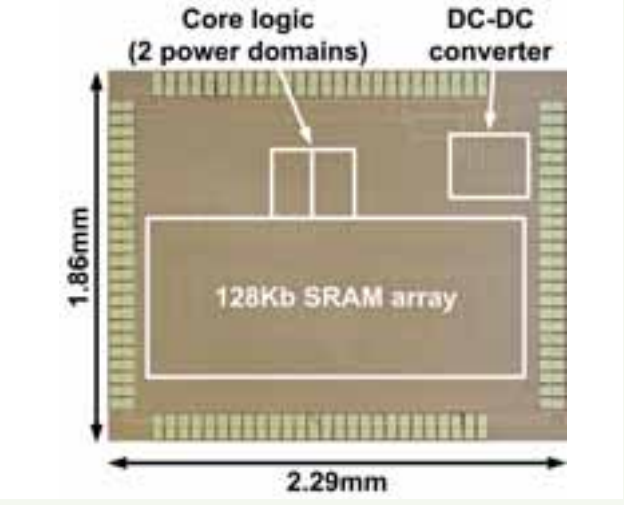

Figure 10: Die micrograph of 65nm sub-V_t microcontroller [12].

In the mixed-signal domain, an ADC functioning down to 200mV has been demonstrated in [24]. This highly digital 6b flash ADC removes the need for a resistor string reference voltage ladder by building voltage offsets directly into each dynamic, regenerative comparator through sizing. As comparator and reference voltage offset compensation is difficult in the analog domain at voltages below 500mV, comparator redundancy and reconfigurability are employed to tolerate large comparator offsets (> 1 LSB) and improve linearity.

Current mode logic in weak inversion was presented in [25]. To operate at low bias currents, a novel PMOS load device was proposed to provide high resistance and large voltage swing.

Published work on sub-threshold SRAMs has explored a range of bit-cell and peripheral circuit designs. The survey here is organized according to process technology. At the 0.13µm node, authors of [26] demonstrated a 512x13b SRAM with a register-file-based cell, a multiplexed read scheme, and self-timed keepers to achieve functionality at 216mV. The 0.2V, 480kb SRAM [27] used a 10T bit-cell designed to eliminate data-dependent bit-line leakage. Access devices are lengthened to take advantage of reverse short channel effects and improve sub-V_t writability. A virtual ground replica shifts the trip point of the inverter-based sensing circuit to improve sensing margin. [28] explored use of a 6T cell modified for single-ended read and improved readability. This came at the cost of reduced writability, which was recovered by allowing the bit-cells' virtual V_{DD} and ground rails to droop during a write. The 2kb SRAM array was fully functional from 1.2V to 193mV.

At the 65nm node, local variation becomes more prominent. A 256kb SRAM [29] employed a 10T bit-cell to eliminate the read SNM limitation as mentioned in the SRAM section. Stacked devices in the read-buffer reduced bit-line leakage and improved bit-line integration, while floating the cell supply voltage assisted sub-V_t writes. The SRAM was able to fully read and write at below 0.4V. The 8T design described previously [15] featured peripheral assist circuitry to enable functionality in sub-V_t. During a write, the cell supply voltage is reduced by a write driver, to ensure that PMOS devices are weakened relative to access devices. During a read, the feet of all unaccessed read buffers are pulled to V_{DD}, eliminating their sub-V_t leakage currents which would otherwise degrade the read bitline voltage.

Next Steps

Significant advances have been made in the recent year related to sub-threshold circuit design. Important issues such as device variability have been addressed through circuit design and system architecture. To transition these concepts to products, it will be critical to develop design methodologies and CAD tools to encapsulate variation-aware methodology (e.g., statistical timing tools compatible with low-voltage design). A number of exciting new applications can leverage ultra-low-voltage operation to dramatically reduce energy consumption. This includes sensor networks, medical electronics and multimedia devices.

Acknowledgements

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Gigasensors for an Attoscope: Catching Quanta in CMOS

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Silicon Takes the Stage in Particle Physics Experiments

The gigantic experiments at CERN, the elementary particle accelerator laboratory in Geneva, Switzerland rely on custom-designed CMOS for much of their functioning. Close to a million CMOS chips, silicon-based sensors and other sensitive material, such as scintillating crystals or liquid argon, fill the space in and around a superconducting magnet, the size of a 6-stories building. The chips have to process small electrical signals, typically 10 to 20 thousand electrons, generated by the ionizing particles in the sensor elements. Silicon is sensitive to light, but very thick diode structures also deliver signals that are proportional to the energy loss of swift particles that pass through. The sensor cells have been connected in a fully parallel approach to their integrated readout amplifiers and further signal processing, because the 'snapshots' of the successive interactions are uncorrelated, and take place every 25 ns: 40 million pictures per second. These massively parallel detector systems with close to 10^9 sensor cells have become possible only by exploiting the miniaturization of electronics.

The CERN experiments are situated deep underground along the 27 km circular accelerator called the 'Large Hadron Collider' LHC. Figure 1 gives an idea of such a collider detector, still under construction.

Fig. 1 Part of the Atlas team assembled in between the end-caps, in the underground cave. Several thousand scientists and technicians have worked on the Atlas construction. The blue cylinder is a shielding block that surrounds the entry/exit of the not yet installed beam pipe. The magnet and the main barrel are to the left, invisible here. Photo CERN/Atlas.

The experiments study the fundamental physics processes between elementary particles at the highest momenta on earth. Particle beams circulating in opposite directions with thousands of bunches of protons are accelerated to 7 TeV, and then made to collide head-on in 4 crossing points. The experimental set-up around an interaction point consists of successive shells of different detectors in which one records all the effects in the miniature explosions that result when quarks inside these protons occasionally fuse together. Figure 2 illustrates the variety of reaction products in a rare, sought-after type of collision.

Fig. 2 Simulated interaction in the Atlas detector with all outgoing reaction products traversing the successive shells of the detector. The central region where most particles are colored red, represents the inner tracker detectors. The surrounding heavy calorimeters provoke showering around the absorbed particles. The yellow track to the right is an escaping muon. The scale of the figure is ~10m across. Photo CERN/Atlas.

Only a tiny 'needle' fraction of the 'events' represent new physics phenomena, and these have to be filtered out from the majority 'haystack' of uninteresting data. A particle or quantum with 1 TeV energy has an equivalent wavelength of one attometer (10^{-18}m), compared to a micrometer for visible light, and so one can say that these experiments in the TeV energy range act as 'attoscopes' rather than microscopes, when they look at the properties of these energetic quanta on the atto-scale.

The introduction of silicon chips in particle physics experiments went by steps, and in this article I trace some of the history of silicon detectors and readout chips for tracking detectors. These form the inner shells of the equipment. As shown in Figure 2, they record the trajectories of the ionizing particles in a

somewhat similar way as cloud chambers, spark chambers or bubble chambers did in the earlier times. Although providing fewer measurement points along a track, the main advantage of the silicon tracker systems is the fully electronic operation and the ns collection time of the signals in the silicon layers. Already in 1976 at the EPFL, the Swiss Federal Technical University in Lausanne, during a workshop 'Limits on Miniaturization' my colleague Pierre Jarron and I became enthusiastic to apply developments in microelectronics for detection of particles. As shown in the next section, segmentation is the key to the silicon trackers, and in 1980 we introduced the silicon diode 'microstrip' detector with full parallel readout, following a visit at the nuclear physics institute IKO in Amsterdam. Then the design of custom chips for silicon detector readout was started at SLAC in 1981 and at CERN in 1986. Now, 25 years later a community of designers and users supply the various integrated circuits for detection and signal processing in the experiments at CERN, at Fermilab near Chicago, at the Stanford linear accelerator SLAC, and other facilities worldwide. The most recent development with 'ultimate' segmentation for particle tracking, ~ 1995, was the true 2D silicon pixel detector, for which Eric Vittoz and his coworkers in CSEM and at the EPFL contributed significantly, with advice, designs and training.

Segmentation of Sensors, Serial or Parallel Readout

The use of a contiguous array of segmented diodes on monolithic silicon for nuclear particle detection, as far as I know, was first proposed ~1961 by Leo Koerts from Philips/IKO in Amsterdam. Their 'checker board' detector with Schottky barrier strips on the front and orthogonal ohmic strips on the rear, both with 1.2 mm pitch, was described by Hofker in 1966 [1]. This was the device that Jarron and I took as the example for our silicon diode 'microstrip' detectors, with much smaller segmentation at 200 µm [2] and later at 50 µm pitch. The readout of the checker board was not yet fully parallel, but it had single analog amplifier channels, for front and rear of the sensor, together with a series of pick-up transformers for position determination along the diode array. The full system 'BOL' with 8000 'pixels' [3], operational 1968-1974, needed several cubic meters of electronics for this readout. It is interesting to remember that around this time monolithic 2D matrix approaches for imaging of visible light also were studied at Philips and at Bell Labs. Within a few years these proposed respectively BBD [4] and CCD [5] for imaging, and both approaches used serial signal readout.

The earliest system with fully parallel readout for a sizeable array of sensing elements was the Multi-Wire Proportional Chamber (MWPC) for particle position measurement in 1968 [6] which earned Georges Charpak a Nobel prize in 1992. A separate amplifier connects to each wire and with a typical distance between wires of ~5mm, this electronics could be fabricated with the discrete components of the time. For the 'microstrip' detectors, made on kΩcm Si wafers by Schottky barriers and later by ion-implantation [7] at first also discrete components were used for readout, but the need for integrated circuits now was obvious. Several teams initiated analog design work: Hyams, Parker and Walker started at Stanford with an NMOS chip, called Microplex [8]. Their design used a switched capacitor feedback amplifier and evolved later, thanks to Kleinfelder [9], Spieler [10] and coworkers at Lawrence Berkeley Lab into a family of CMOS chips, used still now at Fermilab in the CDF and D0 Tevatron collider experiments. In Germany, a team of the Munich Heisenberg Laboratory and the Duisburg Microelectronics Institute, with Lutz and Buttler, together with Manfredi et al. at the University of Pavia, developed a 128 channel CMOS circuit with JFET frontend transistors [11]. Later this chip was called CAMEX and was used in the electron collider experiment Aleph at CERN, from 1989 to 2001. All these circuits used a front-end amplifier with switching feedback and double correlated sampling, contrary to the continuous feedback in 'Amplex' that I will discuss in the next section.

But first more on the 'ultimate' segmentation: for the planned proton collider experiments in the USA and Europe, with their large number of simultaneous particles, from the early 1980's we at CERN wanted to push towards parallel sensor cells of micrometer dimensions in a true 2D matrix, using photolithography [12]. Damerell had shown the power of 2D measurements by using CCD [13] but the serial readout restricts this method to particular situations of low repetition rate or experiments where the beam can be stopped after an interesting interaction, such as in a linear accelerator. The question was, if we could implement conventional, ns signal processing and full parallel readout on a microscopic area with reasonable power dissipation. We approached Eric Vittoz with this question in 1986. For the first Workshop on Pixel Detectors in Leuven [14] Vittoz analyzed this problem, and he summarized some parameters in Table 1. Also he sketched the signal processing chain in Figure 3, and came with positive conclusions on

Table 1
State of the problem

Total number of pixels	10^8
Pixel size	0.1×0.1 mm^2
Chip size	50 mm^2
Number of pixels per chip	5000
Number of chips in system	20000
Total system area	1 m^2
Power per chip	10–100 mW
Total power	0.2–2 kW
Power per pixel	2–20 µW
Supply voltage	3 V
Current per pixel	0.7–7 µA
used for: amplifier; 1 bit A/D converter (comparator); multiplexer	
Cycle time (periodicity of events)	100 ns (10 MHz)
Nominal signal charge	10000 electrons
Intrinsic detector capacitance	4 fF per pixel
Total detector capacitance	
minimum: multilayer by SOI	10 fF per pixel
maximum: hybrid mount (flip-chip)	1 pF per pixel

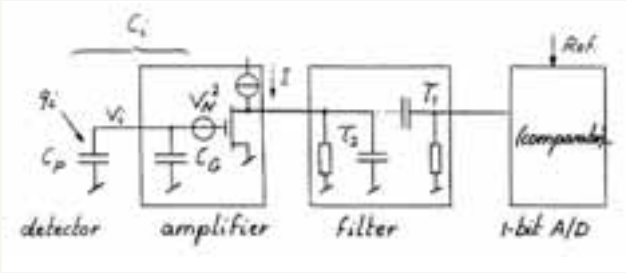

Fig. 3 Schematic by Eric Vittoz for the analog front end for an integrated pixel detector[14].

power and noise. Such small pixels pinpoint positions of the particles in space with much better precision, but also have the pleasant characteristics of low capacitance and reduced dark current.

This allows low electronic noise, and recent matrices achieve ~ 100 e- r.m.s.equivalent, at the input of the signal processing circuit, even with ~100ns signal shaping. The signal generated in the Si sensor by ionizing quanta is typically between 2000 and 20000 electron-hole pairs, so that one has a comfortable signal/noise ratio. In 1987 I dubbed these devices 'micropattern' detectors, because I imagined that eventually they would be able to recognize useful interactions from pre-defined patterns in the image. In practice the name 'pixel' detectors has now become the standard. In the English language, contrary to the French, there is an ambiguity between 'detector of patterns' and 'detector with patterns,' and the latter meaning has more recently been adopted in the field of gaseous devices.

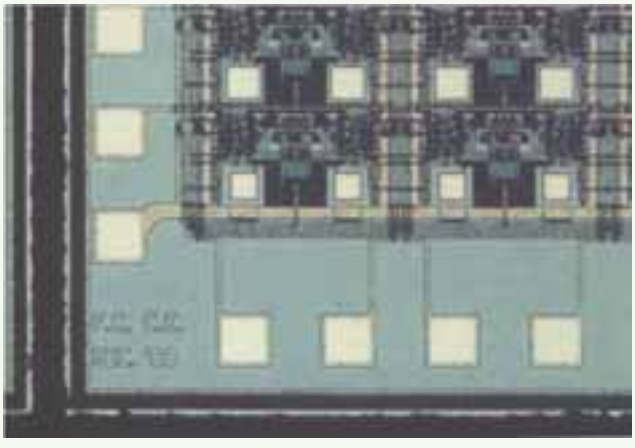

Fig. 4 Corner of the first pixel readout chip, showing 8 pixels with input contacts for bump bonding and some output pads for wirebonds. Design and layout by François Krummenacher and Christian Enz, Dec 1988. Made in SACMOS3 technology. Photo CERN.

The Earliest 'Micropattern' Pixel Detectors

In 1988, after the Workshop in Leuven, the design work started on a first prototype of a 9x12 pixel detector matrix, by Smart Silicon Systems, a startup from the EPFL, with Christian Enz and François Krummenacher as designers, Eric Vittoz as adviser and the CERN team as the critical customers and users. With a future particle collider in mind some design choices were made, such as a latched input circuit, in order to obtain low power dissipation. By Christmas the layout was ready, the chip was processed in the 3 µm SACMOS technology at Faselec AG in Zurich. With self-aligned contacts (SAC) this technology offered increased density, allowing a small pixel area of 200 µm x 200 µm. In June 1989, after dicing at CSEM we made the microphoto of Figure 4, which shows one corner of the matrix with 8 input contacts and readout cells.

Michael Campbell and I made the first measurements over the summer, and our late paper was accepted for presentation at the 1989 Nuclear Science Symposium near San Francisco. The chip worked well, with noise below 500 e- rms, detection threshold ~3000 e- and power of 30 µW/pixel, all well below the design goals. But then some strange problems beset the first publication. The Symposium was cancelled because of the 17 October San Francisco earthquake. Despairing, we submitted the paper to Nuclear Instruments and Methods [15]. The Conference eventually was rescheduled in a different, undamaged hotel where Michael Campbell presented the paper only in January 1990 for a small audience. We also found that the planned bump-bonding could not be made because of a mm wide guard ring that is needed around the active sensor area, and this would obscure the wirebond pads on the electronics readout chip.

We initiated the design for a next chip, now aiming at an asynchronous input amplifier and a large, more practical matrix of 16 columns and 63 rows. The 64th row was dedicated to a provision for dark current compensation. Each pixel of 75µmx500µm contained ~80 transistors. The chip was again manufactured in the SACMOS3 technology, and after bump-bond assembly at GEC-Marconi in Caswell, the first particle tracks were measured at CERN on 20 October 1991. These measurements were presented at the 1991 Nuclear Science Symposium in Santa Fe [16], two years after those of the first chip. In the scientific community, with relatively modest resources long iteration times are typical, also because the design teams are involved in the development and testing of the full application system. Indeed, the following, third chip in this series was the LHC1/Omega3 [17], which became available early in 1995, nearly four years later. This chip with a 16x128 matrix of cells used the SACMOS 1µm technology, which represented at the time a submicron component density in comparison with normal CMOS. The smaller pixel area of 50µmx500µm could now contain as many as 400 transistors. I wonder if we can call this a 'hyperactive' pixel, after Eric Fossum just before [18] had claimed the term 'active pixel sensor' if each pixel contains at least one transistor. It may also be worth mentioning that the Faselec/Philips SAC1 process, although developed in Zurich, in 1994 just was transferred to the Taiwan Semiconductor Manufacturing Company TSMC, with the Swiss technology specialist J. Solo making many trips between Zurich and Taipei. That technology was never actually implemented anymore at the Zurich foundry of Faselec, illustrating the

swift worldwide concentrations in microelectronics manufacturing. Only 10 years earlier, there still were several MOS factories in Switzerland, serving the local high-tech industries, described in the Summer Newsletter dedicated to Eric Vittoz.

Active Feedback Compensates Dark Current

In semiconductor diode detectors, systematically one has to cope with the dark leakage current at reverse bias and often the input is AC coupled, in order to

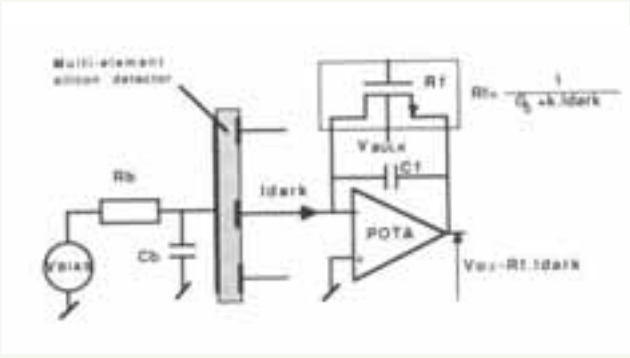

Fig. 5 Schematic diagram of the connection of segmented diode elements to an Operational Transconductance Amplifier (OTA) with a feedback that restores the operating point if there is a large current Idark at the input [19].

avoid baseline shift and amplifier saturation. For highly segmented devices, external filtering networks become impractical and these have to be implemented on the silicon sensor itself. DC interconnections would be preferable, but then a scheme is needed to accommodate varying and sometimes large currents at the inputs of the front-end amplifiers. Sometimes hundreds of nA have to be compensated, even more after extended irradiation, although the current is strongly reduced by the sensor segmentation. For the gaseous detectors this is not an issue, because the gas remains a perfect isolator, even at kV bias.

At CERN, Pierre Jarron and I started in 1986 work on CMOS chip design for the segmented Si detectors with a training course in the INVOMEC division at the just founded IMEC centre in Leuven, Belgium. Jarron followed the nuclear electronics tradition, and implemented a continuous feedback scheme using a long transistor, as shown in Figure 5 [19].

With direct connection, the sensor dark current at the input modulates the effective resistance of the feedback, so that the operational level at the output can be maintained, at the cost of a slight reduction of amplification. A current up to 450 nA per segment can be compensated. The 16-channel AMPLEX chip [20] was produced in 1987 in the 3um CMOS technology of MIETEC in Belgium. By chance this AMPLEX chip happened in 1989 to become the first integrated circuit to be actually operational in a beam collider experiment: the inner silicon array in the UA2 proton-antiproton experiment at CERN [21] was used a year before the vertex detector at the MARKII in SLAC was taking data in July 1990 [22] although the Microplex

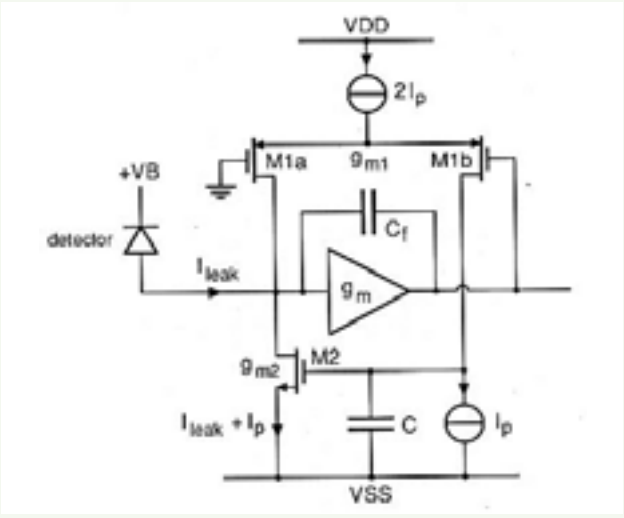

Fig. 6 Schematic diagram of the front end by Krummenacher with sinking of dark current via M2. This scheme can be implemented in each pixel [23].

chip for SLAC had been designed some years earlier. The UA2 silicon detectors had a surface area of more than 1 m^2, and this was at the time the largest silicon detector ever.

For the silicon pixel detector with their thousands of sensor cells and amplifiers, the DC coupling is the only practical possibility and a current compensation has to be implemented, on the small area available. In the Omega2 matrix Michael Campbell replicated the currents from a row of reference pixels. François Krummenacher proposed in 1990 a damped feedback illustrated in Figure 6 [23].

This can be implemented in each pixel, without the need for reference cells. The transistor M2 can sink the leakage current I_{leak}, and with proper choice of C and g_{m2} the tolerated I_{leak} can be much larger than the biasing current I_p With thousands of pixels, in practical implementations a dark current as high as 1mA per cm^2 can be handled with this approach, and current fluctuations are slowly but automatically followed pixel by pixel.

Massively Parallel 2D Gigasensor Array

The heart of three of the CERN LHC experiments is formed by several layers of true 2D pixel matrix detectors, which record at 40 MHz the positions and timing of all particles that pass through. Every single particle, representing a quantum of energy above the detection threshold of ~ 5 keV is registered by these devices. The CMOS chips that are attached to the sensor matrix not only record the signals, but store these in local memory for up to ~4 µs, until a request for readout is received. Optical links could transmit a large fraction of the data but the off-detector data processing is designed for analysis of ~kHz event rates, corresponding to expected numbers of interesting interactions. The actual sensitive area of the inner silicon pixel arrays ranges from 0.22 m^2 and 1200 chips in ALICE, to 1 m^2 with 16000 chips in CMS and 1.8 m^2 with 28000 chips in ATLAS. A much larger

Fig. 7 Final assembly work on the Atlas pixel barrel (half). One can see the modules along the ladders. The white stubs are connecting tubes for the cooling channels, one for each ladder. Photo CERN/Atlas.

area, up to 400 m^2, is covered in the next shells with 1D silicon microstrip detectors. Also these detectors employ tens of thousands of CMOS chips for the signal readout and data processing. At the start of the LHC the overall number of pixels per experiment is not quite 10^9 yet. It is expected that a higher beam intensity in a couple of years will bring a need for upgrades with more pixel layers, to replace the currently installed layers of 1D silicon microstrip detectors. If the particle density in each beam crossing is increased, the projective 1D detectors can not cope with the ambiguities between several coincident particles anymore, and true 2D detectors are necessary.

It is not possible here to describe in detail all aspects of these complex systems, such as the data readout systems, the power distribution (~ 50 kW for the inner silicon detectors) and the cooling. Figure 7 gives an impression of the pixel detector for ATLAS, showing half of the barrel under final construction.

This device will sit tightly around the beam pipe, detect millions of particles per second and undergo a large amount of radiation over the planned lifetime of ~10 years. The survival of the CMOS as well as the silicon sensors has been studied and the use of standard technologies has been found acceptable. The unavoidable increase of sensor dark current and the changes of material properties can be mitigated by operating the detector well below 0 degree C. With the installation completed, the number of dead sensor elements is still below 1%, and the 'giga' detectors are practically ready to take beam.

Some Future Developments

The increased density in CMOS allows to integrate ever more functionality in each pixel while keeping dimensions of some tens of µm. This can improve precision in space and time for particle experiments. Eventually, trigger selectivity may profit if signatures for useful interactions could be determined. In other fields of science various new applications of particle detectors begin to appear. For example, pixel arrays are now used for X-ray imaging with individual processing of each incoming photonic quantum. This

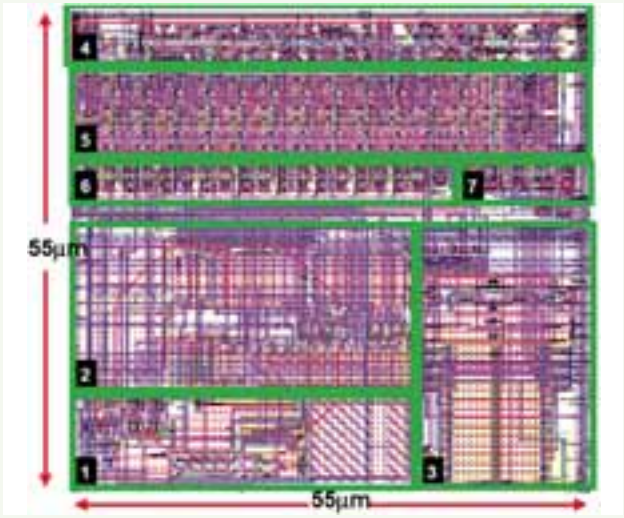

Fig. 8 Layout for the Medipix3 chip of a 55µm pixel cell in a 130 nm CMOS technology. Preamplifier, shaper and comparators, resp. 1, 2 and 3 form the analog part, while 3-7 are the control logic, counters, configuration and arbitration circuits. This pixel has more than 1080 transistors [25].

allows selection of energy bands and representation of the image in different "colours." Thresholding eliminates various types of background and long exposures can be made, such as needed with low intensity, nanofocus X-ray sources. Our group at CERN, with Michael Campbell as team leader, has designed the family of 'Medipix' imagers [24], building on the expertise in ionizing particle detectors. Figure 8 shows the layout of a pixel in the Medipix3 readout chip [25], the first particle detector where each pixel communicates in real time with all of its neighbours, to compare and add up coincident signals that belong to the same incident radiation quantum.

The Medipix chips are 3-side buttable, and the construction of a large area array will be needed to allow for use in medical applications. For a CT scanner a detector array of ~m^2 may be required. With ~ 50 000 pixels per cm^2 then such a device also will present close to 10^9 sensor cells, another gigasensor.

In conclusion, CMOS chips in conjunction with silicon diode matrices are now used on a large scale for ionizing particle imaging. They are catching quanta in physics experiments as well as in X-ray imaging. Eric Vittoz has been instrumental in guiding the early developments leading to these gigasensors. Not only computing and consumer electronics but also various branches of science can profit from the progress in microelectronics.

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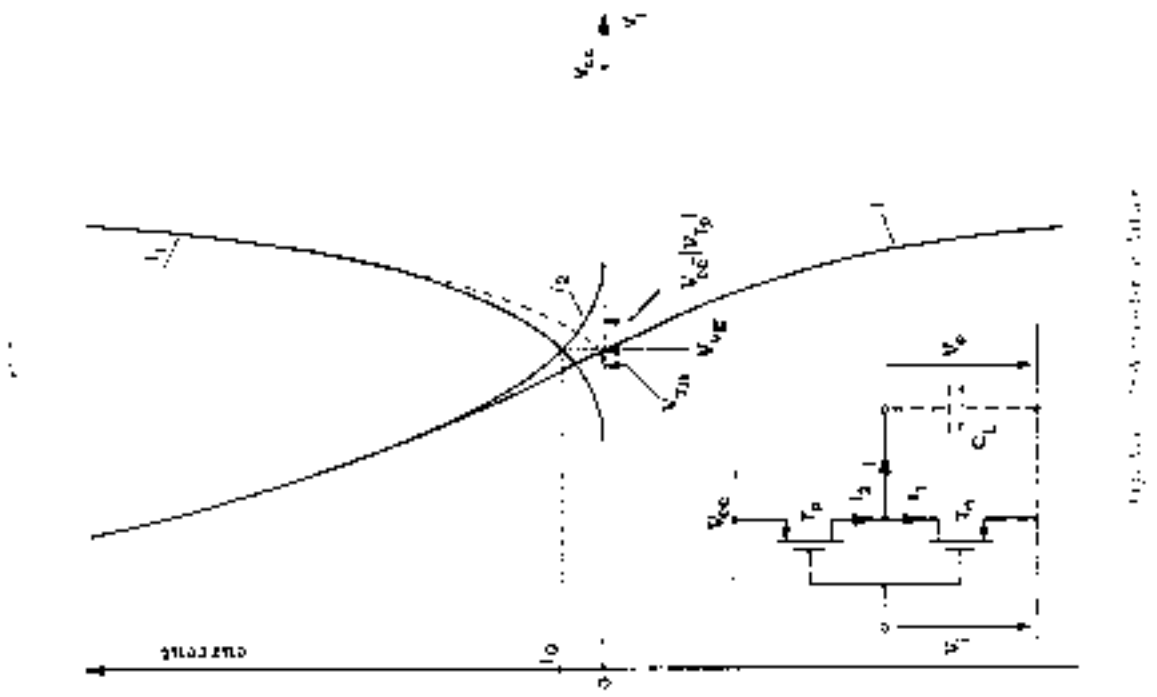
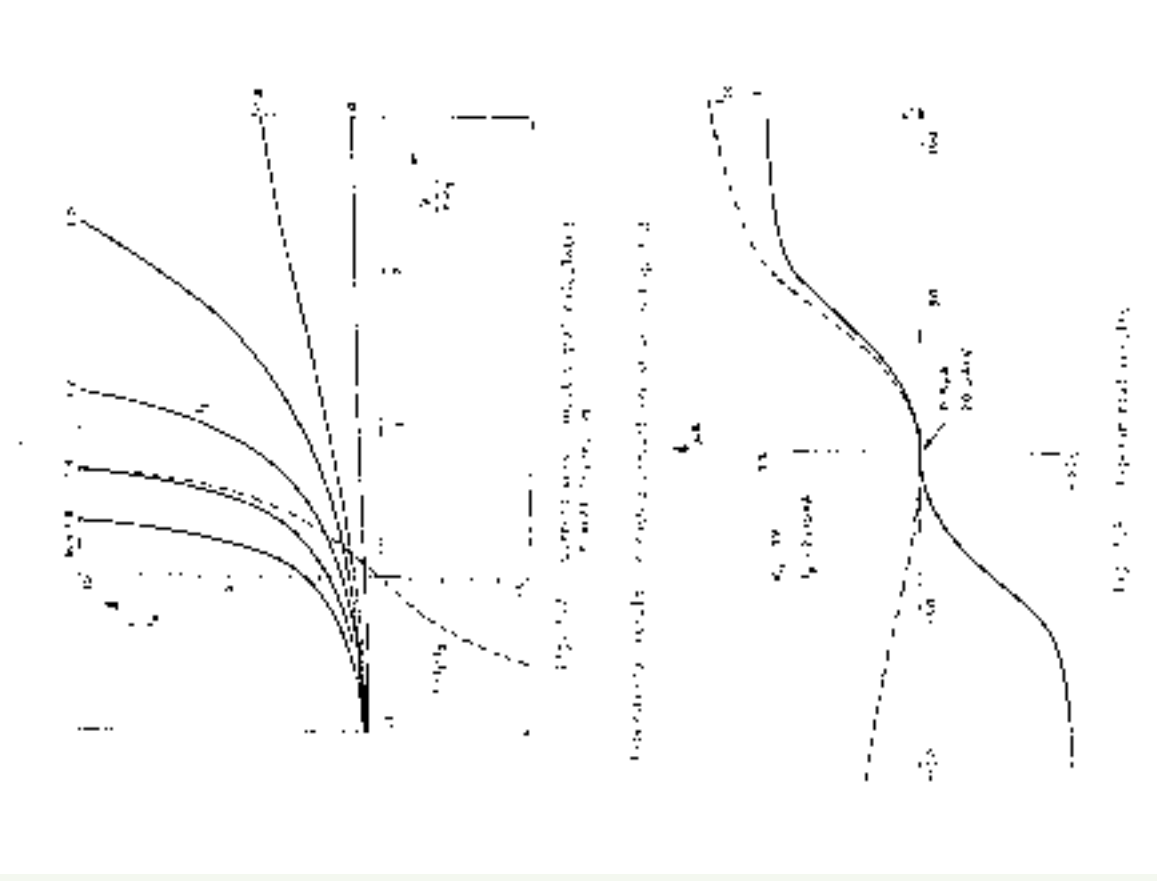
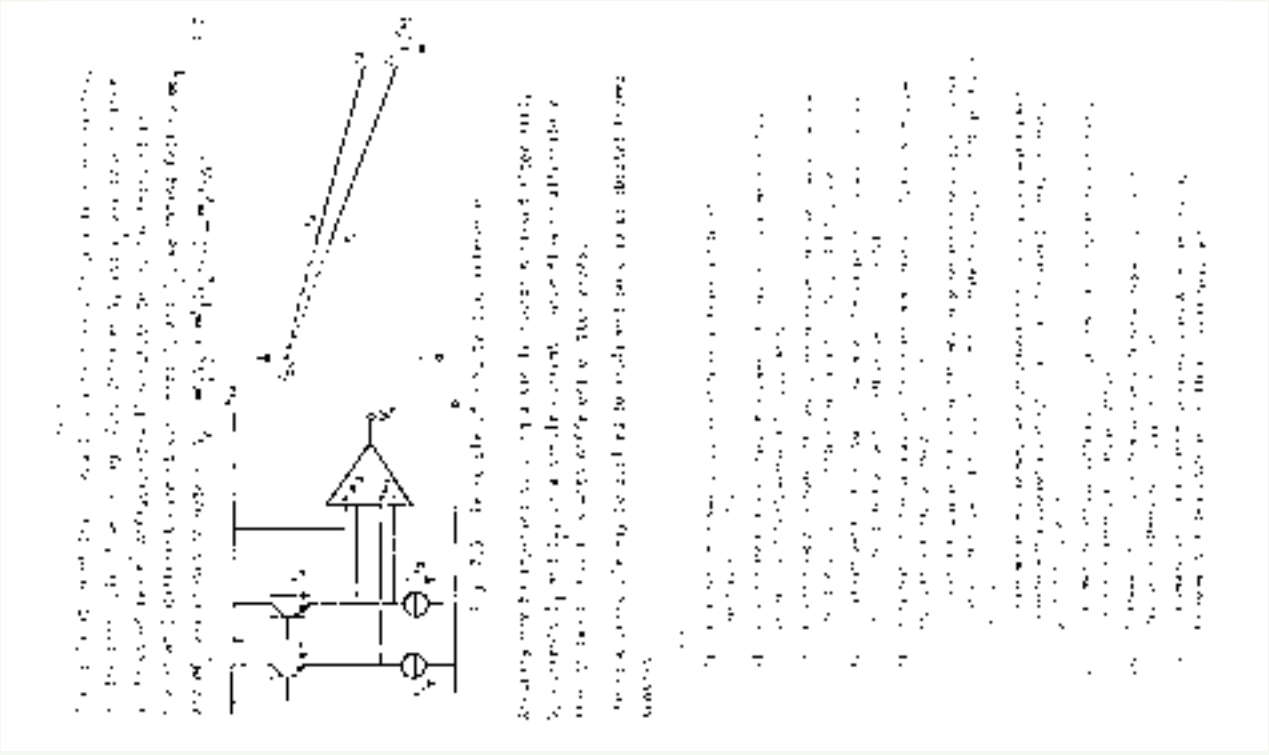
About the author

Erik Heijne (F '77) studied physics at the University of Amsterdam, where he assisted in projects on hydrogen/deuterium in palladium (1969) and on quantum effects in thin silicon films (1970). He came to CERN in Geneva in 1973, to work on silicon detectors for the monitoring of the neutrino beams. In 1980 the introduction of the silicon microstrip detector opened new ways for charm and beauty physics. A stay in Leuven (B) in 1984 led to the start of a microelectronics design group at CERN. Learning through different contacts in the IEEE, around 1995 he introduced at CERN the ideas for radiation hardness by design, which eventually became the basis for widespread use of CMOS in collider experiments. He is a Fellow of the IEEE and in 1999 received the Merit Award of the IEEE Nuclear and Plasma Sciences Society.







Eric A. Vittoz was born on 9 May 1938 in Lausanne, Switzerland. He obtained a Dipl. Ing. degree in 1961 from the Ecole Polytechnique de l'Université de Lausanne (EPUL) and a Ph.D. degree in 1969 from the Swiss Federal Institute of Technology in Lausanne (EPFL), both in Electrical Engineering. After spending one year at EPUL as a research assistant, he joined the Centre Electronique Horloger S.A. (CEH), Neuchâtel, in 1962, where he participated in the development of the first electronic wristwatch. He worked out various possible approaches for very low-power crystal oscillators and frequency dividers in bipolar technology, and co-published the first low-voltage CMOS integrated frequency divider in 1969.

In 1971, Dr. Vittoz was appointed vice-director of CEH, supervising and working on advanced developments in electronic watches and other micropower systems. While developing CMOS frequency dividers that became the standard in Swiss watches, he introduced the first true single-clock logic circuits. He later pioneered several new techniques for low-power and low-voltage CMOS analog design. These include circuits based on weak inversion operation (that he first applied to the watch crystal oscillators), bipolar-operated MOS transistors and pseudo-resistive circuits. These techniques were progressively applied to other low-power systems including biomedical devices, hearing aids, pagers, sensor interfaces and various portable instruments.

Together with several colleagues and students at CEH and EPFL, Dr. Vittoz progressively developed a model of the MOS transistor applicable to low-current and low-voltage circuit design, which later became known as the EKV model. He recently co-authored a book on this original model with Christian Enz.

In 1984, he joined the newly created Swiss Center for Electronics and Microtechnology (CSEM) in Neuchâtel, where he was appointed Executive Vice-President, responsible for Integrated Circuits and Systems from 1991 to 1997 and for Advanced Microelectronics later. While pursuing his work on very low-power systems, he championed the idea of biology-inspired collective processing by means of analog VLSI; his team has since developed several integrated vision systems based on this concept. From 1999 to 2004, he was partially retired from CSEM, with the position of Chief Scientist. He is now fully retired from CSEM.

In 1975, Dr. Vittoz introduced the first course on IC design at EPFL, emphasizing low-power devices and circuits. Becoming Professor in 1982, he lectured and supervised undergraduate and graduate student projects in analog circuit design until his retirement in 2004. He is still connected with EPFL as an invited professor, co-supervising some Ph. D. student projects. He has participated and still participates in numerous post-graduate and summer courses there, and in many countries around the world.

A Life-Fellow of IEEE, he has published more than 140 papers and holds 26 patents, receiving the Gold Medal from the Swiss Society of Chronometry and three ESSCIRC best paper awards. He is an ESSDERC/ESSCIRC Fellow, after contributing to the organization of these European conferences for more than 25 years. He was also a member of the European Program Committee of ISSCC from 1977 to 1989. As European representative to the IEEE Solid-State Circuits Council from 1987 to 1989, he participated in the creation of the SSC Society as one of the first AdCom members, and gave lectures for many years as a SSCS Distinguished Lecturer. He was the recipient of the 2004 IEEE Solid-State Circuits Award "For pioneering contributions to low-power modeling and CMOS circuit design."

Besides enjoying life with his family, Dr. Vittoz still pursues technical activities in teaching, writing and sporadically consulting in low-power circuits and systems.

Ankush Goel and Shih-An Yu Receive SSCS Predoctoral Fellowships for 2008-2009

John Corcoran, SSCS Awards Committee, john_corcoran@agilent.com

Ankush Goel of USC and Shih-An Yu of Columbia University have won the Solid-State Circuits Society Predoctoral Fellowship for 2008 - 2009. Their advisors are Hossein Hashemi and Peter Kinget, respectively.

This year the Society had nine very qualified nominees, seven from U.S. Universities and one each from China and India. The nominations were reviewed and ranked by a team of four professors from leading universities. (None of these universities had nominees in the running for this year's awards.)

According to the reviewing team, Ankush and Shih-An "stand out through their excellent academic records combined with an impressive list of high-quality journal and conference publications." In addition, they said "the research of the two recipients is very innovative and has the potential to have significant impact on the field of solid-state circuits." Please join us in congratulating Ankush and Shih-An for their achievements and for receiving this year's Fellowship awards.

Ankush Goel

Shih-An Yu

Ankush Goel received the B.Tech. degree in electrical engineering from the Indian Institute of Technology-Madras, Chennai, India in 2003. He was the recipient of the Prof. Achim Bopp Endowment Prize for best undergraduate hardware project. He received the M.S. degree in electrical engineering from the University of Southern California (USC), Los Angeles with a GPA of 4.0 in 2006. Earlier that year, he received an award from USC for outstanding academic achievement. He is currently pursuing his Ph.D. degree at USC and is a research assistant in the Electrical Engineering - Electrophysics Department.

From 2003-2004, he was an Analog Design Engineer with Texas Instruments, India. While he was there, he designed a slew-rate controlled pad driver in digital CMOS process for USB 2.0.

Mr. Goel is a recipient of the 2007 USC Annenberg Graduate Fellowship. During the summer of 2008 he was an intern at IBM T.J. Watson Research Center, NY, and worked on the design of a compact, low-power, low phase-noise, wideband digitally controlled oscillator.

At USC, his research has focused on analyzing nonlinear systems exhibiting multiple modes of operation and exploiting them for the implementation of multi-mode multi-antenna reconfigurable radios. He has designed and developed the theory of concurrent dual-frequency oscillators, dual-loop phased-locked loops and concurrent phased-arrays. He has published two MTT papers and one in JSSC related to that work. During his Ph.D. studies, he also worked on design and theory of sub-dB noise-figure, high-gain, wideband LNA.

Shih-An Yu received the B.S. and M.S. degrees in electrical engineering from National Taiwan University (NTU), Taipei, Taiwan in 1999 and 2001, respectively. For his M.S. research, he worked on wideband amplifiers with multiple feedback loops, and 5GHz VCO and image rejection receiver designs for ISM band applications. From 2001 to 2003, he designed self-calibrated fractional-N frequency synthesizers and mixed-mode analog baseband circuits for multi-standard mobile phone and WLAN transceivers at VIA Technologies Inc., Taiwan. From 2003 to 2005, he was a research assistant at NTU and did research on quantization noise suppression in fractional-N frequency synthesizers. He also designed the baseband circuits for an energy-efficient transceiver for long-term wireless bioactivity monitoring applications, presented at the ISSCC in 2006.

Since 2006, he has been working towards his Ph.D. degree at Columbia University in New York, NY under the guidance of Prof. Peter Kinget. His research focuses on highly scalable design techniques for RF frequency synthesizers addressing ultra-low supply voltage challenges, robustness issues and area scaling challenges in extremely scaled CMOS technologies. He has designed a 0.65V

fractional-N 2.4GHz frequency synthesizer that was presented at ISSCC 2007. He was also part of the student team designing a 0.6V highly integrated receiver for 2.4GHz applications in 90nm CMOS that was presented at ISSCC 2008. His latest results on a 0.042mm^2 fully integrated dual band 2.5/5.0GHz analog PLL in a 45nm CMOS technology will be presented at ESSCIRC 2008. This ultra-compact PLL incorporates a customized stacked capacitor-inductor structure that overlays the tank inductor over the loop filter capacitor, achieving a significant reduction of the active area. He is also investigating architectures for ultra wide-band, multi-standard frequency synthesizers for software-defined radio applications. At Bell Laboratories, Alcatel-Lucent, Murray Hill, NJ, he is participating in the design of a fractional-N frequency synthesizer operating from 50MHz to 8GHz.

Mr. Yu was the recipient of the 2008 Outstanding Student Designer Award presented by Analog Devices, Inc. He has published eight papers in conferences and five papers in journals. He has one U.S. patent application under review.

The Solid-State Circuits Society grants Predoctoral Fellowships each year to two deserving graduate students in the field of Solid-State Circuits. These Fellowships provide a $15,000 stipend and up to $8,000 in tuition and fees for the student, and an additional $2,000 for the student's department. The awards are granted to students who show promise for outstanding doctoral research, and who have shown concrete evidence of achievement early in their graduate careers. Nominations are typically due by May 1 of each year; see //sscs.org/awards/predoctoral.htm for more details on qualifications and the application process.

To view a list of prior Fellowship winners see //sscs.org/awards/predoctoral.htm#Pastrecipients.

IEEE DL Vojin Oklobdzija Visits Istanbul in May

Focuses on Low Power Digital Design in Talks at Two Universities

SSCS DL Prof. Vojin Oklobdzija lectured on 29 May, 2008 at Istanbul's Bogazici University (left) and at Istanbul Technical University (right).

IEEE Distinguished Lecturer Prof. Vojin Oklobdzija of UC Davis delivered two talks on low power digital design in Turkey, one on the morning of 29 May, 2008 at Istanbul Technical University (ITU) and the other later that day at Bogazici University (BU), also in Istanbul. Each lecture attracted about 25 participants from within the institution and from neighboring universities, design companies, and research centers. Prof. Oklobdzija focused on the problem of increasing power consumption by high-complexity digital integrated circuits, what prospects lie in the future, how power efficiency can be defined, the effect of some parameters such as power supply and device size on power efficiency, and some design suggestions to reduce power consumption. A long discussion followed each lecture. Prof Oklobdzija was delighted by the contributions of the attendees, who in turn enjoyed and profited immensely from his talk.

ITU and BU are two of the leading universities in Turkey. BU has an active IC Design laboratory with competence in analog integrated circuit design, CAD tool development, and low power design; ITU is becoming a center for IC design, with several national microelectronics-based studies and projects located at its VLSI Laboratory, which holds Europractice membership. Data converters, RF ICs, continuous-time filters and increasingly chaotic circuits with digital design are ITUís main areas of interest.

The IEEE Turkey Section is one of the most rapidly developing sections in Region 8, with around 15 chapters and more than 40 student branches; both universities have very strong competing IEEE Student Branches. At Dogus University an IEEE student branch organizes an annual student project contest entitled "PROJISTOR," sponsored by IEEE-Region 8, the IEEE Turkey Section, and local companies.

Izzet Cem Göknar
CAS Professor, IEEE Fellow
IEEE-CAS Turkey Chapter

Congratulations New Senior Members

20 Seniors Elected in May, June and July and August

Daniel Brookshire	Dallas Section
Dorin Calbaza	Toronto Section
James Chu	Atlanta Section
Frank Dunlap	San Francisco Section
Luiz Franca Neto	Santa Clara Valley Section
Prince Francis	Toronto Section
Khosrow Ghadiri	Santa Clara Valley Section
Steven Gillig	Chicago Section
Alireza Kaviani	Santa Clara Valley Section
Ronald Kubacki	Santa Clara Valley Section
C. Andrew Lish	New Hampshire Section
Chao Lu	Santa Clara Valley Section
Wing Luk	New York Section
Ron Maltiel	Santa Clara Valley Section
Mohammad Monzer	Mansour Lebanon Section
Joo Tham	Santa Clara Valley
Antonio Mondragon Torres	Dallas Section
Vladislav Potanin	Santa Clara Valley Section
Mohammad Shakiba	Toronto Section
Roger Sheppard	Oregon Section

Tools: Tips for Making Writing Easier

Part 3: Focus on Your Key Message

Peter and Cheryl Reimold, www. Allabout communication.com

In the last two columns we discussed quick ways to structure your writing to ensure that you tell your readers what they want to know in a format they can easily follow. Now we come to the writing itself: putting one word after the other. To choose the best words and place them in the most readable order, focus on your message. What exactly are you trying to say? If you find yourself getting tangled up in fuzzy words and complicated structures, stop and ask yourself just that: What am I trying to say? Don't write a thing until you are satisfied with your answer. Then try the following suggestions.

Trust your voice. Don't just trust it—use it. Say your sentences to yourself (quietly!) before you commit them to the paper or screen. Mouth them, whisper them; utter them any way you choose but do not put them on paper until you have heard them. After a while you will find that you hear them in your mind as you write them. Then you can dispense with the embarrassing mumbles.

This is the most important rule for clear and simple writing. Almost all the puffy polysyllabic verbiage people produce in the name of business or technical writing would never arrive to torture its readers if the writers had been forced to say the message out loud first. Can you imagine yourself saying, "Per our discussion, enclosed are copies of the documents referenced in our conference paper"? Of course not! You would probably say, "Here are the three articles you requested," and then list the titles, thus giving the reader more information in much easier language. Don't worry about sounding too informal if you trust your voice. Inappropriate or inelegant words will jump out at you as you read over your piece (which you must always do). In the example you might have said, "Here are the three articles you asked to see." Although this is still not nearly as bad as the original pompous statement, it could be smoother. Check your action words. If you find strings of small words (like asked to see), try to substitute a single verb (like requested).

Put your main thought in the main parts of the sentence: the subject, verb, and object. Because we tend to think and speak directly, you will usually follow this rule if you trust your voice. Overcomplicated, wordy writing almost always violates it. It is an easy rule to test, and it can clarify your sentences most wonderfully. Here is an example. The fact that we rewarded all ideas in the brainstorming meeting had the effect of inducing more solutions. Here the subject is fact, the verb had, and the object effect. The result— fact had effect—is meaningless. Let's try a rewrite. Rewarding all ideas in the brainstorming meeting produced more solutions. Here the subject is rewarding, the verb produced, and the object solutions. The result—rewarding produced solutions—captures the essence of the sentence.

Put the most important words at the end of the sentence. In English, the last words get the most emphasis. To get the reader to focus on the main point of your sentence, try to put it there. Consider some famous sentences: To be or not to be, that is the question (Shakespeare). When you come to a fork in the road, take it (attributed to Yogi Berra). Either that wallpaper goes, or I do (said to be the last words of Oscar Wilde). Now look what happens if we reverse the order: The question is whether to be or not to be. Take a fork in the road when you come to it. Either I go or that wallpaper does. Enough said.

Cheryl and Peter Reimold have been teaching communication skills to engineers, scientists, and business people for more than 20 years. Their firm, PERC Communications (+1 914 725 1024, perccom@aol.com), offers businesses consulting and writing services, as well as customized in-house courses on writing, presentation skills, and on-the-job communication skills. Visit their Web site at http://www.allabout-communica tion.com.This article is gratefully reprinted with permission from the authors as well as permission from the IEEE Professional Communication Society Newsletter Editor. This article is reprinted from the July/August 2003 issue, Volume 47, Number 4, page 10 of the IEEE PCS Newsletter.

ISSCC 2009 Feb 8-12 Preview

Anne O'Neill, SSCS Executive Director, a.oneill@ieee.org

As the world's leading forum for the presentation of advances in solid-state circuits and systems-on-a-chip, the International Solid-State Circuits Conference offers a unique opportunity for engineers working at the cutting edge of IC design and use to maintain technical currency and to network with leading experts.

Here are some highlights of the Society's flagship San Francisco-based conference as of the time of print; corrections and details may be found in the official Advance Program published in November. The web site for conference registration will open at the end of November. www.isscc.org/isscc. Forums, Tutorials, and the ISSCC Short Course require special registration.

In 2009 there will be four plenary presentations, approximately 250 technical papers and nine evening panels/special evening sessions, with panelists to be announced; all are included in the registration price. The schedule and details of the all-day Short Course on "Low-Voltage Analog and Mixed-Signal CMOS Circuit Design," the eight circuit design forums, and the ten 90-minute tutorials still under development will be published on the conference site.

Theme: Adaptive Circuits and Systems

Along with the numerous topics that registrants and readers have come to expect from the ISSCC, many papers among the 250 in 2009 will focus on the theme "Adaptive Circuits and Systems." Contributions were encouraged from researchers and designers who have demonstrated novel adaptive circuits and system techniques in the subject.

Technology scaling is enabling the integration of vast systems, encompassing billions of transistors on a single silicon chip. Along with opportunities for integration, sub-50nm technologies present new challenges of device variability, reliability, and low voltage operation. Environmental constraints on power consumption and cooling are further complicating the design space. Adaptive circuits and systems offer the potential to dynamically optimize operating parameters such as performance and power.

ISSCC Student Forum 2009

Anne O'Neill, SSCS Executive Director, a.oneill@ieee.org

ISSCC's Student Forum features the highly acclaimed communications challenge for hi-tech, the 5-minute presentation. It will return to ISSCC in 2009 on Sunday afternoon, February 8 and extend into the evening with poster presentations.

The objective of the ISSCC Student Forum is to provide a networking venue for students to exchange ideas at an early stage in the graduate education process. The presentation opportunity exposes students to ISSCC quality and encourages future paper submissions. The five minute limit on presentations provides a challenge that improves communication skills and will continue this year with shorter and more focused dialogs during the evening poster sessions.

Speakers for the Student Forum will be selected based on a brief recommendation letter from the advisor (1 paragraph) and research results (a 200 to 250-word abstract and 4 to 6 Power Point slides). Work in progress is expected, and results with actual silicon implementation are highly encouraged. Papers that have been accepted at ISSCC will not be considered for the Student Forum. However, papers that significantly extend an ISSCC publication will be considered. Submission will be via the ISSCC web site and are limited to one per faculty advisor. There will be 30 to 40 presentations selected with effective regional balance in mind.

Presentations at the Student Forum are not considered ISSCC papers; they will not be published or referenced as a paper, and do not constitute prepublication.

For details about submission see www.isscc.org/isscc/studentforum/ (The deadline is October 31, 2008). Please contact Professor Anantha Chandrakasan (Student Forum Chair) at anantha@mtl.mit.edu , TEL: 617-258-7619, if you have any questions.

4th Asian Solid-State Circuits Conference - Digital Convergence for a Ubiquitous Lifestyle

More than 100 Papers Selected for Meeting on 3 – 5 November, Fukuoka, Japan

Koji Kito, A-SSCC 2008 Organization Committee Chair, kito.koji@starc.or.jp

The fourth Asian Solid-State Circuits Conference will be held on November 3 - 5, 2008, in Fukuoka, Japan, at the JAL Resort Seahawk Hotel located on the scenic waterfront of the city. Sponsored by the IEEE Solid-State Circuits Society, this annual conference has travelled around major Asian countries including Taiwan (2005), China (2006), and Korea (2007). It offers a unique opportunity for engineers, researchers and business leaders to come together on-site to explore the future of circuit design technologies and to feel the influence of Asian countries in the rapidly globalizing IC industry. The theme of this year's conference is "Digital Convergence for a Ubiquitous Life Style."

Mr. Yoshiaki Kushiki

Dr. Young Hwan Oh

Dr. Bill Krenik

Plenary Talks

Three plenary talks will be presented by distinguished leaders in the IC industry:

The first speaker, Mr. Yoshiaki Kushiki, Senior Fellow of Panasonic (Japan) will give a speech entitled "Aiming for an Environmental-Oriented CE Platform."

The second speaker, Dr. Young Hwan Oh, President and CEO of Dongbu HiTek Semiconductor (Korea) will talk on "Foundry- Fabless Collaboration for Semiconductor SoC Industry in Korea."

The last speaker, Dr. Bill Krenik, CTO of TI (USA) will give a talk on "4G Wireless Technology: When will it Happen? What does it Offer?"

Submissions Represent 26 Countries

A-SSCC 2008 received 309 paper submissions, of which 116 were selected for presentation. The paper submission distribution is: Taiwan 68, Japan 53, China 51, Korea 42, USA 22, India 14, Iran 11, Singapore 11, Canada 6, Vietnam 5, Sweden 4, Belgium 3, Australia 2, Finland 2, Hong Kong 2, Poland 2, Switzerland 2, Austria 1, Egypt 1, Germany 1, Malaysia 1, Netherlands 1, Portugal 1, Spain 1, Romania 1, United Arab Emirates 1. Since the TPC consist of a balanced mix of experts from both industry and academia, the final technical program covers the interests of attendees from most IC product segments.

Four Tutorial Sessions and Two Panels

Tutorials on November 3rd are "Design of Femto-joule Energy Efficient ADCs in CMOS," "Advanced SiP Design," "Economic and Design Choices for Nano-scale Electronic Systems," and "Advanced Clock Distribution Systems." The two panel discussions on 4 November are entitled "SiP2.0: What, When, and How?" and "Digitally Assisted Analog and RF Circuits: Potentials and Issues."

Industrial Program

In A-SSCC's unique "Industry Program," speakers present cutting-edge product chips, not only in a detailed chip or circuit description but also through demonstrations and evaluation results to show how customers have improved their performance by using the chips.

Student Design Contest

Authors of the eight outstanding chip designs accepted for the conference program will offer demonstrations and commentary at the conference site. The student design that best reflects the high research standards of Asian academies will be selected from the eight.

I am looking forward to seeing you in November in Fukuoka, and hope that you will enjoy an excellent meeting and warm hospitality at the conference.

For more detailed information about A-SSCC, please visit the web site: www.a-sscc.org

The International Conference on Computer Aided Design (ICCAD) Previews Novel Program

External Workshops will Collocate with ICCAD on 10-13 November in San Jose

Juan Antonio Carballo, ICCAD Publicity Chair, juananto@us.ibm.com

Already past its 25th anniversary, the International Conference on Computer-Aided Design (ICCAD) continues to evolve with an outstanding technical program in 2008. Offering high quality technical papers, interactive panels, networking receptions, and embedded and stand-alone tutorials, ICCAD will also open its doors to new external workshops, which will be collocated with the conference and will leverage the professional management for which it is known.

Outstanding Keynotes and Special Talks in Emerging Fields

In the opening session, a keynote address by Mary Lou Jepsen, founder and CEO of Pixel Qi and chief hardware architect and first CTO of the "One Laptop per Child" project will focus on innovating computing platforms for emerging low-income geographies. Dr. Jepsen will also speak on CAD for displays.

Our second keynote will feature the world-renowned Dmitri "Mitya" Chklovskii, of Janelia Farm, Howard Hughes Medical Institute, whose research is on the human brain and how it relates to conventional computers.

During lunch on Tuesday, November 11, Giovanni de Micheli, a distinguished EDA (Electronic Design Automation) veteran will discuss exciting new frontiers in biology and environmental engineering.

World Class Technical and Non-technical Program

ICCAD continues to be the ideal place for discovering top design technology innovation and staying on top of emerging design fields. This year's meeting offers superb papers and tutorials within a venue for maintaining and growing one's network and touching base with all aspects of the electronic design automation sector.

From 458 worldwide submissions, a 90-strong technical program committee selected 122 outstanding papers for presentations split into 40 sessions over three days. ICCAD will also feature four half-day tutorials plus three embedded tutorials and two special designer sessions providing additional broad perspectives. To enable registrants to attend tutorials and collocated workshops, tutorials will run in parallel with technical sessions, while workshops will be held on Sunday and Thursday.

Recognizing the increasing value of networking, ICCAD will host numerous social events and meetings designed to keep attendees in touch with like-minded colleagues. These events include ICCAD's traditional Monday evening panel on the future of technology plus numerous meetings for CEDA, SIGDA, DATC, and other organizations.

About ICCAD

The International Conference on Computer-Aided Design (ICCAD) is the world's premier conference in electronic design technology and has served EDA and design professionals for the last 25 years by highlighting new challenges and breakthrough innovative solutions for integrated circuit design technologies and systems. To learn more, please visit the ICCAD website at www.iccad.com.

ICUWB 2009 to Focus on Microvave and Millimeter Wave Band Technology

IEEE International Conference on Ultra-Wideband Will Meet on 9–11 September 2009 in Vancouver

Lutz Lampe, General Chair, 2009 IEEE ICUWB, lampe@ece.ubc.ca

The IEEE International Conference on Ultra-Wideband (ICUWB) of 2009 will center around the general topic of UWB transmission in micro-wave and millimeter wave bands and over power lines.

Continuing a series of annual international UWB conferences held in Baltimore (2002), Reston-VA (2003), Oulu (2003), Kyoto (2004), Zurich (2005), Waltham-MA (2006), Singapore (2007), and Hannover (2008), it will focus on the latest advances in UWB technology, current and future applications ranging from UWB communication for personal area and sensor networks to UWB-based localization and positioning systems to UWB vehicular radar and imaging systems, and standardization and regulation for UWB transmission.

The conference venue is the Hyatt Regency Vancouver, located in the heart of the city. Main technical and social functions will be held at the Hyatt's Perspectives Level on the 34th floor, from which ICUWB attendees will have a stunning picture-postcard view of Vancouver and its surrounding scenery. The social program includes a welcome reception, luncheons, and the gala conference banquet,

ICUWB has evolved since 2002 into the leading annual conference solely dedicated to UWB technology, bringing together more than 200 researchers and engineers from academia, industry, government and standardization organizations, as well as vendors and customers of UWB technology. The ICUWB program of 2009 will feature invited plenary sessions and symposia by international experts and new product displays by market leaders in the field.

The technical program will extend over three full days and include topics in

- UWB Hardware Architecture and Implementation (RF modules, circuits and systems, low power consumption techniques, pulse generation and detection, OFDM implementations, integrated circuits designs, and system architectures)
- Antennas and Propagation (UWB antennas and arrays, channel measurements and modeling, field trials)
- UWB Cognitive and Cooperative Systems (energy efficient cross-layer design, spectrum sensing and dynamic spectrum sharing)
- Communication and Signal Processing (coding and modulation, ranging, localization and positioning)
- Applications (wireless personal/body area networks, sensing and medical imaging, home networking, radar, consumer electronics)
- Standardization and Regulation (spectral management, co-existence, emerging wireless standardizations).

Prospective authors are invited to submit technical papers until 23 February 2009. All accepted papers will be published by the IEEE and included in IEEE *Xplore*.

For more information visit the 2009 ICUWB website www.icuwb2009.org.

First IEEE COMCAS a Mega Event in Tel Aviv

SSC Sessions Span Two Days

Mark Ruberto, IEEE Israel Chapter Chair of the Solid-State Circuits Society, ruberto@ieee.org,
Shmuel Auster, COMCAS Conference Chair, auster@ieee.org,
Barry Perlman, COMCAS Technical Program Chair, b.perlman@ieee.org

The annual meeting of the Israeli Chapter of the Solid-State Circuits Society took place at the Hilton Hotel in Tel Aviv on 13-14 May, 2008 within the framework of the first IEEE Conference on Microwaves, Communications, Antennas, Solid-State Circuits and Electronic Systems (IEEE COMCAS 2008).

Building on the yearly IEEE Israel AP/MTT & AES Chapters Symposium, this exciting, two-day conference and exposition was organized as a multidisciplinary forum for internationally recognized scientists and engineers and students from various complementary disciplines to meet and discuss subjects of common interest.

Last year's very successful 21st IEEE AP/MTT&AES Chapters Symposium, with over 500 participants from many companies and R&D institutions, encouraged and inspired the organizers to work with other IEEE societies to take on the challenge of organizing an even greater event with the help of the larger IEEE and global technical community. The three additional IEEE societies, namely the Solid-State Circuits Society (SSCS), the Communications Society (ComSoc), and the Electromagnetic Compatibility Society (EMCS) joined forces with the Microwave Society (MTT-S), Antennas and Propagation Society (AP-S), and Aerospace & Electronic Systems Society (AES-S) to create this mega-event.

COMCAS 2008 delivered on the promise of attracting the global community to Israel, with over 700 participants, 146 papers, 15 technical sessions, five parallel meeting rooms and a large professional exhibition with 62 booths. The program offered a very impressive list of speakers, including expert R&D engineers, top scientists and managers from Asia, the US, Europe, Latin America, the Far East and Israel.

The disproportionately large number of solid-state circuit contributions required the extension of the original, one day SSCS session to two full days. On the first, Tuesday, May 13, there were eight papers in Analog/Mixed Signal and five papers on VLSI/SoC/Sensors. On Wednesday, May 14, there were four papers on VLSI/SoC/Sensors, 14 papers on RFICs, and three papers on Si MEMS.

There were two keynote speakers: The first was Raviv Melamed, General Manager, Mobile Wireless

Group lunch at COMCAS 2008 on the Mediterranean Coast of Israel.

62 exhibitors operated booths at COMCAS 2008.

COMCAS 2008 keynote speakers were Linda Katehi and Raviv Melamed.

Group, Intel Corp., Haifa, Israel. The title of his talk was "Future Wireless Applications and Technologies." The second keynote speaker was Prof. Linda Katehi, Provost, University of Illinois, USA whose talk was entitled "Advanced Component Architectures." Both keynote addresses were very well received.

Other conference sessions had an interesting breadth of technical papers, from leading edge microwave devices, ingenious architectures, advanced analog and mixed-signal circuits to clever antenna technology, and information on new and old RADAR and communication systems. Many local practitioners, engineers and decision makers from the technology, communication, radar and electronic systems communities participated and many presented papers on technology, circuits, system aspects and innovations in these fields. Fascinating up-to-date topics were also presented to enrich the microwave, antenna, communication, EMC, solid-state circuits (RFIC) and electronic systems communities with knowledge, ideas, applications and challenges. Emphasis was on applications-oriented research and development, from devices and components to circuits and systems, to antennas, communications and networking, sensors and radar and software, on a variety of subjects including

- FICs
- Low Power Solid-State Circuits
- Microwave Plasmonics and Nano-meta materials
- Novel Antennas and Spectrum Data Base Issues
- Phased Arrays, Communications Networking
- C3/C4 modeling and simulation, and analysis (MS&A)
- RF Propagation to MMW Wavelengths
- High Power Amplifiers
- Advanced Devices for Communications
- RF Filters, Modeling for EMC, MEMs
- Ultra-wide Band Technology
- Metrology and Parameter Extraction
- Space-time Adaptive Processing
- Cognitive Radios/Radar and Spectral Processing

COMCAS 2008 was chaired by Shmuel Auster of Elta Systems. The Technical Program Chair was Dr. Barry Perlman, U.S Army Communications-Electronics RD&E Center (CERDEC) and incoming MTT-S President. SSCS Technical Sessions were organized by Mark Ruberto, SSCS Israel Chapter Chair, David Gidony, and Miki Moyal, all from the Israel Design Center of Intel Corporation.

The full technical program can be seen on the conference webpage at www.comcas.org, and papers from the conference are now available in IEEE *Xplore*. It is the intent of the Israel SSCS Chapter to participate annually in subsequent COMCAS conferences as the main venue for its annual technical meeting, and to encourage a larger foreign participation as well.

Mark Ruberto (center), a COMCAS 2008 Technical Session organizer, receiving a certificate of appreciation from COMCAS Chair Shmuel Auster (left) and Barry Perlman, COMCAS Technical Program Chair.

SSCS-Singapore Hosts 90 at ISSCC 2007 Tutorial in August

DVD Replay Combined with Colloquium on How to Write an ISSCC Paper

Prof. Yong Ping Xu moderating an ISSCC DVD tutorial replay at the National University of Singapore in August.

To encourage submissions to ISSCC from industry in Asia, SSCS-Singapore hosted an ISSCC 2009 promotional event in August featuring a replay of the 2007 Conference tutorial "Continuous-time Sigma-Delta Data Converters" by Yiannos Manoli.

Spearheaded by Prof. Yong Ping Xu., Singapore Chapter Treasurer, in cooperation with the Department of Electrical and Computer Engineering of the National University of Singapore, the event was open to academics and students and attracted 24 from industry. Admission was free and light refreshments were served. Dr. Xu also moderated the replay of the Manoli tutorial as well as a presentation of the audio tutorial "Writing a good ISSCC paper," created by ISSCC Press/Awards Chair Kenneth C. Smith and past ISSCC Program Chair Prof. Jan Van der Spiegel of the University of Pennsylvania, who is SSCS Chapters Chair. It is available at the Societyís website //sscs.org/Chapters/07ChptLnch/ 07FEBCafe.htm.

SSCS-Singapore expects to hold more ISSCC 2007 DVD replay events at Nanyang Technological University and at other sites.

Katherine Olstein,
SSCS Administrator,
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SEMINAR ANNOUNCEMENT

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NUS

DVD replay of ISSCC 2007 Tutorial and Promotion of ISSCC 2009

Organized by
Dept of ECE, NUS and
IEEE Solid-State Circuits Society Singapore Chapter

TOPIC	:	Continuous-Time ΔΣ Data Converters
SPEAKER	:	Yiannos Manoli Chair of Microelectronics University of Freiburg, Germany
DATE	:	22 August 2008 (Friday)
TIME	:	3.00 pm to 6.00 pm
VENUE	:	E3-06-09, Engineering block E3, NUS

ABSTRACT

While technologies are continuing to provide us with ever faster transistors they also demand that we work at lower supply voltages. The analog designer has to search for new concepts to counteract the reduction of signal swings and increase in power. Although time-continuous circuits are anything but new, they are gaining a renewed interest not only in the academic, but also in the industrial community. With the main focus on baseband applications, different aspects of continuous-time modulators will be covered when operated under low-power and low-voltage constraints; Architectures for baseband applications; Implicit anti-aliasing filter; Influence of non-idealities and correction techniques; Implementations (low power, ultra wideband, high performance).

SLIDES PRESENTATION

"How to write good ISSCC papers" by Jan van de Spiegel and Kenneth Smith.

Presented by Associate Professor Xu Yong Ping.

BIOGRAPHY

Yiannos Manoli holds the Chair of Microelectronics at the University of Freiburg, Germany. His current research interests lie in the design of low-voltage and low-power mixed-signal CMOS circuits, sensor read-out circuits as well as A/D- and D/A-converters with over 150 papers in these areas. He holds a B.A. degree in Physics and Mathematics, a M.S. degree in electrical engineering and computer science from the University of California, Berkeley, and the Dr. Ing. Degree in electrical engineering from the Gerhard Mercator University in Duisburg, Germany.

REMARKS

All are welcome! Admission is free and refreshment will be served.

Pre-registration will be required.

Kindly register with Ms Diana Ng of ECE Dept by 21 August 2008 (12noon), either by Tel: 6516 2109; Fax: 6779 1103; or Email: diana_ng@nus.edu.sg

If you are unable to view this email correctly, please refer to the ECE seminar webpage at: http://www.ece.nus.edu.sg/stfpage/elehmp/seminar/2007.htm

SSCS-Taipei Offers Short Course on CMOS Single-chip Radio Design

Programs in Hsinchu and Taipei Funded by SSCS Extra Chapter Subsidy

Eric Tsung-Hsien Lin, IEEE SSCS Taipei Chapter, thlin@cc.ee.ntu.edu.tw

Dr. Bogdan Staszewski of Texas Instruments presenting his lecture on CMOS single-chip radio design at National Chiao-Tung University, Hsinchu, on August 20, 2008 (left) and at National Taiwan University, Taipei, on August 21, 2008 (right).

Integrated radios for multi-GHz frequencies have recently migrated to low-cost nanometer-scale CMOS processes. Unfortunately, this environment, which is optimized for digital circuits, is extremely unfriendly for conventional RF and analog designs. As a result, a paradigm shift is occurring that transforms RF and analog circuit design complexity to the digital domain for wireless transceivers to enjoy the benefits of digital approaches, such as process node scaling and design automation.

In light of this shift, SSCS-Taipei invited Dr. Bogdan Staszewski of Texas Instruments to give a two-day short course on the subject of CMOS single-chip radio design.

Approximately 45 participants attended his lecture "Digital RF Processor (DRPTM) for Single-chip Mobile Radios: All-digital PLL, Transmitter and Discrete-time Receiver" at National Chiao-Tung University in Hsinchu, and 35 attended the same course at National Taiwan University, Taipei, on August 20 and 21, 2008, respectively. Participants from industry and academia were about equal, an indication that the topic elicited wide interest from the Taiwanese IC research and development communities.

Dr. Staszewski began with an introduction to the DRP approach and explained how it was conceived initially. He then described the design principles of an all-digital phase-locked loop (ADPLL). Various aspects of ADPLL design, including theoretical analysis, system modeling, sub-circuit designs, and simulation considerations were discussed, including transmitter design based on the ADPLL. Dr. Staszewski next presented a direct-sampling discrete-time receiver design and several more design examples.

His course, which included a good mix of theoretical and practical design knowledge, was well-received and considered valuable for the research of many attendees.

The Taipei Chapter greatly appreciates the financial support of the IEEE Solid-State Circuits Society for this program.

SSCS DL Stefan Rusu Speaks at Santa Clara Valley Chapter Meeting in August

Katherine Olstein, SSCS Administrator, k.olstein@ieee.org

SSCS DL Stefan Rusu, a Senior Principal Engineer at Intel Corporation, addressed the Society's Santa Clara Valley chapter on 21 August about "Power and Leakage Reduction in the Nanoscale Era." One attendee, Himanshu Arora said, "I rate his talk among the top 1% of presentations that I have ever attended at IEEE local meetings." The slides that Dr. Rusu used may be found on the chapter website, at //ewh.ieee.org/r6/scv/ssc/index.html.

Dr. Stefan Rusu discussed nanoscale power and leakage reduction with members of SSCS Santa Clara in August.

Lectures by Ali Niknejad of UC Berkeley, Michael H. Perrott of MIT and Boris Murmann of Stanford are planned for the chapter's September, October and November meetings, respectively.

Prof. Niknejad will speak on research at the Berkeley Wireless Research Center (BWRC) related to mm-wave electronics, including active and passive design techniques; circuit approaches, and system architecture for short range mm-wave communication links; and the design of several key building blocks, such as the LNA, mixer, and PA.

Dr. Perrott (now with SiTime, Sunnyvale, CA) will discuss the implementation advantages provided by digital phase-locked loops compared to their analog counterparts, and explore the question of whether such digital structures can support high performance applications in which low jitter and high PLL bandwidth is required by discussing techniques for achieving high performance digital fractional-N synthesizers, including high resolution time-to-digital conversion, digital quantization noise cancellation, and low-jitter divider structures. Prof. Murmann will present "Future Directions in Mixed-Signal IC Design" in his talk. The Santa Clara Valley Chapter Chair is Dan Oprica.

SSCS-Scotland Sponsors Technical Meeting in September

K. Kundert Speaks on Verification of Complex Analog Circuits

Jim Brown, SSCS-Scotland Chapter Chair, jim.brown@diasemi.com

Around 40 people from local industry and academia gathered at the Central Edinburgh offices of Dialog Semiconductor on 28 September, 2008 to hear Dr. Ken Kundert talk about Verification of Complex Analog Integrated Circuits. The historic background of Edinburgh Castle contrasted with a topic which is at the leading edge of technology development.

Verification is becoming widely recognized as one of the most important issues in designing large complex analog and RF mixed-signal circuits. As a result, design methodologies are starting to change, mirroring a comparable change in digital design 10-15 years ago. In his presentation, Dr Kundert showed why the problem has become so significant, and what people are doing to control it.

From left: SSCS-Scotland members Dr. Sebastian Loeda and Dr. Paul Hammond, with Dr. Ken Kundert.

Dr. Ken Kundert is President and co-founder of Designer's Guide Consulting, a company that is guiding the industry towards the adoption of formalized analog verification. He worked previously at Cadence and HP, where he created Spectre, SpectreRF, Verilog-A/MS and HP's (now Agilent's) harmonic balance simulator. He has written three books on circuit simulation and modeling and created "The Designer's Guide Community" website. He received his Ph.D. in Electrical Engineering from UC Berkeley in 1989 and was elevated to the status of IEEE Fellow in January 2007 for contributions to simulation and modeling of analog, RF, and mixed-signal circuits.

Leuven Student Branch and SSCS Chapters Organize 2nd SSCS-Benelux Microelectronics Symposium

Cedric Walravens, IEEE Student Branch, Leuven, cedric.walravens@esat.kuleuven.be

After the success of last year's first Microelectronics Symposium, the IEEE-Leuven Student Branch and SSCS-Benelux chapters again put their hands together to organize a second symposium at the Electrotechnical Engineering Department of K.U.Leuven.

This year's meeting set out to investigate how industry and research institutions cope with the various budgets encountered by engineers, in particular how constraints, such as cost, energy consumption, and silicon area drive [or "empower"] them to go beyond the current state-of-the-art.

Sponsored by On Semiconductor (formerly AMIS) and NXP on 19 March, 2008, the event included a total of five speakers, who presented their views on "Power of Budget":

- Professor Wim Dehaene (K.U. Leuven) gave an introduction to Wireless Sensor Networks (WSN) and presented the current status of the Flemish-funded IWT-sbo Pinballs research project that focuses on the in-door localization of ultra-low power RFID nodes.

From left, Raff Rovers (NXP), Willy Sansen (SSCS President), Damien Mac (On Semiconductor), Ramses Valve kens (EASICS) and Cedric Walravens (IEEE Leuven Student Branch Chair). Missing from this picture are Wimp Deane (K.U.Leuven) and Tim Piessens (ICsense).

- Ramses Valvekens (EASICS) and Tim Piessens (ICsense) reported the results of the fruitful cooperation between their companies, both spin-offs of K.U.Leuven, on a project concerning novel commercial RFID applications.
- Professor Willy Sansen (K.U.Leuven and SSCS President) elaborated on the question of whether Moore's Law will save microelectronics and whether there is such a thing as "Moore than Moore."
- Damien Macq (On Semiconductor) presented an overview of both digital and analog commercial solutions currently available to customers world-wide and the different challenges encountered during their development.
- Raf Roovers (NXP) covered the whole design process from research to the final development of a W-USB product in a wrap-up speech, and shared his experiences in tackling different hurdles.

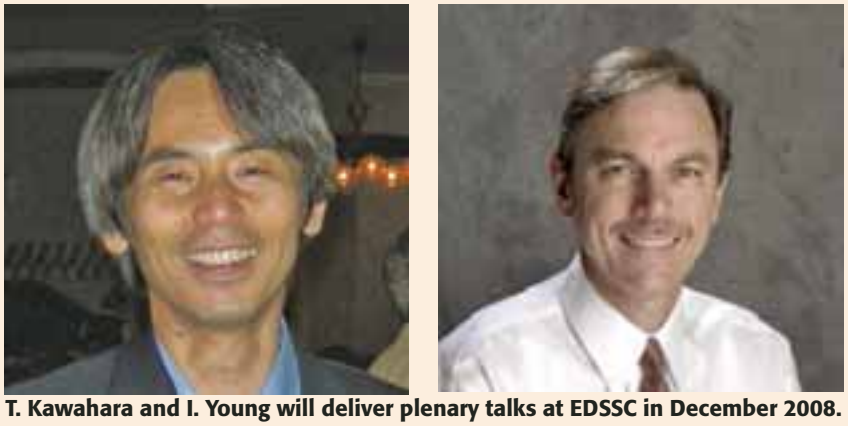
Preview of EDSSC2008 in Hong Kong

Three-Day Program in December to Feature 150 Papers and Plenary Talks by SSCS DLs T. Kawahara and I. Young

KP Pun, General Co-Chair, EDSSC'08, kppun@ee.cuhk.edu.hk

The 4th IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC 2008) will be held at the Renaissance Kowloon Hotel in Hong Kong from 8 to 10, December, 2008. The conference hotel is next to the famous Victoria Harbour, where attendees can enjoy Hong Kong's most beautiful night views.

Organized by the IEEE Electron Devices/Solid-State Circuits Hong Kong Joint Chapter and sponsored by the Hong Kong Applied Science and



T. Kawahara and I. Young will deliver plenary talks at EDSSC in December 2008.

Technology Institute and K. C. Wong Education Foundation, EDSSC 2008 is a three-day program covering broad areas in electron devices and solid-state circuits. It is expected that 150 technical papers will be presented by authors both from academia and industry around the world.

Highlights of the conference include two plenary speeches by renowned experts in the ED/SSC fields.

The first is "SPRAM (SPin-transfer torque RAM) Technology for Green IT World," by Dr. Takayuki Kawahara, Chief Researcher, Central Research Laboratory, Hitachi Ltd., Japan.

The second is "The SOC transformation of the Microprocessor - Clocking and Analog Circuits in High Performance Processors," by Dr. Ian Young, Intel Senior Fellow, and Director of Advanced Circuit and Technology Integration, Technology and Manufacturing Group, Intel Corporation, USA.

Details about the conference can be found at the conference website: www.ee.cuhk.edu.hk/edssc08.

IEEE SSCS Joint Chapter Formed in Penang, Malaysia

Yut Hoong, Chow. Chapter Chair, IEEE MTT-ED-SSCS Joint-Chapter, Penang, Malaysia

Boon Eu, Seow. Secretary, IEEE MTT-ED-SSCS Joint-Chapter, Penang, Malaysia

Founded by Dr. Grant A. Ellis in 2005, Penang's MTT/ED/AP chapter was the first IEEE chapter in the Bayan Lepas Free Industrial Zone, Penang, Malaysia.

A plan to start an IEEE SSCS chapter in Penang was started by Mr. Boon Eu Seow in 2006, but delayed due to the insufficiency of SSCS members there. Two years later, MTT/ED/AP Chapter Chair Mr. Yut Hoong Chow proposed that the AP unit of MTT/ED/AP be replaced by SSCS to better focus on related industries in the Bayan Lepas Free Industrial Zone. The group was reorganized officially on 15 May, 2008 and renamed the IEEE Microwave Theory and Techniques Society, the IEEE Electron Devices Society and the IEEE Solid-State Circuits Society (MTT/ED/SSC) joint chapter

A website that details the present and past activities of the chapter can be viewed at //ewh.ieee.org/r10/malaysia/mttedssc.

The Penang Chapter Mission

The IEEE Penang chapter hopes to support and accelerate the growth of electronic industries in its region by sponsoring and organizing seminars and lectures by subject matter experts. In this regard, IEEE distinguished lecturers have been very supportive, delivering many well-received and well-attended lectures to our group.

Penang - Malaysia's "Silicon Island"

Located in the north of Malaysia, Penang is one of the world's high-tech manufacturing centers, with more than 33 years of electronics industry activity, begun in 1972 with the establishment of the first Free Trade Zone in the country.

Penang's Bayan Lepas Free industrial Zone (FIZ) was started in 1972 by YAB Tun Dr. Lim Chong Eu, former Chief Minister of Penang. Bayan Lepas FIZ. At the size of 1300 acres, it serves as the country's free trade zone and has been home for over three decades to some of the world's top technology companies, such as Intel, Motorola, Agilent Technologies, Robert Bosch, Osram Optosemi-

Map of Penang, courtesy of Penang RF Cluster, www.investpenang.gov.my/PRFC.php

conductor, Seagate, AMD, Hitachi and Clarion.

Today, more than 700 transnational and local companies operate in the industrial parks in Penang, including Penang Biotech Park (also known as Penang Science Park), Perai Free Industrial Park, Perai Industrial Park, Seberang Jaya Industrial Park, Bukit Tengah Industrial Park, Bukit Minyak Industrial Park and Mak Mandin Industrial Park.

The State, whose economy for over three decades has been anchored in its manufacturing sector, is now moving upstream to include R&D and product development. Multinational companies including Motorola, Intel, Avago, Agilent, Altera, Renesas and Spansion have set up significant R&D centres to design MMICs, two-way radios, analog and digital ICs and measuring instruments.

Penang's skilled and knowledgeable workers are strongly supported and incubated by the institutions of higher education in the state, including the University of Science Malaysia, Wawasan Open University at George Town, the Penang Skill Development Center (PSDC) at Bayan Lepas, and the Malaysia-Japan Technical Institute at Bukit Minyak.

SSCS-Penang would like to thank Professor Jan Van der Spiegel of the University of Pennsylvania and SSCS Administrator, Katherine Olstein for their advice and support in setting up the chapter.

We would also like to take this opportunity to thank our chapter sponsors, the Motorola Penang and Penang Skill Development Center (PSDC) for allowing us the use of their halls and facilities for our chapter meetings and seminars.

ISSCC 2007 Short Course DVD Replayed in Penang in August, 2008

Attendees at SSCS-Penang's DVD replay of "RF Transceiver System Design in Nanometer CMOS" on 5 August, 2008. SSCS's new table skirt may be seen on the right.

This presentation reviewed the history of transceiver design, which has led to the inclusion of all-CMOS transceivers in handheld phones as a fast-becoming norm. It also examined the changes in the CMOS environment - the side effects of all those shrinking gates that are driving the trend toward digitally assisted, and sometimes even disappearing, analog circuits. It also showed examples of how this trend is making itself felt in the RF arena.

Abstract

In articles, textbooks and research papers we are told again and again that even as CMOS gate lengths become ever smaller, "the analog doesn't shrink." But cell phones have gotten smaller somehow, and the smart money says they will continue to pack more features in the same or smaller form factor for some time to come.

Many of the secrets behind this apparent contradiction lie in IC system-level design. The RF transceiver designer is faced with myriad design choices that have huge impacts on overall IC performance; choosing the performance targets for the IC is not to be taken lightly. For example, just as in the digital and traditional mixed-signal domains, a goal of minimizing die area as opposed to minimizing current draw can lead to a vastly different set of choices for the LNA, Mixer, baseband filter, and data converter parameters. Likewise, those ever-shrinking gate lengths do indeed lead one to make sharp turns along the path toward the final block specifications.

Romania SSCS Chapter Formed to Promote Circuit Activities in Eastern Europe

Marcel Profirescu, Chapter Chair, profires@edil.pub.ro

After the. IEEE Romania Section was established in 1986, and EDS-Romania formed in 1992, I had the idea of founding an SSCS Chapter for quite some time to stimulate local activities in circuits, and to promote circuit activities in Eastern Europe. The consensus among my colleagues, professors from other universities, and experts from design houses was that a local SSCS chapter would

help to support SSCS's 30 members in Romania and foster a stronger connection between the academic and industrial circuit design research communities and the Romanian EDS Chapter. With the encouragement of Professors Jan Van der Spiegel, SSCS Chapter Chair, and Cor Claeys, EDS President, I formed the chapter about a year ago. It was the right moment to set up a solid-state circuits forum to enhance the influence of SSCS in the area.

Shortly afterward, I attended the first SSCS pan-European Chapter Chair Meeting in Munich on the occasion of ESSCIRC 2007, where I talked to IEEE Region 8 officials, SSCS officers and European leaders. Of great help were Professor Richard Jaeger, then SSCS President, Professor Jan Van der Spiegel, Anne O'Neill and Katherine Olstein, SSCS staff, and also Professor Cor Claeys, EDS President, and William Van Der Vort, Executive Director of EDS.

In October 2007, EDS and the emerging SSCS Chapter organized NADE- (Nanoelectronic Devices), a very well attended mini-colloquium in Sinaia reported in the EDS Newsletter of January 2008, where 15 well known international speakers presented papers on nanodevices and nanocircuits, This mini-colloquium was organized on the occasion of the 30th anniversary of the CAS-International Semiconductor Conference, the equivalent of the ESSDERC/ESSCIRC conference in Eastern Europe. A first meeting of SSCS members was also held in Sinaia. The chapter was subsequently approved by SSCS, IEEE Region 8 and RAB, thanks to. the prompt help of Jean Gabriel Remy, Region 8 Director and Professor Willy Sansen, SSCS President.

The new SSCS-Romania Chapter will respond to the interests and needs of the local industrial and academic communities: Universities with advanced research topics in IC design are spread all over Romania. In the past ten years, many design houses have been established and their number is expected to increase. The short range goals of the chapter include:

- inviting distinguished lecturers to local technical events;
- co-sponsoring local conferences, workshops and seminars;
- increasing the number of SSCS members;
- fostering collaboration and the cross fertilization of ideas among SSCS and ED members;
- paying special attention to SSCS student activities to fulfill the needs of the already demanding IC circuit and system design national labor market.

In the long run, the new SSCS chapter is expected to increase the visibility of IEEE and SSCS in Romania and to consolidate its contacts with the international scientific communities.

Romania's origins in semiconductor devices and ICs, both in academic/research and design/manufacturing predates 1960. At the beginning of the 1960's, a synergetic interaction between the already-consolidated academic track and the newly launched semiconductor industry took place. A semiconductor school was founded in Romania by Professor Mihai Draganescu, a brilliant visionary who wrote a fundamental book on Electronic Processes in Semiconductor Devices and Circuits in 1962. It was a natural out growth of the electronics and telecommunications school established before the second world war by Professor Tudor Tanasescu, and of the Faculty of Electronics and Telecommunications at the University Politehnica of Bucharest, established in 1953. There has always been a close two-way interaction between academia, research and industry; Professor Roman Stere was CTO of the first foundry in Romania. Professor Draganescu founded ICCE, a semiconductor research institution which continues today as the National Institute of Microtechnology. Many generations of local semiconductor college graduates are now spread all around the world.

About the Author

Marcel D. Profirescu graduated from the Electronics and Telecommunications Department of the University Politehnica of Bucharest in 1964 and received a Ph.D. from University College, London in 1974. He teaches Electronic Devices and Circuits and TCAD, and heads two research centers in Micro and Nanoelectronics, respectively in ICT, and a Microelectronic Design company in Bucharest. Dr. Profirescu is an IET Fellow, IEEE Senior Member nominated for FIEEE, EDS Distinguished Lecturer, ED and SSCS Romania Chapters Chair, the EDS SRC Vice Chair for Europe, Africa and Middle East and the ED/LEO South Africa Chapter Partner.

SSCS AdCom Endorses Newsletter-Magazine Conversion in Summer Meeting

ISSCC Task Force Previews Ground-Breaking Initiatives

Katherine Olstein, SSCS Administrator, k.olstein@ieee.org

In a formal motion at its biannual meeting on 19 August, 2008 in San Francisco, the SSCS AdCom endorsed the tone, scope, administrative structure, and budget of the IEEE Solid-State Circuits Magazine approved by the IEEE Technical Activities Board (TAB) in June. It also heard a work in progress report from the ISSCC 2020 Task Force.

Launching in January 2009 as an official migration of the SSCS Newsletter, which had already grown into a magazine, the IEEE Solid-State Circuits Magazine will have formal Editorial and Advisory Boards and expand upon the SSCS News with the addition of regional Associate Editors, Technology Surveys, and Tutorials. For more information about the conversion of the SSCS News into the Solid-State Circuits Magazine, please read Anne O'Neill's Executive Director column on page 7 of this issue.

SSCS Staff Honored

SSCS Executive Director Anne O'Neill and SSCS Administrator Katherine Olstein were honored at the AdCom's Executive Committee meeting on 19 August, 2008 for the excellence of their work on the Society's enhanced newsletter and their vision during its conversion to Magazine status.

SSCS Past President Richard C. Jaeger (left) and President Willy Sansen presented SSCS Executive Director Anne O'Neill (third from left) and Administrator Katherine Olstein with plaques in recognition of their work on the SSCS News and magazine migration.

At the meeting, Ms. O'Neill was presented with a plaque by President Willy Sansen and Past President Dick Jaeger citing her foresight and leadership:

"The SSCS AdCom recognizes the outstanding vision and leadership of Anne O'Neill in the elevation of the SSCS Newsletter to a Magazine. Her experience and coordination among IEEE staff and volunteers throughout the world have been crucial to the continuing development of the publication."

Ms. Olstein was presented with a plaque recognizing her attention to detail and outstanding management of the SSCS News:

"The SSCS AdCom recognizes the outstanding execution and attention to detail of Katherine Olstein in the elevation of the SSCS Newsletter to a Magazine. Her acquisition of Society news, editing, and interactions with authors, volunteers, and the IEEE staff has been crucial to the continuing development of the publication."

It is wonderful to work with both Anne O'Neill and Katherine Olstein as we migrate the SSCS News to the IEEE Solid-State Circuits Magazine, debuting in Winter 2009.

Mary Yvonne Lanzerotti,
Editor-in-Chief

ISSCC Task Force Proposes Far-Seeing Innovations

Commissioned in 2007 to build a long-term vision for the conference, the ISSCCC 2020 Task Force has focused on broadening the conference venue beyond San Francisco and on migrating print materials to electronic formats, beginning with the conference digest.

Satellite Conference Program To Maximize Global Attendance and Minimize Travel Costs

According to Task Force spokesman Dennis Monticelli, ISSCC has been structured for nearly half a century as a must-attend yearly event in San Francisco in February. The new satellite conferences are envisioned as a set, or sets, of regional events, each built around a collection of outstanding ePapers, and an eDigest from the mother conference, with locally determined forums, workshops, and social events, and a locally-determined admissions policy and business model tailored to the needs of the specific region.

The satellite program promises to "differentiate ISSCC from the crowd" in the 21st century," said

Monticelli. Four SSCS chapters in Asia selected as beta sites for early March 2009 will be "a litmus test for delivering our value to emerging regions," he said. SSCS Taskforce members are Willy Sansen, C.K. Wang, Anantha Chandrakasan, Yoshi Hagihara, and Nicky Lu. Details about the ISSCC Satellite program will be reported in the new Solid-State Circuits Magazine and Society emails, and on the SSCS website.

In an additional AdCom announcement, Awards Committee Chair John C. Corcoran reported that elected AdCom member Tom Lee has agreed to serve as the Society's representative to the National Inventors Hall of Fame, which will rank nominees for recognition in 2009, the 50th anniversary of the integrated circuit.

CEDA Currents: IEEE/ACM MEMOCODE Contest Update

Patrick Schaumont, Virginia Tech, Krste Asanovic, UC, Berkeley, James C. Hoe, Carnegie Mellon University

The second annual IEEE/ACM-MEMOCODE Hardware-Software Codesign Contest concluded successfully on 9 March, 2008. This annual contest was conceived for the ACM-IEEE International Conference on Formal Methods and Models for Codesign (//memocode-conference.com)to help highlight the issues distinct to hardware-software codesign and to expand the conference's emphasis on design and practice. On 8 February, 2008, a "secret" design problem involving the AES (Advanced Encryption Standard) algorithm and sorting was revealed on the contest website. Contestants were given one month to produce working hardware-software codesigned solutions, which would be judged on the basis of performance and elegance of design. Eleven finalists successfully completed the design, from 27 original teams drawn from diverse geographic regions in the US, Europe, and Asia. A panel of judges evaluated the final design entries, and the winners were formally announced at this year's MEMOCODE on 5-7 June, 2008 in Anaheim, California, which was collocated with the Design Automation Conference (DAC).

This year's contest will award two $1,000 cash prizes in the categories of the Highest Performance Design and the Most Efficient Design. In addition, Xilinx is sponsoring a special $1,000 cash prize for the best entry employing a high-level design methodology. Along with the three of us (who organized this year's contest), the panel of judges also includes Kees Vissers (Xilinx) and Satrajit Chatterjee (Intel). This year's contest is sponsored by Nokia, Xilinx, Bluespec, and CEDA. To see a description of the design problem and the contest rules, go to rijndael.ece.vt.edu/memocontest08. For more information, please contact Patrick Schaumont schaum@vt.edu).

CEDA Honors Richard Brayton

CEDA hosted a luncheon on 10 June, 2008 at this year's DAC to honor Robert Brayton, winner of the 2007 Phil Kaufman Award, for his impact on the field of electronic design through contributions in EDA. Brayton gave a lecture highlighting his career path and challenges, and shed light on some of the turning points he has witnessed while working in industry and academia. In addition to this lecture, EDA award recipients (IEEE Fellow, IEEE Technical Field Awards, and others) were recognized for their accomplishments.

IEEE Annual Honors Ceremony

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prestigious event, recognizes exceptional contributions that have made a lasting impact on technology, society, and the engineering profession. The program honors achievements in industry, research, education, and service. Seventeen institute-level award recipients were recognized at this year's ceremony, which was held on 20 September, 2008 in conjunction with the IEEE Sections Congress in Quebec, Canada.

This year's IEEE Honors Ceremony started at 6:00 pm, with a dinner and afterglow reception immediately following. The event was hosted by 2008 IEEE President and CEO Lewis Terman. The theme was "Innovating to Meet the World's Challenges." All those attending the Sections Congress were invited. For further information, please see 'Awards News' on the IEEE web site or contact William Joyner (william.joyner@src.org).

Perspective: NoCs and EDA Tools Improve MP SoC Designs

Many multiprocessor SoCs (MPSoCs) are used in devices where low-energy operation of the system is critical. As technology advances, wire scaling is not on par with transistor scaling. Moreover, the number of communicating components in the chip, along with their speed of operation, is increasing. Because of these factors, the communication between the cores is causing a major bottleneck for system performance and energy consumption. With architectures becoming more interconnect-dominated, achieving an energy-efficient on-chip interconnect architecture tailored to the needs of the applications running on the chip is an important challenge that designers face.

In recent years, researchers have addressed this challenge in two ways: by developing methods and CAD tools to achieve an energy-efficient design and by developing scalable micro network-based architec-tures, or simply networks on chips (NoCs). CAD tools allow an exploration of the interconnect design space early in the design cycle and automate the building of efficient application-specific interconnect architectures. The NoC paradigm results in a structured, modular interconnect design with improved performance and energy efficiency.

The main goal is to let designers explore trade-offs in interconnect design—for example, between band-width, power, reliability, and cost. State-of-the-art methods exist to solve some of the most important, time-intensive problems encountered during interconnect design, such as interconnect topology synthesis, core mapping, crossbar sizing, route generation, resource reservation, and RTL code and layout generation. Application-specific inter connect optimization can lead to significant improvements in all relevant cost metrics. Improvements by factors of 2 to 5 are not uncommon, and become even greater with technology and architectural complexity scaling. Design automation support is essential to guarantee that these custom-fit solutions can be readily deployed, tested, and verified. Although the state of maturity of these tools is not perfect, results are promising, and automated interconnect design is poised to become an essential component in energy-aware SoC design and validation flows.

Direct any questions and comments about this report to Srinivasan Murali (srinivasan.murali@epfl.ch).

Upcoming CEDA Events

IEEE CEDA currently sponsors or cosponsors ten conferences and workshops, and two additional conferences in which it is in technical cooperation with other societies. Our conferences provide excellent opportunities for those interested in learning about the latest technical trends in electronic design and automation and to being engaged with a community of volunteers. If you are interested in participating or have an idea about new topics of interest for our conferences, please contact William Joyner (william.joyner@src.org), CEDA vice president of conferences.

3rd International Conference on Nano-Networks (Nano-Net)
15-17 September, 2008, Boston
www.nanonets.org

18th International Workshop on Power and Timing Modeling Optimization and Simulation (PATMOS)
10-12 September, 2008, Lisbon, Portugal www.fpl.uni-kl.de/conferences/patmos/patmos.html

16th IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SOC)
13-15 October, 2008, Rhodes Island, Greece
//vlsi.ee.duth.gr/vlsisoc-2008

Embedded Systems Week (ESWEEK)
19-24 October, 2008, Atlanta
www.esweek.org

IEEE/ACM International Conference on Computer-Aided Design (ICCAD)
10-13 November, 2008, San Jose, California
www.iccad.com/2008/index.html

Formal Methods in Computer Aided Design (FMCAD)
17-20 November, 2008, Portland, Oregon
//es.fbk.eu/events/fmcad08

CEDA Currents is a publication of the IEEE Council on Electronic Design Automation. Please send contributions to Jose Ayala (jayala@fdi.ucm.es) or Anand Raghunathan (anand@nec-labs.com).

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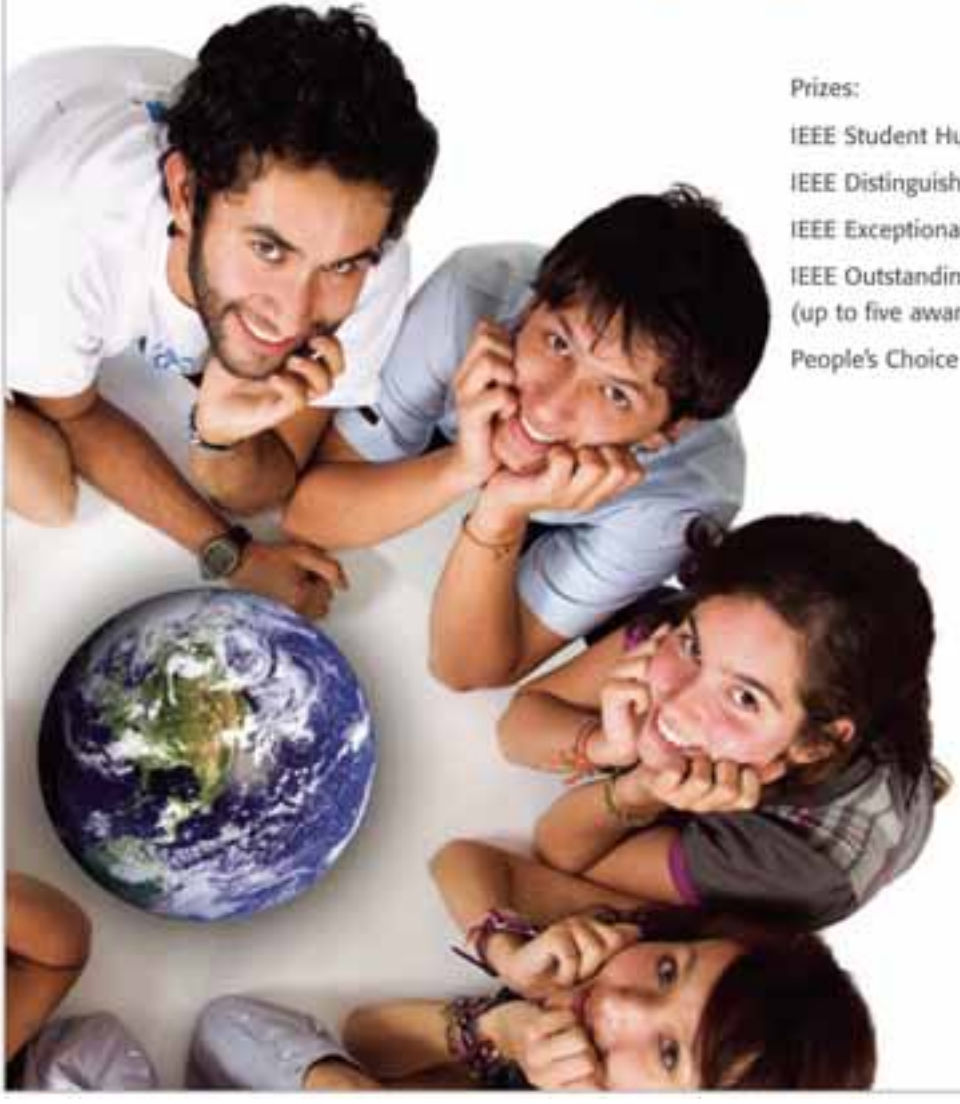

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Kalman Filtering
Theory and Practice Using MATLAB, 3rd Edition

Mohinder S. Grewal

9780470173664 • Cloth • 576pp • $110.00 • August 2008
Wiley-IEEE Press

This third edition successfully provides readers with a solid introduction to the theoretical and practical aspects of Kalman filtering. Authors Grewal and Andrews draw upon their decades of experience to offer an in-depth examination of the subtleties, common problems, and limitations of estimation theory as it applies to real-world situations. They present many illustrative examples drawn from an array of application areas including GNSS-aided INS, the modeling of gyros and accelerometers, inertial navigation, and freeway traffic control.

FPGA Prototyping By Verilog Examples

Pong P. Chu

9780470185322 • Cloth • 488pp • $84.95 • June 2008
Wiley

FPGA Prototyping by Verilog Examples utilizes a "learn by doing" approach to introduce the concepts and techniques of Verilog and FPGA to designers through a series of hands-on experiments. This book provides a collection of clear, easy-to-follow templates for quick code development and a large number of practical examples to illustrate and reinforce the concepts and design techniques. Although the book is an introductory text, the examples are developed in a rigorous manner and the derivations follow strict design guidelines and coding practices used for large, complex systems.

Nano-CMOS Design for Manufacturability
Robust Circuit and Physical Design for Sub-65nm Technology Nodes

Ban P. Wong, Anurag Mittal, Greg W. Starr, Franz Zach, Victor Moroz, Andrew Kahng

9780470112809 • Cloth • 408pp • $94.95 • October 2008
Wiley

This book examines the challenges that design engineers face in the nano-scaled era, such as exacerbated effects and the proven design for manufacturability (DFM) methodology in the midst of increasing variability and design process interactions. In addition to discussing the difficulties brought on by the continued dimensional scaling in conformance with Moore's law, the authors also tackle complex issues in the design process, including the use of a functional first silicon to support a predictable product ramp. Real-world examples simplify complex concepts, helping readers see how they can successfully handle projects.

Microprocessor Theory and Applications with 68000/68020 and Pentium

Mohamed Rafiquzzaman

9780470380314 • Cloth • 576pp • $125.00 • August 2008
Wiley

This self-contained book includes a number of basic topics and assumes a basic digital logic background. The author has chosen to emphasize the characteristics and principles common to typical microprocessors. He demonstrates the basic microcomputer interfacing techniques via examples using the simplest possible devices such as switches, LEDs, A/D converters, hexadecimal keyboard, and seven-segment displays. This book is an ideal textbook for undergraduate and graduate-level courses in electrical engineering, computer engineering, and computer science. (An instructor's manual is available upon request.)

Understanding Lasers
An Entry-Level Guide, 3rd Edition

Jeff Hecht

9780470088906 • Paper • 478pp • $69.95 • May 2008
Wiley-IEEE Press

Updated to reflect advancements since publication of the previous edition, *Understanding Lasers, Third Edition* offers an introduction to lasers and associated equipment at a level that nontechnicians can fundamentally understand. The author focuses on real-world lasers and assumes only a minimal background in algebra, making the book a practical, easy-to-follow guide for a broad audience. Topics covered include: optics and laser accessories, semiconductor diode lasers, gas lasers, low-power laser applications, solid-state and fiber lasers, high-power laser applications, and more.

RF Measurements for Cellular Phones and Wireless Data Systems

Allen W. Scott, Rex Frobenius

9780470129487 • Cloth • 504pp • $110.00 • June 2008
Wiley-IEEE Press

Covering all topics needed to effectively test radio frequency (RF) components and systems for cell phones and wireless data systems, this guide balances practical real-world information with relevant theory. It summarizes basic RF principles before describing the digital technology used in cell phones and wireless data systems. Methods and equipment used in mass testing of components during manufacturing also receive detailed treatment. Industry professionals building, installing, and maintaining cell phone and wireless equipment, as well as advanced students will find this guide useful.

Electromagnetic Shielding

Salvatore Celozzi, Rodolfo Araneo, Giampiero Lovat

9780470055366 • Cloth • 376p • $84.95 • April 2008
Wiley-IEEE Press

This reference provides a comprehensive survey of options for the reduction of the electromagnetic field levels in prescribed areas. After an introduction and an overview of available materials, it discusses figures of merit for shielding configurations, the shielding effectiveness of stratified media, numerical methods for shielding analyses, apertures in planar metal screens, enclosures, and cable shielding.

Advanced Design Techniques and Realizations of Microwave and RF Filters

Pierre Jarry, Jacques Beneat

9780470183106 • Cloth • 304pp • $115.00 • June 2008
Wiley-IEEE Press

This book provides readers with the knowledge and skills to design and realize microwave and RF filters, as well as the numerous approaches for solving the filter design problem. Each chapter concerning the design of a microwave filter starts with a characterization of the elements in the microwave structure. Choices and assumptions leading to each design technique are explained in some detail. This approach gives readers a better understanding of how the design technique came about, so that they will be able to propose modifications to suit their own needs.

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www.a-sscc.org/
3-5 November, 2008
Fukuoka, Japan
Contact: Secretariat of A-SSCC2008
E-mail: *A-SSCC2008@ics-inc.co.jp*

2009 ISSCC International Solid-State Circuits Conference
www.isscc.org
8– 12 February 2009
San Francisco, CA, USA
Paper deadline: 22 Sept. 2008
Contact: Courtesy Associates,
ISSCC@courtesyassoc.com

2009 Symposium on VLSI Circuits
www.vlsisymposium.org
16-18 June, 2009
Paper deadline: 14 Jan 2009
Contact: Phyllis Mahoney, *phyllism@widekehr.com*

2009 Organic Microelectronics Workshop
www.mrs.org
July 6-9, 2009
San Francisco, CA 94103
Contact: Edwin A. Chandross,
eac@materialschemistry.com

2009 Custom Integrated Circuits Conference
www.ieee-cicc.org/
20–22 September 2009
San Jose, CA, USA
Paper deadline: TBD
Contact: Ms. Melissa Widerkehr,
Conference Manager *cicc@his.com*

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Sensors Conference
www.ieee-sensors2008.org
26-29 October 2008
Lecce, Puglia, Italy
Paper due date : Passed
Contact: *Info@ieee-sensors2008.org*

2008 International Conference on Computer Aided Design (ICCAD)
www.iccad.com/
9-13 November 2008
San Jose, CA
Paper due date : Passed
Contact: Kathy MacLennan, Conference Manager
kathy@mpassociates.com

Conference on VLSI Design
vlsiconference.com/vlsi2009/
5-9 January 2009
New Delhi, India
Paper Deadline: Passed

IEEE International Conference on Microelectronic Test Structures
www.see.ed.ac.uk/ICMTS/
30 Mar – 2 Apr 2009
Oxnard, CA
Paper Deadline: Passed
Technical Chairman: Richard Allen
richard.allen@nist.gov

Design Automation and Test in Europe (DATE) 2009
www.date-conference.com/
20-24 April 2009
Paper Deadline: Passed
Nice, Alpes-Maritime, France

VLSI -TSA/DAT
vlsitsa.itri.org.tw/2009/General/
27-30 April 2009
Hsinchu, Taiwan
Paper deadline: 18 Oct 2008
VLSI-TSA Contact : Clara Wu
vlsitsa@itri.org.tw
VLSI-DAT Contact: Ms. Elodie HO *vlsidat@itri.org.tw*

2009 Radio Frequency Integrated Circuits Symposium
www.rfic2009.org/
7-9 June 2009
Boston, MA
Paper deadline: 6 Jan 2009
Contact: Larry Wicker, *lrwassoc@carolina.rr.com*

2009 Design Automation Conference
www.dac.com
27-31 July 2009
San Francisco, CA
Paper deadline: 19 Nov 2008
Contact: Kevin Lepine, Conference Manager
kevin@dac.com

Hot Chips
www.hotchips.org
August, 2009
Stanford, CA

ISLPED International Symposium on Low Power Electronics and Design
www.islped.org/
2009 Date TBD
Contact: Diana Marculescu,
dianam@ece.cmu.edu

2009 IEEE Integrated Circuit Ultra-Wide Band ICUWB
www.icuwb2009.org
9-11 Sep 2009
Vancouver, Canada
Paper deadline: 23 Feb 2009
Contact: Lutz Lampe, Chair, *lalmpe@ece.ubc.ca*

ESSCIRC/ESSDERC 2009- 39th European Solid State Circuits/Device Research Conferences
www.esscirc2007.org
14 - 18 Sep 2009
Athens, Greece
Abstract deadline: 4 Apr 2009
Contact Cor Claeys, IMEC, *cor.claeys@imec.be*

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