SSCS
IEEE SOLID-STATE CIRCUITS SOCIETY NEWS
Winter 2008 Vol. 13, No. 1 www.ieee.org/sscs-news

The DRAM Story

with articles by Dennard, Itoh, Koyanagi, Sunami, Foss and Isaac

Editor's Column

Welcome to the Winter, 2008, issue of the Solid-State Circuits Society Newsletter! We appreciate all of your feedback on our first year of issues presenting The Technical Impact of Moore's Law, The Impact of Dennard's Scaling Theory, The 40th Anniversary of Amdahl's Law, and Barrie Gilbert: The Gears of Genius. Thank you for supporting our efforts!

The goal of each issue is to be a self-contained resource with background articles (that is, the 'original sources') and new articles by experts who describe the current state of affairs in technology in view of the impact of the original papers and/or patents.

This issue contains one Education Highlights article:

"Turning Students On to Circuits," by Yannis Tsividis of Columbia University in New York City, NY.

The theme of the issue is "The DRAM Story with new articles by Dennard, Itoh, Sunami, Koyanagi, Isaac and Foss," discussing the evolution and current status of DRAM:

(1) "Revisting 'Evolution of the MOSFET Dynamic RAM-A Personal View'" by Robert Dennard (IBM);
(2) "The History of DRAM Circuit Designs - At the Forefront of DRAM Development" by Kiyoo Itoh (Hitachi Ltd);
(3) "Stacked Capacitor DRAM Cell and Three-Dimensional Memory" by Mitsumasa Koyanagi (Tohoku University);
(4) "The Role of the Trench Capacitor in DRAM Innovation" by Hideo Sunami (Hiroshima University);
(5) "The Remarkable Story of the DRAM Industry" by Randy Isaac, retired Vice President (IBM);
(6) "DRAM - A Personal View" by R. C. Foss, retired Chairman of the Board and Founder (MOSAID Technologies Incorporated).

In addition, the issue includes reprints of two original papers and an original patent:

(1) R. H. Dennard, "Evolution of the MOSFET Dynamic RAM - A Personal View," IEEE Transactions on Electron Devices, vol. ED-31, No. 11, November, 1984, pp. 1549-1555.
(2) R. H. Dennard, "Field-Effect Transistor Memory," Patent 3,387,286, June 4, 1968.
(3) K. Itoh, "In Quest of the Joy of Creation," in "Innovate the Future," 2005 Hitachi Hyoron Special Edition, pp. 34-39, Hitachi Hyoronsha, Tokyo, Japan.

Thank you for taking the time to read the SSCS News. We appreciate all of your comments and feedback! Please send comments to myl@us.ibm.com.

IEEE Solid-State Circuits Society AdCom

President:
Willy Sansen
K. U. Leuven
Leuven, Belgium
willy.sansen@esat.kuleuven.be
Fax: +32 16 321975

Vice President:
Bernhard Boser
University of California
Berkeley, CA

Secretary:
David A. Johns
University of Toronto
Toronto, Ontario, Canada

Treasurer:
Rakesh Kumar
Technology Connexions
Poway, CA

Past President:
Richard C. Jaeger
Alabama Microelectronics Center
Auburn University, AL

Other Representatives:
Representative to Sensors Council
Darrin Young
Representative from CAS to SSCS
Domine Leenaerts
Representative to CAS from SSCS
Un-Ku Moon

Newsletter Editor:
Mary Y. Lanzerotti
IBM T.J. Watson Research Center
myl@us.ibm.com
Fax: +1 914 945 1358

Associate Editor for Europe/Africa:
Tony Harker
ISLI Alba Centre Alba Campus
Livingston Scotland EH54 7EG
tony.harker@sli-institute.ac.uk

Elected AdCom Members at Large
Terms to 31 Dec. 08:
Wanda K. Gass
Ali Hajimiri
Paul J. Hurst
Akira Matsuzawa
Ian Young
Terms to 31 Dec. 09:
John J. Corcoran
Kevin Kornegay
Hae-Seung (Harry) Lee
Thomas H. Lee
Jan Van der Spiegel
Terms to 31 Dec. 10:
Terri S. Fiez
Tadahiro Kuroda
Bram Nauta
Jan Sevenhans
Mehmet Soyuer

Region 8 Representative:
Jan Sevenhans

Region 10 Representative:
C.K. Wang

Chairs of Standing Committees:

Awards	John J. Corcoran
Chapters	Jan Van der Spiegel
Education	C.K. Ken Yang
Meetings	Bill Bidermann
Membership	Bruce Hecht
Nominations	Stephen H. Lewis
Publications	Bernhard Boser

For detailed contact information, see the Society e-News: *www.ieee.org/portal/site/sscs*

For questions regarding Society business, contact the SSCS Executive Office.

Contributions for the Spring 2008 issue of the Newsletter **must be received by 8 February 2008** at the SSCS Executive Office. A complete media kit for advertisers is available at www.spectrum.ieee.org/mc_print. Scroll down to find SSCS.

Anne O'Neill, Executive Director
IEEE SSCS
SSCS-West: 1500 SW 11th Ave. #1801
Portland, OR 97201
Tel: +1 732 981 3400
Fax: +1 732 981 3401
Email: sscs@ieee.org

Katherine Olstein, SSCS Administrator
IEEE SSCS
445 Hoes Lane,
Piscataway, NJ 08854
Tel: +1 732 981 3410
Fax: +1 732 981 3401
Email: k.olstein@ieee.org

SOLID-STATE CIRCUITS SOCIETY

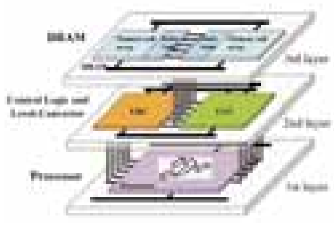
Where ICs are in IEEE

Winter 2008 Volume 13, Number 1

Photo by Michiko Sunami. From left, Kiyoo Itoh, Hideo Sunami, Robert H. Dennard, Mitsumasa Koyanagi.

EDUCATION HIGHLIGHTS

TECHNICAL LITERATURE



40

60

PEOPLE

62

CONFERENCES

75

CHAPTER NEWS

81

NEWS

President's Message

Richard C. Jaeger, Auburn University, jaeger@eng.auburn.edu

My two-year term as President of the IEEE Solid-State Circuits Society is nearly at an end. Thanks to the efforts of our membership, staff, and volunteers, the Society continues to strengthen and expand its international activities. Our conferences are attracting record numbers of paper submissions and attendees. The Journal of Solid-State Circuits sees strong submissions, and the Journal's papers continue to have some of the highest download rates from IEEE Xplore. The number of SSCS chapters and their activities are at a record level. By the end of 2007, SSCS financial reserves are also projected to be at a record level.

We all should be thankful for the exceptional efforts of Anne O'Neill, Executive Director of the Society, and Katherine Olstein, SSCS Administrator, who ensure smooth day-to-day operation of the society and support the President in ways that are too many to enumerate. I thank Past President Steve Lewis for his always considered advice and insight, and I also want to acknowledge the many contributions of the members of our Administrative Committee and Subcommittees. Finally, the past two years have seen outstanding development of the content of the Newsletter through the hard work of Anne, Katherine and technical Editor, Mary Lanzerotti.

As of January 1, 2008, Willy Sansen, Professor at KU Leuven, Belgium, and Director of ESAT-MICAS, becomes SSCS President. Professor Sansen is well known internationally for his work in analog circuits and has been involved with a wide range of SSCS activities including Society Vice President and Chair of the 2002 ISSCC.

Our Society will be in good hands under Willy's leadership.

Richard C. Jaeger

Outgoing President

New Recruit to the SSCS Editorial Team

Tony Harker, ISLI Alba Centre, tony.harker@sli-institute.ac.uk

Hello Everyone

As the newest recruit to the SSCS News Editorial team, I'd like to introduce myself and give you some ideas about the subject areas I will be addressing in future issues.

I am Tony Harker, Chief Executive of the Institute for System Level Integration (ISLI) in Livingston, a town situated between Scotland's capital city, Edinburgh, and its largest city, Glasgow. Livingston has been home to a number of electronics companies since the 1970s and is commonly known as Silicon Glen.

ISLI positions itself as a bridge between academic and commercial worlds, promoting and encouraging technology transfer and collaborative research. One of our main charters is the provision of postgraduate education with our partners – the informatics, computing science and electronic engineering departments of the Scottish universities of Edinburgh, Glasgow, Strathclyde and Heriot Watt. Academic staff from each institution work together to support, supervise and deliver Master's and PhD--level programmes at our campus in Livingston.

ISLI also has its own research group specialising in integrated silicon MEMS, and a design group, which hold widely ranging engineering skills and whose primary aim is to help promote technology transfer between academia and industry. This is a considerable challenge in itself bearing in mind the frequently diverse driving factors within each sphere.

The massive changes to the semiconductor industry witnessed over the past decade have left few unscathed. The UK's electronics industry, including ISLI, has been required to respond and adapt, faced with reduced inward investment from multinationals. Indeed the apparent new world order of fabless suppliers, linked to the mega-foundries, plus the rise of small and medium-sized enterprises (SMEs) are filling gaps and providing a new level of challenges to those tasked with supporting their endeavours.

Such phenomena are not simply UK or Europe-wide. The constant drive for cost-effective development, the quest for competitive margins, the need to maintain innovation, and the availability of a highly educated workforce will continue to drive the commercial world at an aggressive pace. The challenge to us all is how we maintain an adaptable and scaleable response to these market needs.

The trend towards globalisation of resource, the high cost of embarking on advanced design on the crest of the silicon wave, time-to-market pressures, and the inherent need to mitigate the large and diverse risks (more than anything due to the cost of failure), present a plethora of challenges requiring engineers to think more laterally than ever before. Gone are the days of compartmentalised, isolated designers; nowadays design engineers working with Silicon need to wear many different hats, as well as embrace ideas from mechanical or chemical engineering environments and the world of business.

The pervasive nature of electronics, and its clear underpinning of almost all of our leisure and business lives, accelerates the need to cross-pollinate with other engineering disciplines. Recent examples of this include the integration of MEMS technologies with CMOS control circuits and the addition of RF to sensing platforms in the medical world. Huge leaps in available computing power, offered by ever greater integration in faster and smaller technologies, continues to open avenues for product consolidation and innovative development. Massive digital processing capability coupled with advanced analogue blocks for human interfacing within innovative encapsulation is the very basis for many of the devices we now take for granted. (If anyone needs evidence of this just look at the cell phone in your pocket!)

Perhaps most importantly, we must not forget the urgent need to harness new energy sources through innovative scavenging techniques. These, coupled with smart and efficient energy management systems, will help form the backbone of new development in portable products in the coming decade.

Topics such as these, plus associated challenges in supporting diverse markets, geographical dispersion of development resources, new and emerging players, and key driving technologies, will form the backbone of my plans for articles throughout the coming year as I explore the vital areas for a successful symbiotic relationship between academia and industry.

I sincerely hope you enjoy my musings and welcome any feedback you may have.

Best regards

Tony Harker
Associate Editor of
Europe/Africa
www.sli-institute.ac.uk
Tel: +(44) 1506 469 300
Fax + (44) 1506 469 301

Tony Harker graduated from Northumbria University (formerly known as Newcastle Upon Tyne Polytechnic) with a degree in Physical Electronics in 1983. After graduation, he moved to Scotland and took up a product engineering role with National Semiconductor at Greenock. During his time with National, Tony moved into IC design, working in a small group of engineers in full custom and standard cell telecom development for the Ethernet market.

After a move to Fujitsu's ASIC design group in Manchester, England in 1989 Tony spearheaded advanced layout techniques in leading edge silicon processes with his team, and introduced the concept of IP-based design and development. This culminated in a hugely successful 25+ ASIC-based system project for a major European telecom customer.

Tony joined Cypress Semiconductor in 2000 to run the UK full custom design centre. Specialising in global technology, project and product management, he rose to become Programme Director before leaving in 2005 to run the Institute for System Level Integration, In his time at ISLI, Tony has enhanced the commercial face of the organisation, increasing its international profile and its interaction with the UK design community.

In his spare time, Tony enjoys spending time with his family, dogs and horse and also the outdoor life being a keen angler and field sports participant.

Turning Students On to Circuits

By Yannis Tsividis, Department of Electrical Engineering, Columbia University New York, NY, tsividis@ee.columbia.edu

When one compares today's students to those of earlier generations, the differences are striking. Yet the way most of us teach has essentially remained unchanged since the middle of the past century. No wonder, then, that our students are not attracted to electrical engineering or, among those who are, many are disappointed and just drag along, or even drop out. In this article we discuss what can be done to turn things around. Parts of this article draw on an earlier one on an introductory EE class [1].

Today's students

Today's students differ from those of older generations in several respects [2]:

1. *They have not tinkered.* Thus, if they get started in EE through the conventional circuit analysis class, they have no idea where, in practice, all the theory fits and why it is needed. In the past, many students had tinkered and could see why the theory they were being taught was useful. This provided motivation, which is missing today.

2. *They are impatient.* Today's students are used to immediate gratification (exemplified by their obsessive playing of computer games, where they push a button and see "major results" right away). Telling these students that they "will see later in the curriculum" why circuit analysis is useful, does not work; two semesters down the road, or even one, is too far into the future for them. Thus they lose motivation, develop frustration and many become passive learners.

3. *They think that software is everything.* Being members of the computer games generation, today's students relate to the computer screen extremely well. This is good, but also has a negative side: Students tend to develop the impression that all that needs to be done is press keys, and somebody else, somewhere, will take care of designing and building the hardware.

In view of the above generational differences, it does not make sense to keep teaching students using techniques that were appropriate half a century ago. Doing so risks losing some of the best minds, or at least turning them off as far as circuits are concerned.

Efforts to turn things around

Several attempts to turn things around have been made in recent years at several universities, all involving a laboratory. Many universities have tried a software-oriented first lab; this can be about multimedia, or it can use software packages as aids to teach signal processing or control systems. This approach can provide immediate gratification, but it fails to address problems #1 and #3 above; in fact, it reinforces #3. If the first engineering courses students see are software-oriented, by the time they get to hardware it is too late to make them relate to it well. What is needed is a course with real contact to the real world, using a real (not a virtual) laboratory. Our chance to do something, before the students get turned off with circuits, is the first circuits lab.

Approaches to the first circuits lab

About ten years ago, we noticed a worrying downward trend in our enrollment; more and more engineering students were opting for different departments. We looked into this problem, and found that its cause was the fact that we were not addressing the needs of today's students, as outlined above. A key problem was our first circuits lab, which was run the classical way: it involved dry instructions which served to teach measurement techniques and to verify the theory. This reinforced the general impression out there that engineering is not fun, and failed to motivate students. It also did not allow them to be creative. In other words, our first circuits lab was wasting a unique opportunity to excite today's students about electrical engineering in general, and circuits in particular. We decided to turn things around; we begun by looking at approaches elsewhere that departed from the classical approach.

One approach we saw was to run the lab concurrently with a theory class, and have students gradually build a large system, usually based on a kit, with the end result achieved at the end of the term. This approach is certainly better than the classical one as far as motivation is concerned. Unfortunately, we did not find it easy to make such a lab compatible with the order in which we wanted to present the theory in class; this would have required tight coordination between different instructors, who in fact changed from year to year, and was not practicable. Even if we offered this lab in the semester following the theory class, the need to tie all individual experiments to one specific application was over-constraining for our purposes; we did not find this the best vehicle for illustrating the many different concepts in our first circuits class.

In another approach elsewhere students assembled simple circuits using kits, before they had a theory class or, in some cases, with accompanying short lectures[1]. However, we could not afford to introduce an extra term of circuits in order to accommodate this approach, since in our curriculum, as in those elsewhere, circuits classes had already been squeezed into a small number of terms. And, such a class could not replace a classical circuits class; although the "light lab" approach can be fun and can serve a useful purpose, for us it did not adequately relate practice to theory, and was not a substitute for a real teaching lab.

A teaching lab that excites and motivates

Following our study of the alternatives, we set out to create a lab that would retain their advantages without their drawbacks. From the beginning, our goal was to do this in a most general way, so that hopefully our approach would stand a chance of being adopted elsewhere as well. It soon became evident that the best solution was a mix of the modern and the classical. Our goal was to get the students to tinker while understanding the links of practice to theory, and to provide them with rewarding lab experiences that would excite and motivate them. The lab we ended up with has the following features:

Experiment independence: We found that it is best at this level to keep the experiments largely independent (as opposed to their being part of a larger construction project culminating at the end of the term). In this way we had great flexibility in designing the experiments, in order to reinforce certain important concepts. This makes the lab compatible with a variety of curricular formats used at various institutions. The experiments are as follows:

1. Measuring DC voltages and currents
2. Simple DC circuits; resistors and resistive sensors
3. Generating, observing and hearing time-varying signals
4. Basic characteristics of op amps and comparators
   D1. Mini design project
5. Amplifier design using op amps; a sound system
6. RC circuit transients; more on measurement techniques
7. Filters, frequency response, and tone control
8. LC circuits, resonance, and transformers
9. Diodes and their applications
10. Modulation and radio reception - Final design project
    D2. Final design project

The above experiments can be done based on knowledge provided in any “Circuits 101” class, except for the diodes, which are fully covered in the lab manual. Diodes are introduced for two reasons: They drive the point home that not everything in circuits is linear; and they make for interesting experiments, such as radio reception, that help reinforce other topics. The experiments involving diodes can be skipped if desired.

The following experiments are included in the manual, and can be used, along with some of the above, in electronics classes or in classes that mix circuits with electronics:

11. MOSFET characteristics and applications
12. Principles of amplification using MOSFETs
13. Bipolar transistors and amplifiers
14. Digital logic circuits; gates and latches
15. D flip-flops and shift registers
16. JK flip-flops and ripple counters

Extra equipment: In addition to the usual oscilloscope, signal generators, multimeters, and power supplies, a few more pieces of equipment are an integral part of the lab stations: a microphone, a CD/MP3 player, a small power amplifier, and a loudspeaker. See Fig. 1.

Fig. 1. Audio in the first circuits lab. A microphone, a CD/MP3 player, a small power amplifier, and a loudspeaker are standard equipment in each station.

Emphasis on reality: The lab reinforces the point that everything the students do in it is real and useful, by helping them relate what they measure to their senses. Thus for example, they do not just observe waveforms on the oscilloscope screen, but also hear them through a power amplifier. They do not obtain these waveforms only from a signal generator; instead, using a microphone, they observe the waveforms of their voice, whistling, and clapping. They are even asked to remove the loudspeaker’s panel, feel the vibrations of the speaker’s cone for various frequencies and amplitudes, and finally lay the speaker flat, remove its front panel, and observe how a small particle bounces when placed on the vibrating cone. This may sound overdone, but those of us who where hobbyists at a young age know that such experiences stay in memory, and help make things click; they help students relate to their experiments, increase intuition, and motivate further study.

Emphasis on applications: Because the experiments are largely independent, many different types of applications could be woven into them. For example, in Experiment 2 on resistors, we take the opportunity to introduce resistors that are sensitive to temperature (thermistors) and light (photoresistors). Thus, sensors are introduced very early on. Students see more transducers (microphones and loudspeakers) in Experiment 3. In Experiment 4 they see yet another transducer (an LED), and they learn how to turn it on from the output of a comparator. Similarly in other experi-

---

[1] Recently, in some schools this approach has even been taken up by the students themselves [3,4]. If that does not give us the message that students are crying for a change in the way they are taught, I don’t know what will!

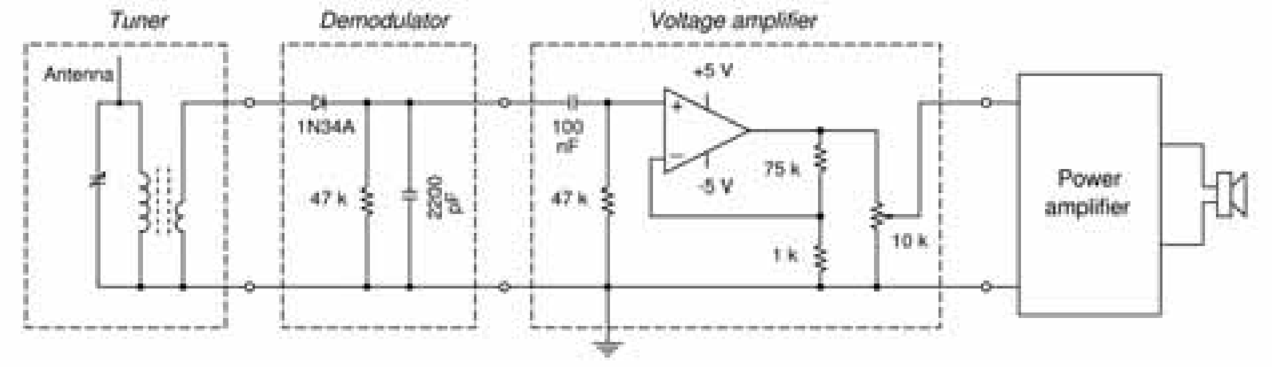


Fig. 2. RF in the first circuits lab. Before building this radio receiver, students have studied each of the three blocks shown in broken lines in separate experiments on resonant circuits, diode applications, and op amp circuits.

ments; they do not just measure the gain of an op amp/resistor amplifier, but they use it to amplify their own voice signal and listen to it. They do not just measure the frequency response of RC circuits, but apply these circuits to tone control, using them to process music from their favorite recordings stored on their iPods or CDs, and listen to the result. After having studied diodes, LC circuits, amplifiers, and their applications, they are asked to put these together to make a simple radio receiver, shown in Fig. 2. This, for them, is obviously a large system, and they can spend a couple of frustrating hours in making it work; but in the end, when they receive their first station, the effect on them is palpable. The coupling to applications also serves to motivate students to take classes in other subjects; for example, the radio receiver experiment points to classes in communications.

Design projects: Thanks to the experiment independence mentioned above, mini design projects can be introduced very early. For example, in the 5th week students are asked to come up with a specified system that does something useful, e.g. a “night lamp” that turns on when the light intensity in the room is low. We don’t tell them how to do this. After struggling for a couple of hours, and with discreet help from the TAs if needed, a spark goes on in their heads, and they realize that they can combine the knowledge they have already acquired on resistors, photoresistors, comparators and LEDs to make this task possible. This is a unique moment in their education, and it has a lasting effect on their motivation for further study in this and other classes. A much more extensive, final project completes the class. Students can choose from a list of suggested projects, or can propose their own design project.

Balance between freedom and guidance: A completely regimented approach stifles creativity and does not ensure learning; it is entirely possible for a student to blindly follow instructions and leave the lab without having really understood much. To avoid this, a certain amount of freedom must be allowed. On the other hand, complete freedom is not appropriate, as many students do not know how to begin and become stuck very often. Thus we opted for a compromise, which works best for the large majority of students. There are steps to be followed in each experiment, but parts of the story are withheld, and the students are required to search for these parts themselves. “What if” questions are used often for this purpose. For example, in Experiment 5 the students have verified that the loudspeaker converts electricity to sound. They are then asked, could the loudspeaker perhaps be used to do the opposite, i.e. convert sound to electricity? They thus have to set up an experiment to find out. This brings up in their mind the issue of energy conversion reversibility in transducers, and encourages them to experiment.

Throughout the lab, we have avoided large circuits and complicated equations, which at this stage would only serve to cloud things. There is room for those in follow-up classes and labs. In the first lab, it is best to concentrate on exciting students, giving them intuition, and making them look forward to such classes! In the end, students who have gone through this first lab tend to relate to both practice and theory better. Motivation is the key.

The experiments described above have been fine-tuned over repeated trials, and the lab now practically runs itself. The resulting manual has been published [5]. An effort has been made to make this manual appropriate for a variety of situations, and to make it easy for colleagues elsewhere to reproduce this lab. A companion Web site [6] contains detailed information on how to set up the lab, how to run it, where to get the parts, how to fool-proof the equipment, ideas for design projects, etc.

As already mentioned, before this class was introduced at Columbia, we were losing students to other departments at an alarming rate. Three years later, thanks to the introduction of this lab, our enrollment had doubled. We found that students who took this lab did better in follow-up classes, and not only ones in circuits; we attribute this to the motivational aspect of the class. Some quantitative results are given elsewhere [1]. The students’ comments, collected anonymously by the Dean’s Office and communicated to the EE department over the years, have been very positive and include “Thank you for this great experience” , “Lab very useful”, “Every department should have a class like this”, “I learned a lot and feel prepared for the rest of my major”, “Labs were great - very helpful in understanding the material”, “Labs are very helpful in familiarizing students with …the concepts from the lecture", "The lab was excellent", "The lab manual is excellent", "The lab session is great - helps you get hands on knowledge of the topics you learn", "For the first time I felt that the lab actually reinforced the subjects taught in class", and "I even...dare I say it... enjoyed... the lab portion of the class".

A variety of settings for this lab

The lab described above has been adopted in a variety of settings at several universities. For example, at Princeton it is offered concurrently with the first circuits analysis class in the sophomore year; the same for the University of Connecticut, which provides a good example of how the lab can be synchronized with lectures using a standard circuits text [7]. At San Diego State University the lab accompanies the first electronics class in the junior year. At Columbia, we run this lab as part of a first-year class in circuits and electronics. Caltech is planning to introduce this lab into their curriculum starting this fall [8].

Conclusions

Today's students can be turned on to circuits if the first lab they take is exciting and motivating. This article describes an approach to achieving this. In addition to illustrating the many concepts taught in theory classes, this approach couples experiments to applications, and encourages students to tinker and explore. We found that a proper mix of the modern and classical approaches gives excellent results. The most unambiguous indication of success for us has been seeing the students' face light up when their designs work for the first time, and hearing them say that this lab made them realize that EE is for them. Motivating students in this way is especially important in view of the recent trend towards decreasing EE enrollments.

This author would be happy to provide more details to instructors who are implementing, or are considering implementing, this lab at their own institution. He can be e-mailed at tsividis@ee.columbia.edu.

References

[1] Y. Tsividis, "Teaching circuits and electronics to first-year students", Proc. 1998 IEEE International Symposium on Circuits and Systems, vol. 1, pp. 424-427, Monterey, May/June 1998.

[2] R. A. Rohrer, "Taking circuits seriously", IEEE Circuits and Devices, vol. 6, no. 4, pp. 27-31, July 1990.

[3] "Students Create Hands-On Electrical Engineering Course", The Institute Online, http://www.theinstitute.ieee.org, 5 January 2007.

[4] "Student Branches Boost Membership with Hands-On Projects", The Institute Online, http://www.theinstitute.ieee.org, 5 October 2007.

[5] Y. Tsividis, A First Lab in Circuits and Electronics, John Wiley and Sons, New York, 2002.

[6] http://he-cda.wiley.com/WileyCDA/HigherEdTitle/productCd-0471386952.html

[7] http://www.engr.uconn.edu/ece/crsdata/210sy01.pdf

[8] Prof. A. Emami-Neyestanak, Caltech, private communication.

About the Author

Yannis Tsividis received the B.S. degree from the University of Minnesota, Minneapolis in 1972, and the M.S. and Ph.D. degrees from the University of California, Berkeley in 1973 and 1976, respectively. He is Charles Batchelor Memorial Professor at Columbia University in New York. His research has been in analog and mixed-signal MOS integrated circuits at the device, circuit, system, and computer simulation level, starting with the first fully-integrated MOS operational amplifier in 1975. A Fellow of the IEEE, he has received the 1984 Baker Prize Award for the best IEEE publication and the 2007 IEEE Gustav Robert Kirchhoff Award, and was co-recipient of the 2003 ISSCC L. Winner Outstanding Paper Award. He received Columbia's Presidential Award for Outstanding Teaching in 2003, and the IEEE Undergraduate Teaching Award in 2005.

Revisiting “Evolution of the MOSFET Dynamic RAM – A Personal View”

I am very pleased to have my 1984 paper reprinted here in this "DRAM" issue of SSCS News. It is a great honor for it to be included here with original papers from several authors who have made very significant contributions to the advancement of DRAM.

I want to explain why I wrote this paper in the first place. It was invited for the CENTENNIAL SPECIAL ISSUE of IEEE Transactions on Electron Devices, commemorating the 100th anniversary of the founding of IEEE. That was very special to be among a dozen authors chosen to describe the history and future prospects of some important developments in electronic devices. I remember that I was given very little time to write this paper, and I was very pleased that I was able to pull it together and let it flow out with very little editing.

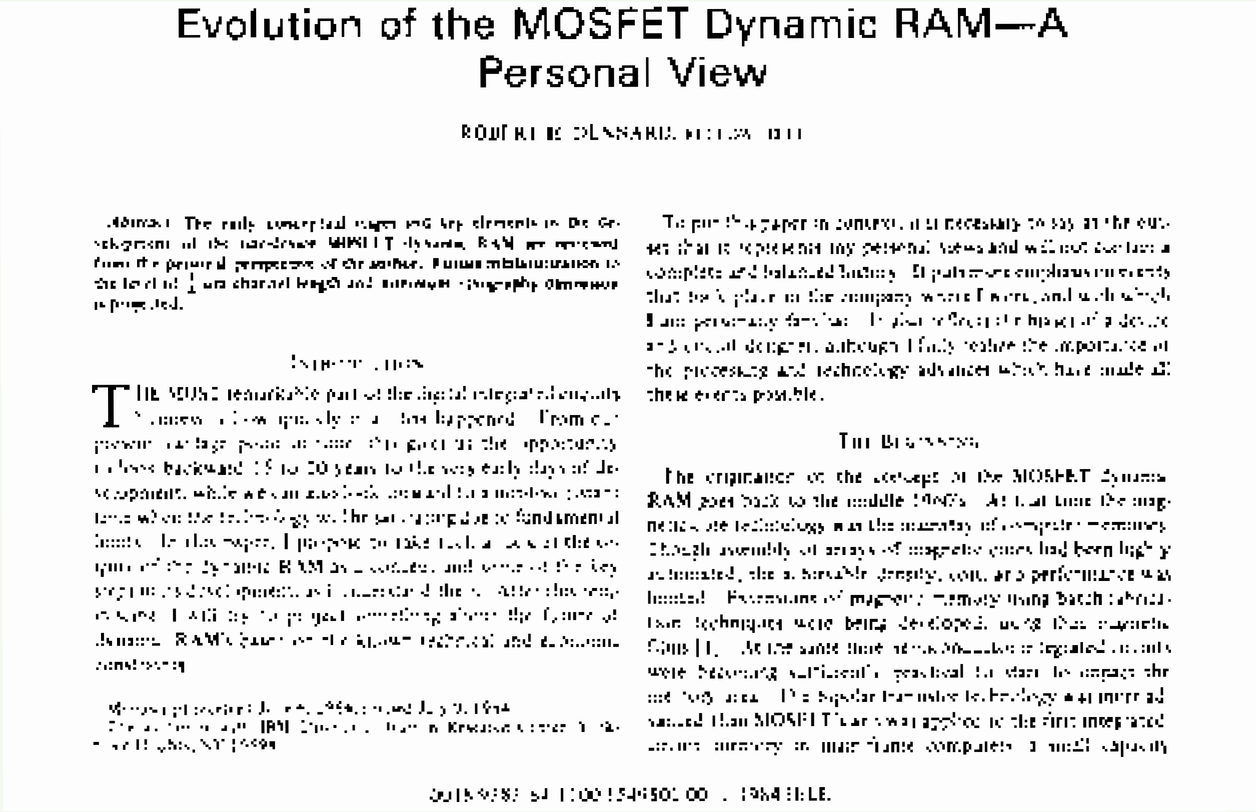
On rereading my paper, I feel it is a good history of the early days of semiconductor memory development, and it explains as clearly as I can how my invention of DRAM came about. However, I have done a little more work since then to delineate what the capability of magnetic-core memory was at the time of my invention of DRAM in 1967. I found that the largest IBM mainframes had 1MB of memory with an access time of 1-2 microseconds, and apparently dissipated 40kW of power according to the data in Ref.1 of the reprinted paper. (Hardly what one wants to have in their PC.) That is in sharp contrast to the capability of DRAM even in it’s infancy in the middle 1970s, which certainly led to the rapid growth in personal and portable computers thereafter.

The history of DRAM development up to 1984 is based on what I knew personally and was able to find references for. It only touches some highlights. There were a lot of technology, circuit and architectural advances in the very competitive environment of that period, with only a little documentation in the public literature.

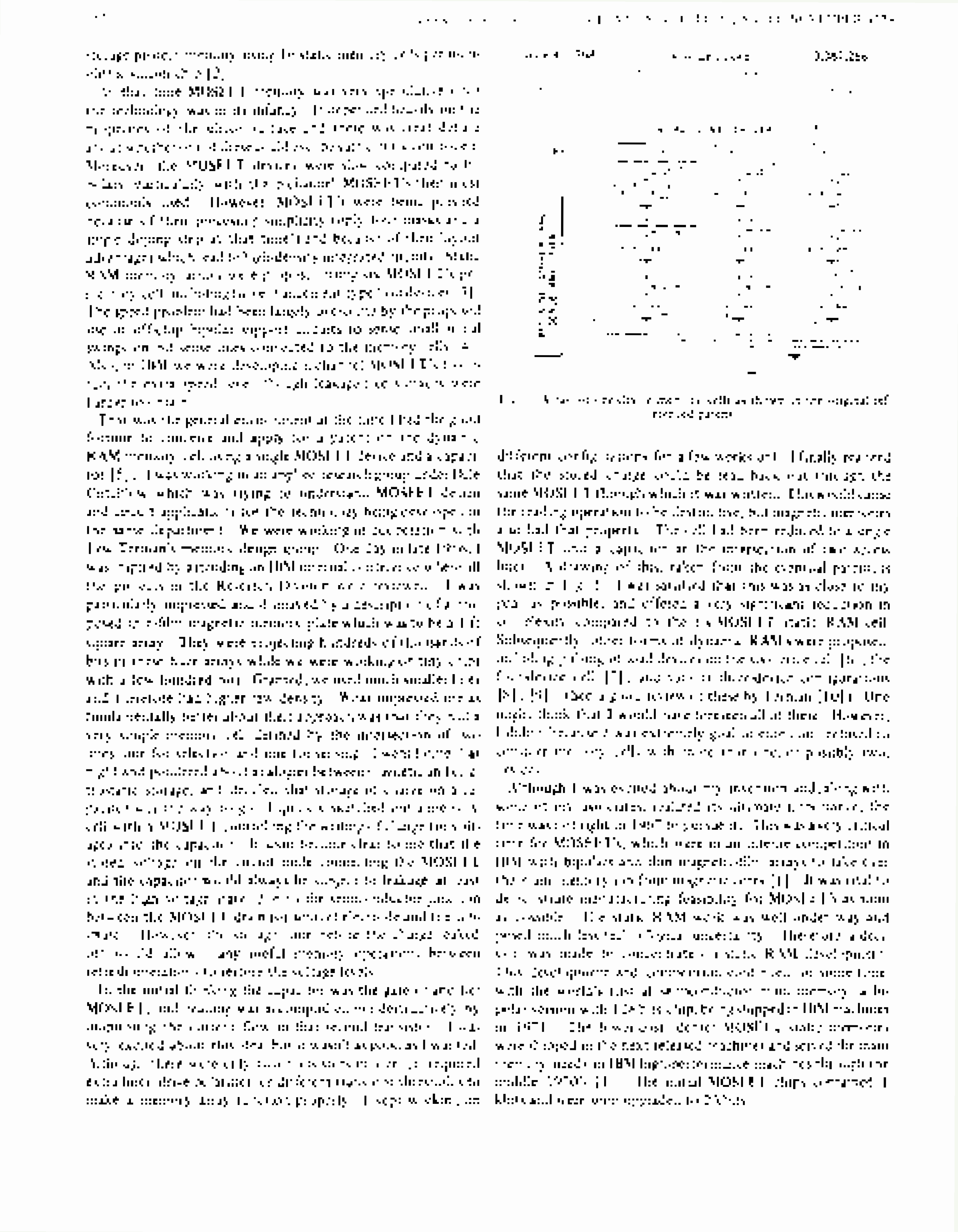
My final topic of “FUTURE PROSPECTS” in this reprinted paper is a case study in the hazards of predicting the future. It does serve as a good reference to the state of knowledge in 1984. As we all know, optical lithography has progressed to give more than ten times smaller features than we expected at that time. Scaling of transistors has also gone a lot further. Here the progress was driven by the unexpected robustness of gate insulators which allowed them to be scaled thinner and operated at much higher electric fields than we ever dreamed possible. Moreover, the emergence of CMOS offset (for a while, at least) the dramatic increase in power density associated with this large increase in electric fields.

At this point in time we are finding it very challenging to continue the pace of progress we have enjoyed in the past 35 years or so. I now know better than to make predictions for the future, but I will repeat the final line of my 1984 paper: It should be interesting to look back in 15 more years and see what has really happened!

Robert H. Dennard, November 2007



Evolution of the MOSFET Dynamic RAM—A Personal View



storage product memory using bipolar static memory [illegible] [2].

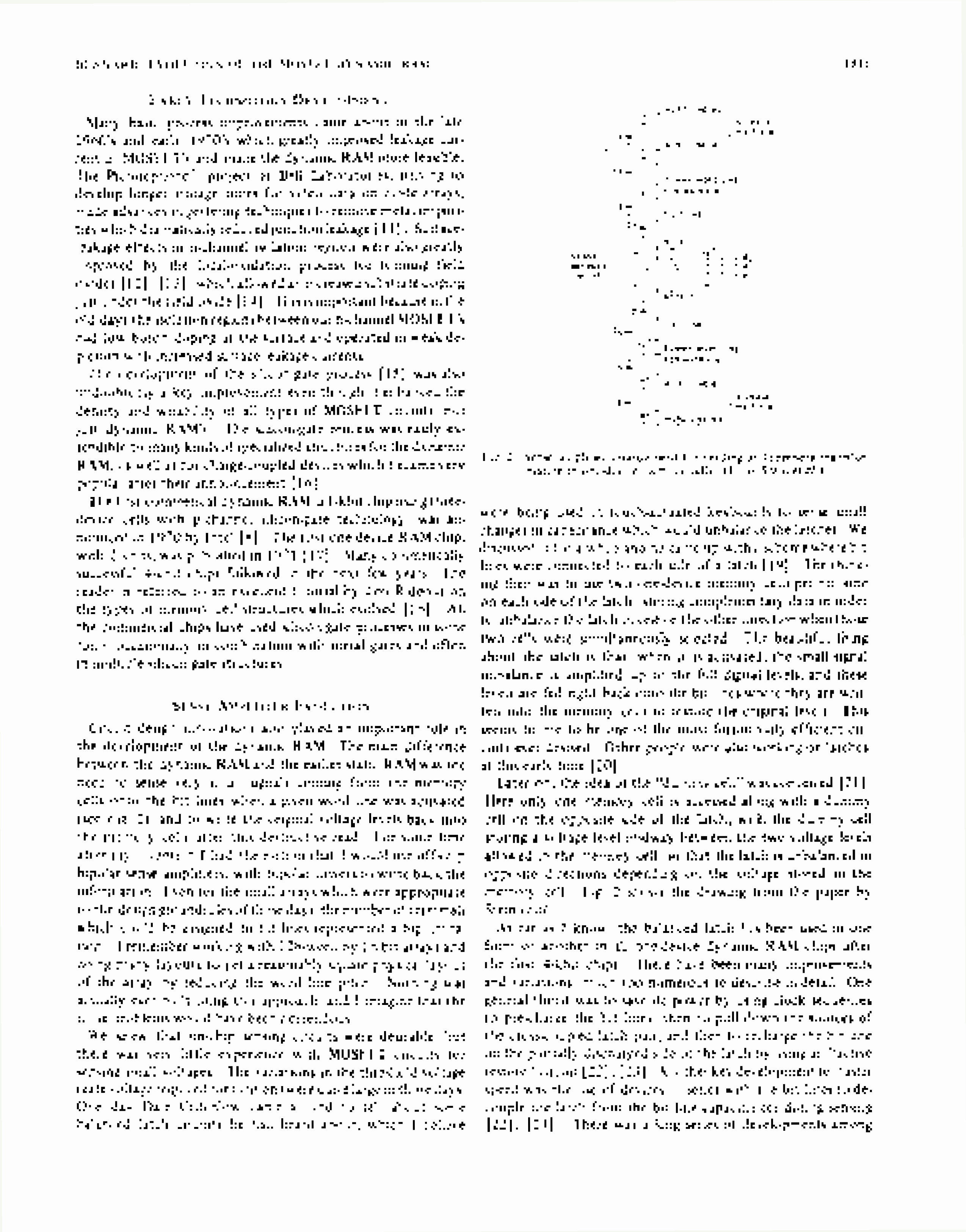
At that time MOSFET memory was very speculative since the technology was in its infancy. [illegible] and [illegible] the [illegible] of the [illegible] [illegible] and there was [illegible] [illegible] [illegible] [illegible]. Moreover, the MOSFET devices were slow compared to bipolar [illegible] especially with the p-channel MOSFET's then most commonly used. However, MOSFET's were being pursued because of their processing simplicity (only four masks and a single doping step at that time) and because of their layout advantages which lead to high-density integrated circuits. Static RAM memory arrays were [illegible] using six MOSFET's per [illegible] cell [illegible] [3]. The speed problem had been largely overcome by the proposed use of effective bipolar support circuits to sense small signal swings on the sense lines connected to the memory cells. Also, in IBM we were developing n-channel MOSFET's to [illegible] the extra speed, even though leakage problems were larger in this case.

This was the general environment at the time I had the good fortune to conceive and apply for a patent on the dynamic RAM memory cell using a single MOSFET device and a capacitor [5]. I was working in an applied research group under Dale Critchlow which was trying to understand MOSFET device and circuit applications to the technology being developed in the same department. We were working in cooperation with Lew Terman's memory design group. One day in late 1966, I was inspired by attending an IBM internal conference where all the projects in the Research Division were reviewed. I was particularly impressed and disturbed by a description of a proposed thin-film magnetic memory plane which was to be a 1 ft square array. They were projecting hundreds of thousands of bits in those flat arrays while we were working on chips with a few hundred bits. Granted, we used much smaller lines and therefore had higher raw density. What impressed me as fundamentally better about that approach was that they had a very simple memory cell defined by the intersection of two lines, one for selection and one for sensing. I went home that night and pondered about analogies between magnetic and electrostatic storage, and I decided that storage of charge on a capacitor was the way to go. I quickly sketched out a memory cell with a MOSFET controlling the writing of charge [illegible] onto the capacitor. It soon became clear to me that the stored voltage on the circuit node connecting the MOSFET and the capacitor would always be subject to leakage, at least in the high voltage state, due to the semiconductor junction between the MOSFET drain (or source) electrode and the substrate. However, the storage time ought to be long enough to allow many useful memory operations between refresh operations to restore the voltage levels.

In the initial thinking, the capacitor was the gate of another MOSFET, and reading was accomplished nondestructively by monitoring the current flow in that second transistor. I was very excited about this idea, but it wasn't as good as I wanted. Although there were only [illegible] transistors [illegible] it required extra lines [illegible] or different [illegible] to make a memory array function properly. I kept working on different configurations for a few weeks until I finally realized that the stored charge could be read back out through the same MOSFET through which it was written. This would cause the reading operation to be destructive, but magnetic memories also had that property. The cell had been reduced to a single MOSFET and a capacitor at the intersection of two signal lines. A drawing of this, taken from the eventual patent, is shown in Fig. 2. I was satisfied that this was as close to my goal as possible, and offered a very significant reduction in [illegible] compared to the six-MOSFET static RAM cell. Subsequently, other forms of dynamic RAM's were proposed, including [illegible] [6], the [illegible] cell [7], and various other innovative configurations [8], [9]. (See a good review of these by Terman [10].) One might think that I would have been excited at these. However, I didn't because I was extremely [illegible] cells with [illegible] possibly [illegible].

Fig. 2. [illegible] cell as shown in the original issued patent.

Although I was excited about my invention and, along with some of my associates, realized its ultimate importance, the time was not right in 1967 to pursue it. This was a very critical time for MOSFET's, which were in an intense competition in IBM with bipolar and thin magnetic-film arrays to take over the main memory role from magnetic cores [1]. It was vital to demonstrate manufacturing feasibility for MOSFET's as soon as possible. The static RAM work was well under way and posed much less [illegible] uncertainty. Therefore, a decision was made to concentrate on static RAM development. This development and [illegible] at about that time with the world's first all semiconductor main memory, a bipolar system with 128-bit chips, being shipped in IBM machines in 1971. The lower cost, denser MOSFET static memories were shipped in the next related machines and served the main memory needs in IBM high-performance machines through the middle 1970's [1]. The initial MOSFET chips contained 1 kbits and were later upgraded to 2 kbits.



DENNARD: EVOLUTION OF THE MOSFET DYNAMIC RAM 1551

EARLY TECHNOLOGY DEVELOPMENTS

Many basic process improvements came about in the late 1960's and early 1970's which greatly improved leakage currents in MOSFET's and made the dynamic RAM more feasible. The Picturephone® project at Bell Laboratories, aiming to develop longer storage times for silicon diode camera arrays, made advances in gettering techniques to remove metal impurities which dramatically reduced junction leakage [11]. Surface leakage effects in n-channel devices were also greatly improved by the local-oxidation process for forming field oxides [12], [13], which allowed an increased channel-stop doping under the field oxide [14]. This is important because in the old days the isolation regions between our n-channel MOSFET's had low boron doping at the surface and operated in weak depletion with increased surface leakage currents.

The development of the silicon gate process [15] was also undoubtedly a key improvement even though it enhanced the density and versatility of all types of MOSFET circuits, not just dynamic RAM's. The silicon-gate process was easily extendible to many kinds of specialized structures for the dynamic RAM, as well as for charge-coupled devices which became very popular after their announcement [16].

The first commercial dynamic RAM, a 1-kbit chip using three-device cells with p-channel silicon-gate technology, was announced in 1970 by Intel [4]. The first one-device RAM chip, with 2 kbits, was published in 1971 [17]. Many commercially successful 4-kbit chips followed in the next few years. The reader is referred to an excellent tutorial by Jim Rideout on the types of memory cell structures which evolved [18]. All the commercial chips have used silicon-gate processes in some form, occasionally in combination with metal gates and often in multilevel silicon gate structures.

SENSE AMPLIFIER DEVELOPMENT

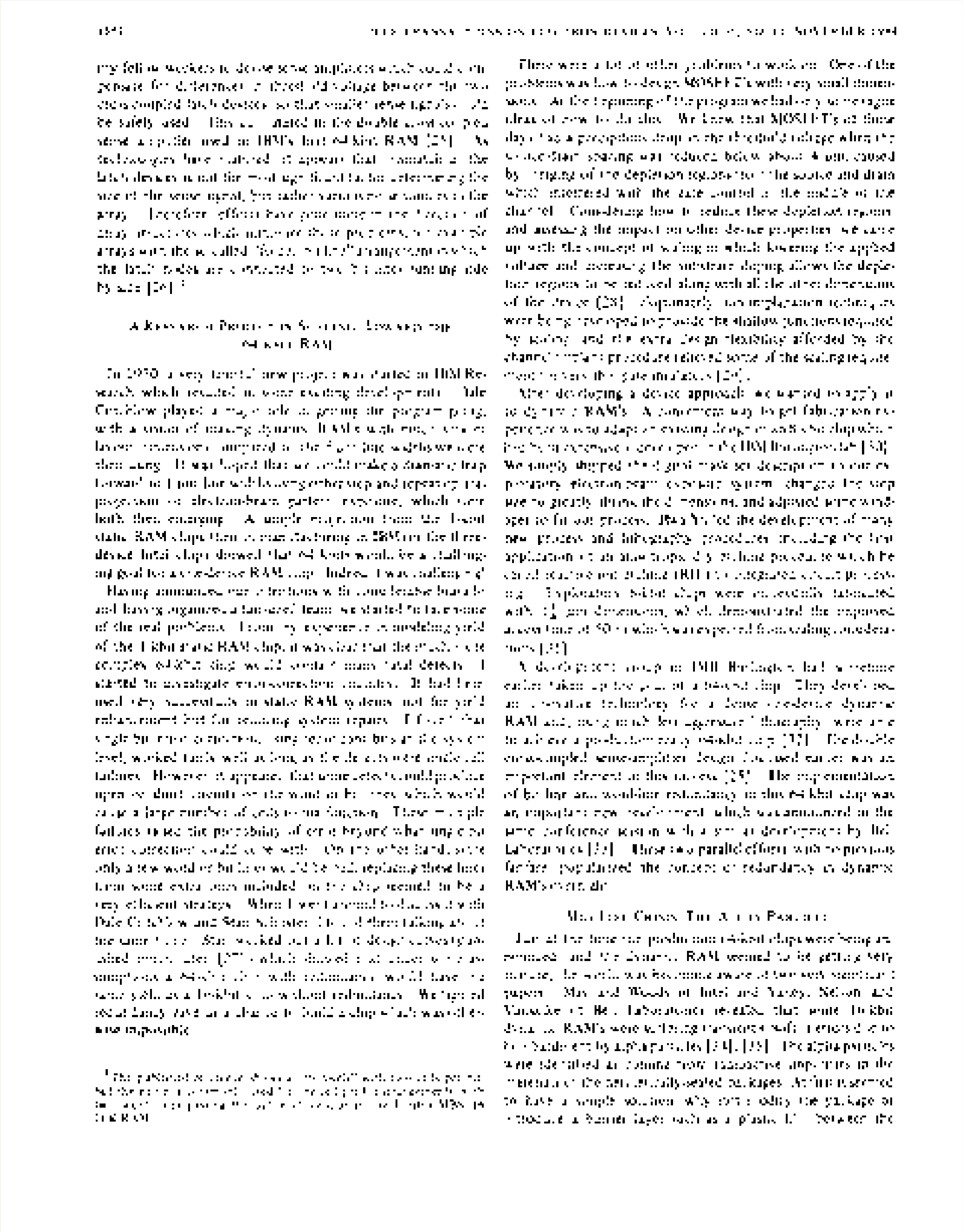
Circuit design innovations have played an important role in the development of the dynamic RAM. The main difference between the dynamic RAM and the earlier static RAM was the need to sense very small signals coming from the memory cells onto the bit lines when a given word line was activated (see Fig. 2) and to write the original voltage levels back into the memory cell after this destructive read. For some time after my invention I had the notion that I would use off-chip bipolar sense amplifiers with bipolar drivers to write back the information. Even for the small arrays which were appropriate to the design groundrules of those days, the number of connections which would be required to the bit lines represented a big problem. I remember working with 32-word by 32-bit arrays and drawing many layouts to get a reasonably square physical layout of the array by reducing the word line pitch. Nothing was actually ever built using this approach, and I imagine that the connection problems would have been horrendous.

We knew that on-chip sensing circuits were desirable, but there was very little experience with MOSFET circuits for sensing small voltages. The variations in the threshold voltage [illegible] in those days. One day Dale Critchlow came around to tell me about some balanced latch circuits he had heard about, which I believe were being used in touch-activated keyboards to sense small changes in capacitance which would unbalance the latches. We designed [illegible] where the bit lines were connected to each side of a latch [19]. The thinking then was to use two one-device memory cells per bit, one on each side of the latch, storing complementary data in order to unbalance the latch in one or the other direction when these two cells were simultaneously selected. The beautiful thing about the latch is that when it is activated, the small signal imbalance is amplified up to the full signal levels, and these levels are fed right back onto the bit lines where they are written into the memory cells to restore the original levels. This seems to me to be one of the most fundamentally efficient circuits ever devised. Other people were also working on latches at this early time [20].

Fig. 2. Sense amplifier arrangement employing [illegible] from Stein et al. [21]

Later on, the idea of the "dummy cell" was conceived [21]. Here only one memory cell is accessed along with a dummy cell on the opposite side of the latch, with the dummy cell storing a voltage level midway between the two voltage levels allowed in the memory cell so that the latch is unbalanced in opposite directions depending on the voltage stored in the memory cell. Fig. 2 shows the drawing from the paper by Stein et al.

As far as I know, the balanced latch has been used in one form or another in all one-device dynamic RAM chips after the first 4-kbit chips. There have been many improvements and variations, much too numerous to describe in detail. One general thrust was to save dc power by using clock pulses to precharge the bit lines, then to pull down the sources of the cross-coupled latch pair, and then to recharge the bit line on the partially discharged side of the latch by using an "active restore" circuit [22], [23]. Another key development for faster speed was the use of devices in series with the bit lines to decouple the latch from the bit line capacitance during sensing [22], [24]. There was a long series of developments among



chip and the package. When experiments like these were done in various labs, the error rates dropped substantially but did not go away, presumably due to radioactive impurities in the coating materials. Also, an analysis of the possible soft-error rate due to cosmic rays showed that this source could be significant [35].

Here was a real crisis! Not only were hundreds of people working around the clock on dynamic RAM development and manufacturing, but the whole future of our cherished MOSFET's was seen to be in jeopardy. Personally, I felt very responsible because of my early role with dynamic RAM's and because I failed to anticipate the problem. Several years earlier I had discussed the possible effect of cosmic rays on dynamic RAM's with an old friend who was knowledgeable about space electronics, but we had concluded that most of the radiation types would pass through with little effect.

After a long period of doing measurements, developing models, and inventing possible cures, a less threatening view of alpha-particles emerged. A good quantitative understanding was provided by various modeling techniques which were developed, including a very powerful Monte Carlo approach [37]. It could be shown that error rates would rise in response to scaling to smaller dimensions, but that structural and design changes would help contain the problem. While some special new structures were invented to block unwanted carriers from deep in the substrate [38], similar benefits are available for free in the CMOS technology if the memory array is built in a shallow well. Thus the alpha-particle problem has helped accelerate the use of CMOS in dynamic RAM's [39]. Although the immediate anxiety over alpha-particles is gone, the authors of the first paper were right in claiming recognition of an important new physical mechanism which would affect the course of future dynamic RAM development [34].

FUTURE PROSPECTS

By now the dynamic RAM has reached a very advanced state compared to its initial beginning. The key factor behind the tremendous improvements has been the shrinking of lithographic dimensions from about 5-7 µm initially down to about 1 µm in the products now being developed with 256 kbit to 1 Mbit capacity per chip. Future progress requires the continuation of these trends. In fact, most experts agree that optical lithography is approaching a fundamental limit in the order of 0.7 µm. A rather profound and costly change to electron beam or X-ray techniques will be necessary for further miniaturization. Such exposure systems are still under development and facing difficult problems. It is fairly generally believed that linewidth reduction down to at least 0.25 µm is technically feasible. At present there is no sign of weakening of the economic incentives which have supported the increasingly costly lithography tools required for these advances.

At one time, we identified the nonscaling off-threshold behavior as a limiting factor in miniaturization of MOSFET dynamic RAM's [28], [29]. This was the case where one device type was used for both array and logic devices, since the nominal device threshold voltage could not be reduced below about 0.7 V for operation over a range of elevated temperatures in order to control leakage from the storage capacitor through the array device when the word line is turned off. However, for some time now, technology evolution has brought about independent optimization of array-device and support-device thresholds, so that the support-device thresholds alone can be scaled down along with the power supply voltage. Furthermore, boosted word-line techniques have been developed to write a full power-supply level into the memory cells in spite of the large array-device threshold. It appears that these design trends can take dynamic RAM's well into the submicrometer regime, even with considerably reduced power supply level.

TABLE I

[illegible]

[illegible]

Many submicrometer MOSFET's have already been built on an exploratory basis, particularly of the n-channel type, with dimensions down to ¼ µm and below [40]. Though the present MOSFET technology is rapidly evolving to CMOS, the scaling of p-channel devices to small dimensions is more difficult because of problems with the depth and resistivity of the p+ source/drain regions. Also, p+-doped silicon gates or other suitable gate materials for low-threshold p-channel MOSFET's, pose substantial technology problems. In the long range, these specific problems will undoubtedly be solved, along with whatever technology changes are necessary because of latchup problems in small dimension CMOS.

To investigate the miniaturization limits of dynamic RAM's, it is useful to consider scaling from design values presently in use at the 1-µm level to dynamic RAM's with ¼-µm dimensions. Table I lists an estimate of design values typically used for current megabit dynamic-RAM development, with a second column scaled by a factor of four. For simplicity this table is defined in NMOS terms, but CMOS may actually be used if the extra problems of building very small p-channel devices can be solved. The third column gives an estimate of practical targets for a not completely scaled design in which the electric field is allowed to increase and the array-device threshold is maintained at a large value. This needs to be done in spite of concerns on how field-induced reliability effects, such as gate-insulator wear-out and hot-electron damage, behave in this regime of dimensions and voltage. Some data and models for evaluating the benefits of annealing hot-electron damage, for example, are encouraging. Therefore, this nonconstantly scaled design trades higher electric field for speed and somewhat higher margin in the memory cell, to arrive at a considerably higher supply voltage. The new device design technique proposed by Ogura et al. [41] can be used to control punchthrough of the very short device even with the thicker gate insulator. With a supply voltage of 2 V, a [illegible] boost to 3 V can be used to write a [illegible] tion and the full 2 V is in the memory cell.

Assuming that such sense amplifiers [illegible] quired design serves the same number of bits as in the [illegible] starting case, then the sense signal would be about 40 percent as much as in the starting case due to the power supply reduction. This signal is amplified in a much more sensitive and delicate sense amplifier because of the gate insulator and channel-length reductions. The common-mode noise in the array will scale down because of the reduced circuit voltage swings. The main question to be addressed is the problem of random noise sources. It is of some comfort to consider that the stored charge represents about 10^5 electrons which is large compared to statistical fluctuations in that number. Thermal noise sources are generally calculated to be on the order of 1 mV [12], and should be fairly negligible even with the reduced signal levels. The main problem would appear to be sensitivity to alpha-particle or cosmic-ray disturbances. Alpha-particle ionization rates vary with energy but typically would be about 10^5 electrons per μm of track. In the ½-μm structure the storage capacitor area is about 1 μm² and the depth susceptible to an alpha-particle hit, using the CMOS well structure [illegible] an excellent protection scheme, would be less than ½ μm by scaling [illegible] present [illegible] technique. It appears that the collected charge from a typical alpha-particle hit on a cell would be a maximum of 10^5 electrons while the effective signal at the sense amplifier would also be a maximum 10^5 electrons because of reductions by the dummy-cell signal and array noise sources. Thus most every alpha-particle hit would cause an error, while few hits would be shallow enough to cause multiple errors. [illegible] the probability of error for the best 1-μm structure in [13], it appears that the probability of error [illegible] 20 [illegible] ½ μm case considered here. Since there are [illegible] more bits per given area, each cell is [illegible] and the error probability per bit in the memory system would remain about constant. Thus, systems will get bigger. Hopefully, error-correction techniques will get more sophisticated, particularly for small systems where they are hardly being used today.

Surely, over the course of time there will be a lot of innovation in this area. The extensive work on three-dimensional capacitor structures using etched trenches [43] clearly can make a big impact. By storing more charge [illegible] the alpha-particle [illegible] and [illegible] to be [illegible] by a given sense amplifier [illegible] in large arrays. Other types of three-dimensional structures may evolve from the silicon-on-insulator (SOI) work.

The possibility of shrinking dimensions much beyond ½ μm at room temperature seems dim. Many authors have pointed out the difficulties, including tunneling effects in the devices and interconnection limits. The main problem is that the voltage has to be reduced to maintain practical electric fields in smaller devices. Low-temperature operation can help dynamic RAM's work at lower voltage because of the sharper turn-off in the subthreshold region [44]. The [illegible] for [illegible] 77 K [illegible] toward further scaling [illegible].

In summary, it seems that 256-Mbit chips are achievable with today's [illegible] ½ μm. Much greater densities than that will be very difficult with our present view of the limits and operation at cryogenic temperature [illegible] chip. Chip sizes larger [illegible] wafer-scale integration [illegible] chip [illegible] make these [illegible] operation. It should be interesting to look back [illegible] 15 [illegible] years and see what has really happened.

ACKNOWLEDGMENT

The help and contributions of many associates have been noted in the text and references. There are many others who played vital roles in the work described. In particular, [illegible] and [illegible] were instrumental in starting and managing the [illegible] research programs I described. Also, I [illegible] the help of [illegible] dynamic [illegible] RAM. I want to thank L. M. Terman for a critical reading of the manuscript.

REFERENCES

[1] [illegible] IBM J. Res. Develop., vol. 24, no. 5, p. [illegible] 1980.

[2] [illegible] presented at [illegible] 1965.

[3] J. D. Schmidt, "Integrated MOS transistor random access memory," Solid State Design, vol. 6, Jan. 1965.

[4] P. Pleshko and L. M. Terman, "An investigation of the potential of MOS transistor memories," IEEE Trans. Electron. Comput., vol. EC-15, no. 4, p. 423, 1966.

[5] R. H. Dennard, "Field-effect transistor memory," U.S. Patent 3 387 286, June 4, 1968.

[6] [illegible] Sept. 1967.

[7] D. P. Spampinato and L. M. Terman, [illegible] U.S. Patent [illegible].

[8] W. M. Regitz and J. Karp, "A three transistor-cell 1024-bit 500 ns MOS RAM," in ISSCC Dig. Tech. Papers, p. 42, 1970.

[9] [illegible] U.S. Patent [illegible].

[10] L. M. Terman, "MOSFET memory circuits," Proc. IEEE, vol. 59, p. 1044, 1971.

[11] [illegible] dimensions," [illegible] 1974.

[12] [illegible] p. 126 [illegible] 1976.

[13] [illegible] 1979.

[14] [illegible] 1977.

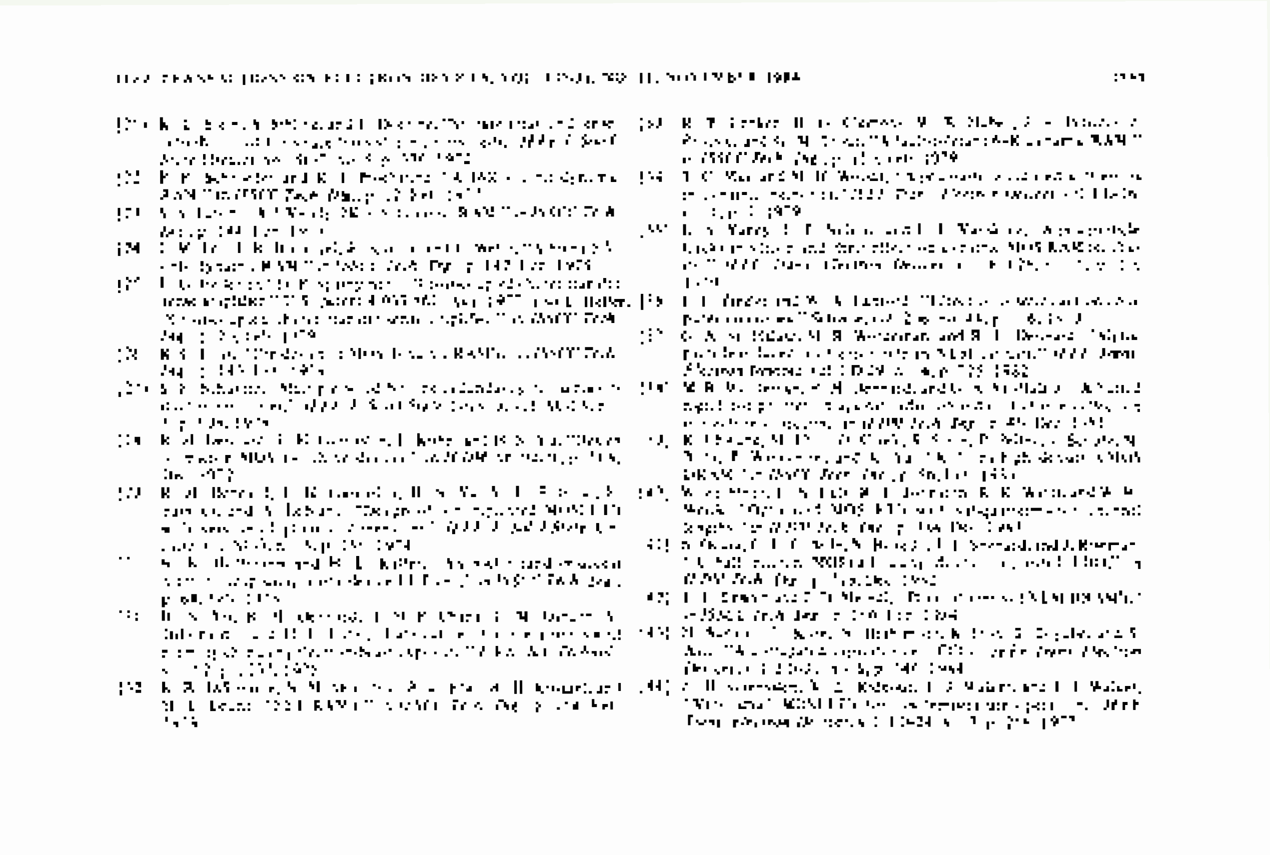
[15] [illegible]

[16] [illegible]

[17] [illegible] 1974.

[18] [illegible] 1974.

[19] [illegible] U.S. Patent [illegible].



June 4, 1968 R. H. DENNARD 3,387,286

FIELD-EFFECT TRANSISTOR MEMORY

Filed July 14, 1967 3 Sheets-Sheet 1

FIG. 1

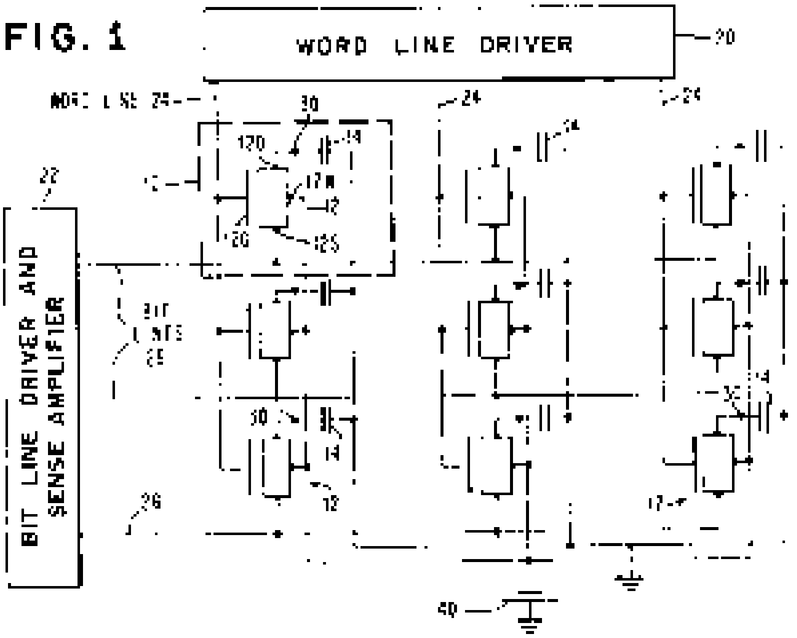
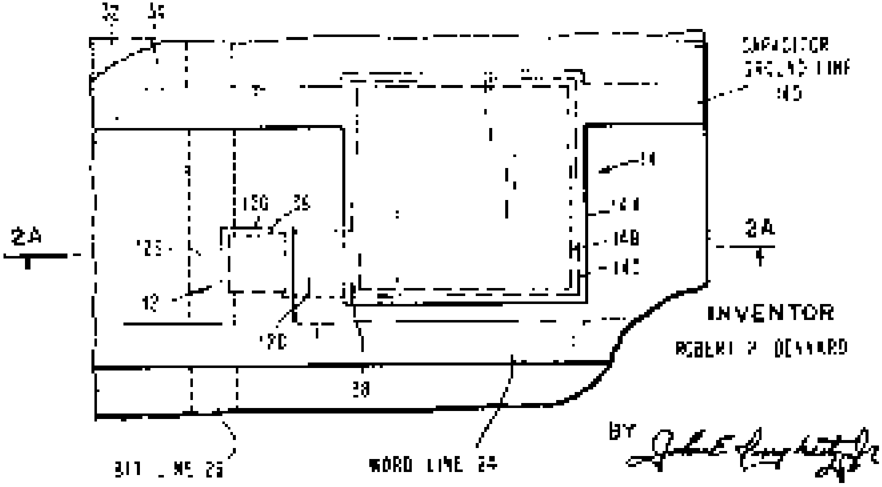


FIG. 2



INVENTOR
ROBERT H. DENNARD

BY

ATTORNEY

June 4, 1968 R. H. DENNARD 3,387,286

FIELD-EFFECT TRANSISTOR MEMORY

Filed July 14, 1967 3 Sheets-Sheet 2

FIG. 2A

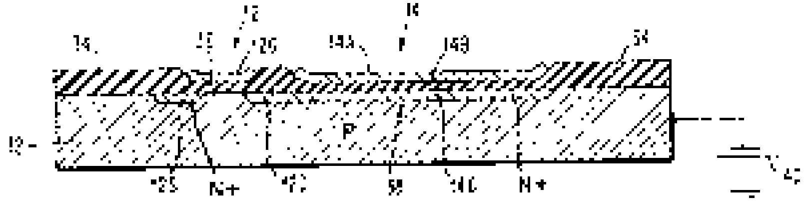
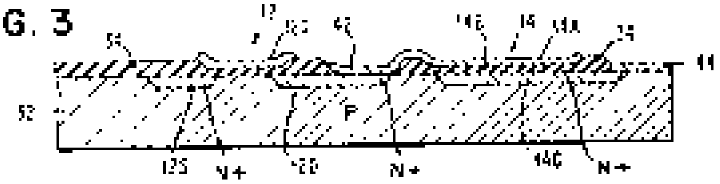


FIG. 3



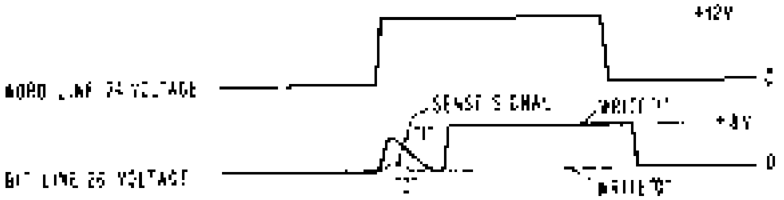


FIG. 4A

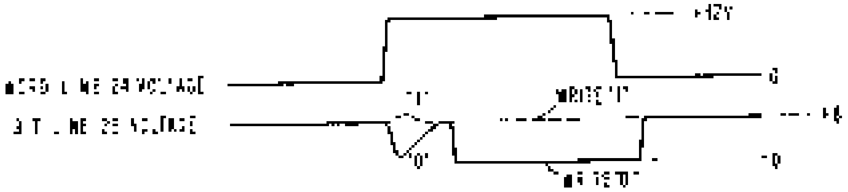


FIG. 4B

June 4, 1968 R. H. DENNARD **3,387,286**

FIELD-EFFECT TRANSISTOR MEMORY

Filed July 14, 1967 3 Sheets-Sheet [illegible]

FIG. 5

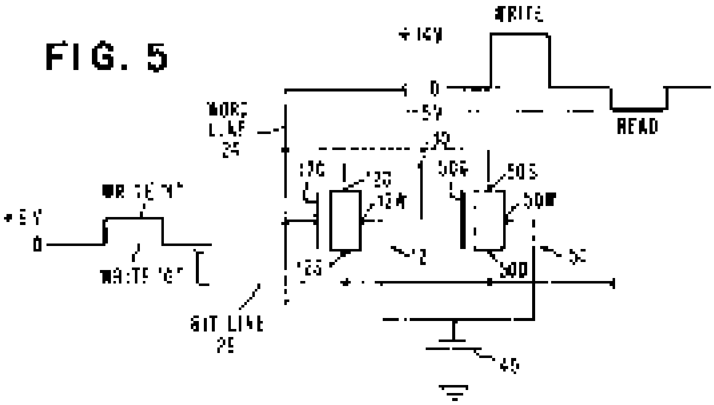


FIG. 7

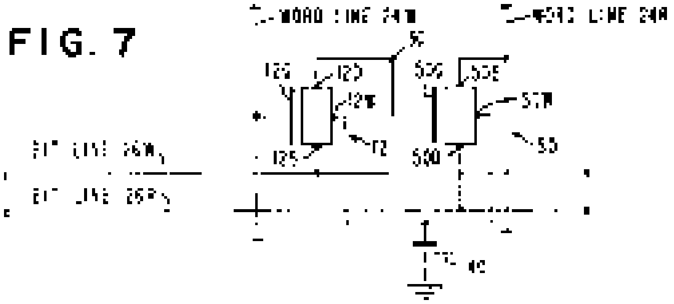
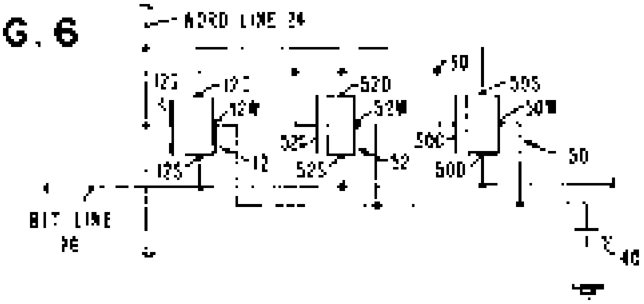


FIG. 6



United States Patent Office

3,387,286

Patented June 4, 1968

1

3,387,286

FIELD-EFFECT TRANSISTOR MEMORY

Robert H. Dennard, Croton-on-Hudson, N.Y., assignor to International Business Machines Corporation, Armonk, N.Y., a corporation of New York

Filed July 14, 1967, Ser. No. 653,415

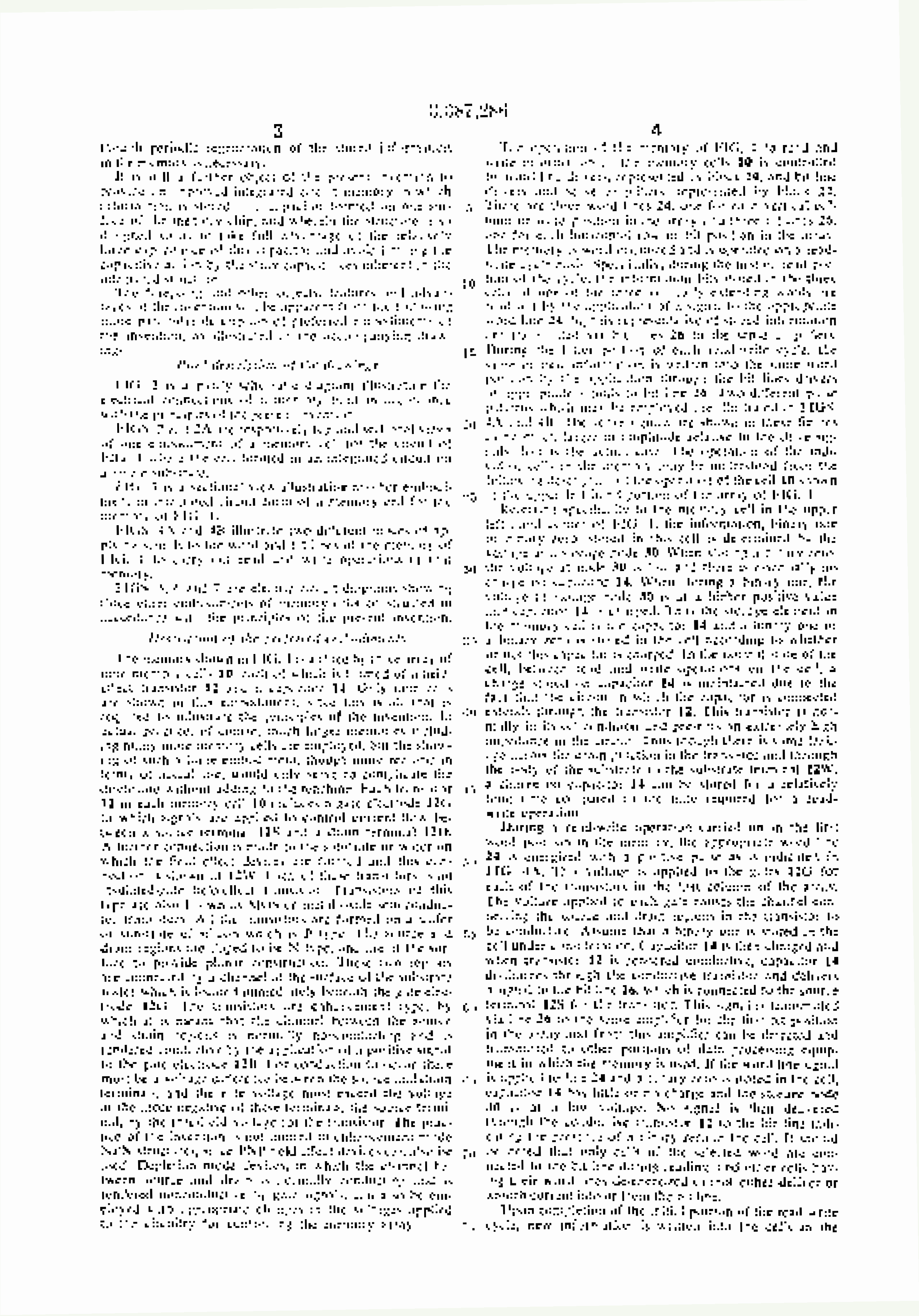
21 Claims. (Cl. 340—173)

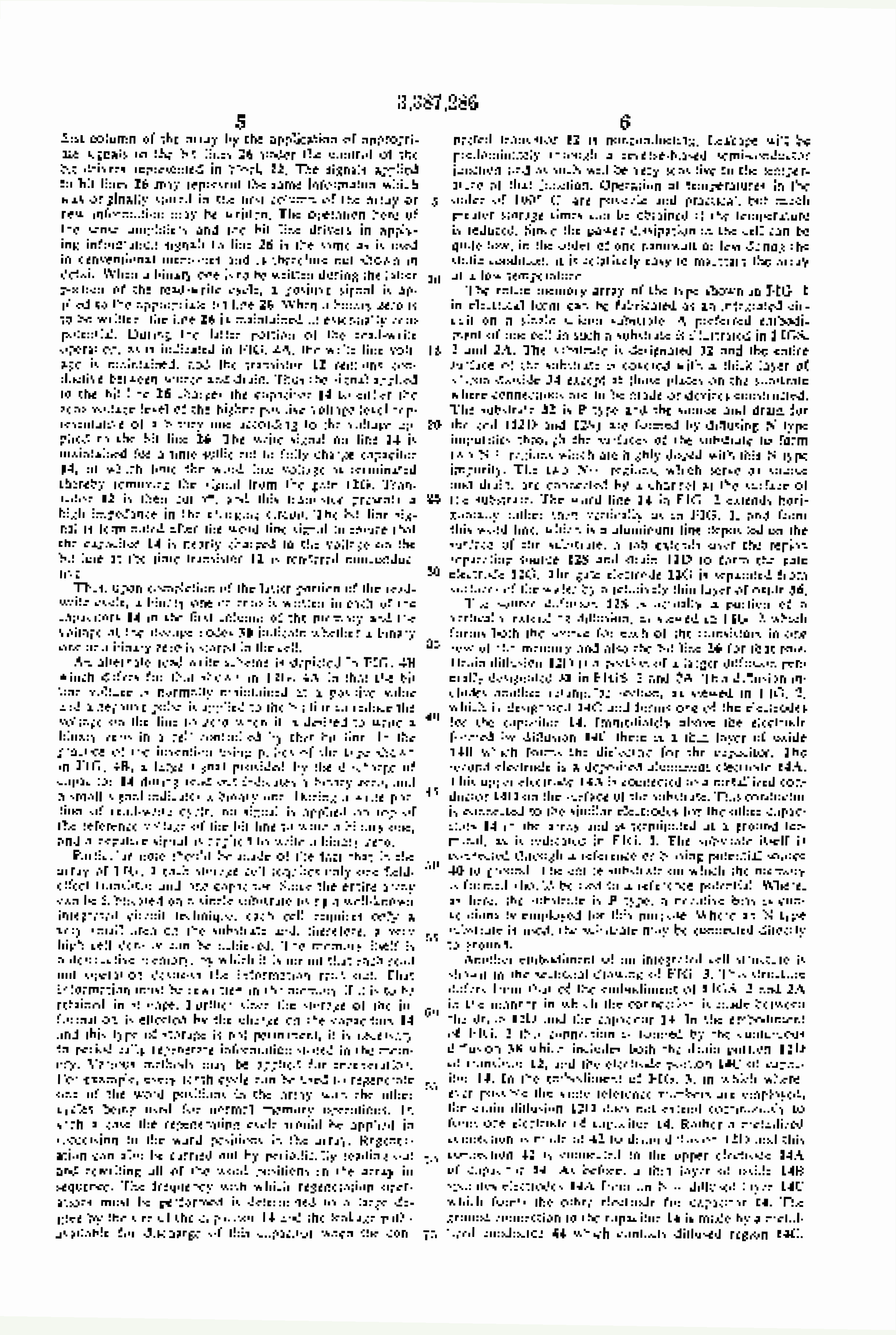
ABSTRACT OF THE DISCLOSURE

Prior art

2

Summary of the invention





3,387,286

5

first column of the array by the application of appropriate signals to the bit lines 26 under the control of the bit drivers represented in block 22. The signals applied to bit lines 26 may represent the same information which was originally stored in the first column of the array or new information may be written. The operation here of the sense amplifiers and the bit line drivers in applying information signals to line 26 is the same as is used in conventional memories and is therefore not shown in detail. When a binary one is to be written during the latter portion of the read-write cycle, a positive signal is applied to the appropriate bit line 26. When a binary zero is to be written, the line 26 is maintained at essentially zero potential. During the latter portion of the read-write operation, as is indicated in FIG. 4A, the write line voltage is maintained, and the transistor 12 remains conductive between source and drain. Thus the signal applied to the bit line 26 charges the capacitor 14 to either the zero voltage level or the higher positive voltage level representative of a binary one according to the voltage applied to the bit line 26. The write signal on line 24 is maintained for a time sufficient to fully charge capacitor 14, at which time the word line voltage is terminated thereby removing the signal from the gate 12G. Transistor 12 is then cut off, and this transistor presents a high impedance in the charging circuit. The bit line signal is terminated after the word line signal to ensure that the capacitor 14 is nearly charged to the voltage on the bit line at the time transistor 12 is rendered nonconductive.

Thus, upon completion of the latter portion of the read-write cycle, a binary one or zero is written in each of the capacitors 14 in the first column of the memory and the voltage at the storage nodes 30 indicate whether a binary one or a binary zero is stored in the cell.

An alternate read-write scheme is depicted in FIG. 4B which differs from that shown in FIG. 4A in that the bit line voltage is normally maintained at a positive value and a negative pulse is applied to the bit line to reduce the voltage on the line to zero when it is desired to write a binary zero in a cell controlled by that bit line. In the practice of the invention using pulses of the type shown in FIG. 4B, a large signal provided by the discharge of capacitor 14 during read-out indicates a binary zero, and a small signal indicates a binary one. During a write portion of read-write cycle, no signal is applied on top of the reference voltage of the bit line to write a binary one, and a negative signal is applied to write a binary zero.

Particular note should be made of the fact that in the array of FIG. 1 each storage cell requires only one field-effect transistor and one capacitor. Since the entire array can be fabricated on a single substrate using well-known integrated circuit techniques, each cell requires only a very small area on the substrate and, therefore, a very high cell density can be achieved. The memory itself is a destructive memory, by which it is meant that each read-out operation destroys the information read out. That information must be rewritten in the memory if it is to be retained in storage. Further, since the storage of the information is effected by the charge on the capacitors 14 and this type of storage is not permanent, it is necessary to periodically regenerate information stored in the memory. Various methods may be applied for regeneration. For example, every Nth cycle can be used to regenerate one of the word positions in the array with the other cycles being used for normal memory operations. In such a case the regenerating cycle would be applied in succession to the word positions in the array. Regeneration can also be carried out by periodically reading out and rewriting all of the word positions in the array in sequence. The frequency with which regeneration operations must be performed is determined to a large degree by the size of the capacitor 14 and the leakage paths available for discharge of this capacitor when the con-

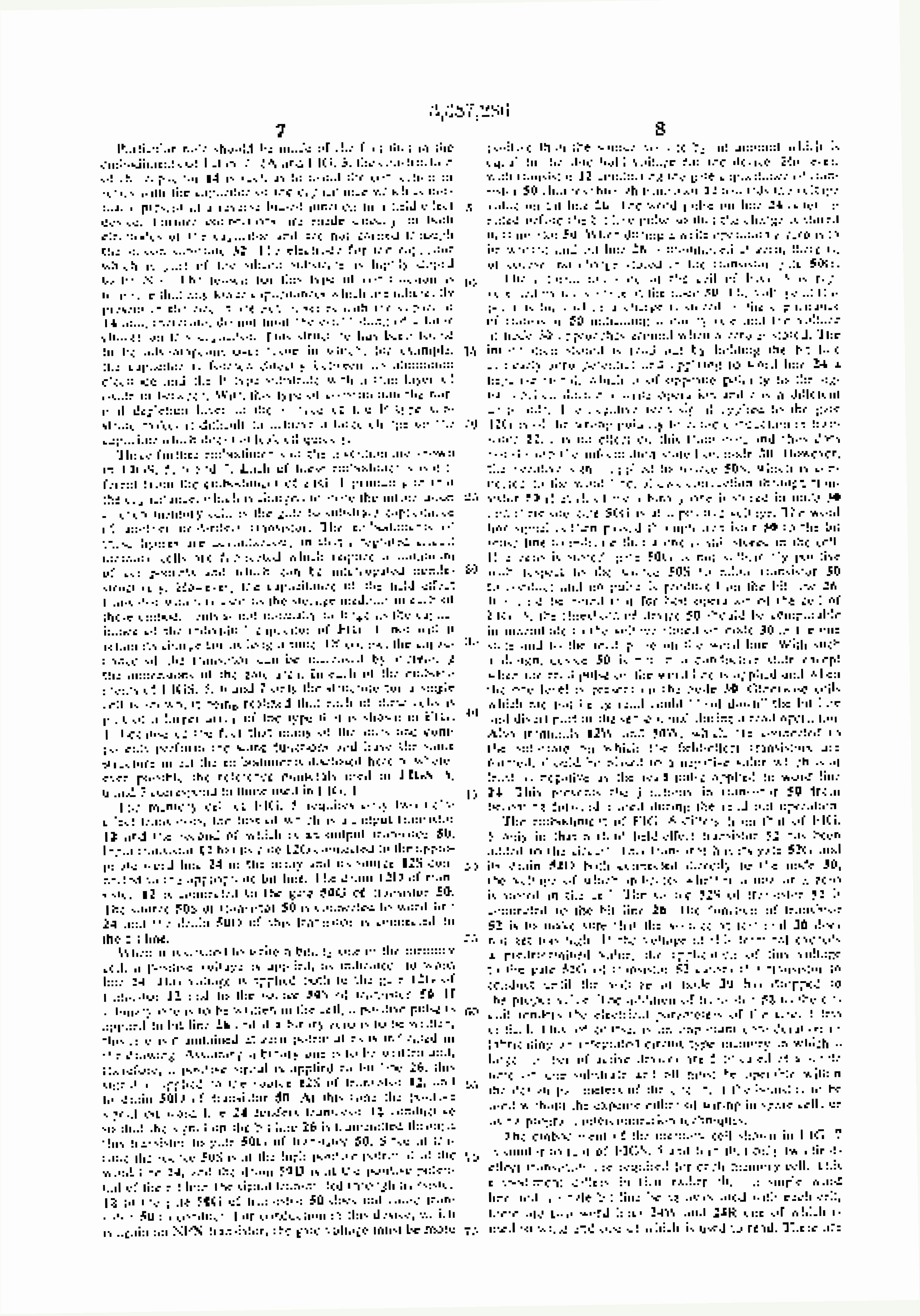
6

nected transistor 12 is nonconducting. Leakage will be predominantly through a reverse-biased semiconductor junction and as such will be very sensitive to the temperature of that junction. Operation at temperatures in the order of 100° C. are possible and practical, but much greater storage times can be obtained if the temperature is reduced. Since the power dissipation in the cell can be quite low, in the order of one nanowatt or less during the static condition, it is relatively easy to maintain the array at a low temperature.

The entire memory array of the type shown in FIG. 1 in electrical form can be fabricated as an integrated circuit on a single silicon substrate. A preferred embodiment of one cell in such a substrate is illustrated in FIGS. 2 and 2A. The substrate is designated 32 and the entire surface of the substrate is covered with a thick layer of silicon dioxide 34 except at those places on the substrate where connections are to be made or devices constructed. The substrate 32 is P type and the source and drain for the cell (12D and 12S) are formed by diffusing N type impurities through the surfaces of the substrate to form two N+ regions which are highly doped with this N type impurity. The two N+ regions, which serve as source and drain, are connected by a channel at the surface of the substrate. The word line 24 in FIG. 2 extends horizontally rather than vertically as in FIG. 1, and from this word line, which is a aluminum line deposited on the surface of the substrate, a tab extends over the region separating source 12S and drain 12D to form the gate electrode 12G. The gate electrode 12G is separated from surface of the wafer by a relatively thin layer of oxide 36.

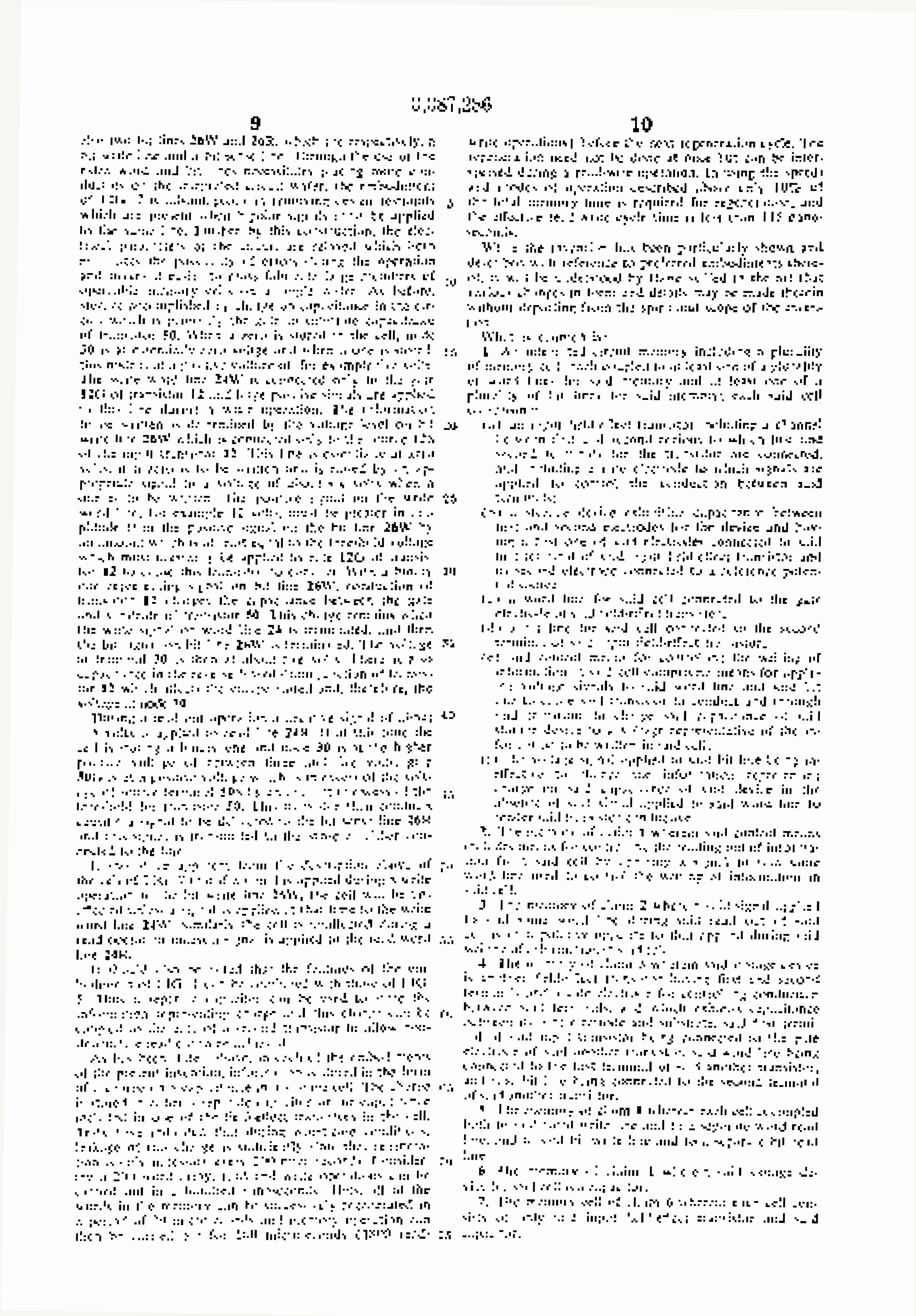
The source diffusion 12S is actually a portion of a vertically extending diffusion, as viewed in FIG. 2 which forms both the source for each of the transistors in one row of the memory and also the bit line 26 for that row. Drain diffusion 12D is a portion of a larger diffusion generally designated 38 in FIGS. 2 and 2A. This diffusion includes another rectangular section, as viewed in FIG. 2, which is designated 14C and forms one of the electrodes for the capacitor 14. Immediately above the electrode formed by diffusion 14C there is a thin layer of oxide 14B which forms the dielectric for the capacitor. The second electrode is a deposited aluminum electrode 14A. This upper electrode 14A is connected to a metallized conductor 14D on the surface of the substrate. This conductor is connected to the similar electrodes for the other capacitors 14 in the array and is terminated at a ground terminal, as is indicated in FIG. 1. The substrate itself is connected through a reference or biasing potential source 40 to ground. The entire substrate on which the memory is formed should be tied to a reference potential. Where, as here, the substrate is P type, a negative bias source is employed for this purpose. Where an N type substrate is used, the substrate may be connected directly to ground.

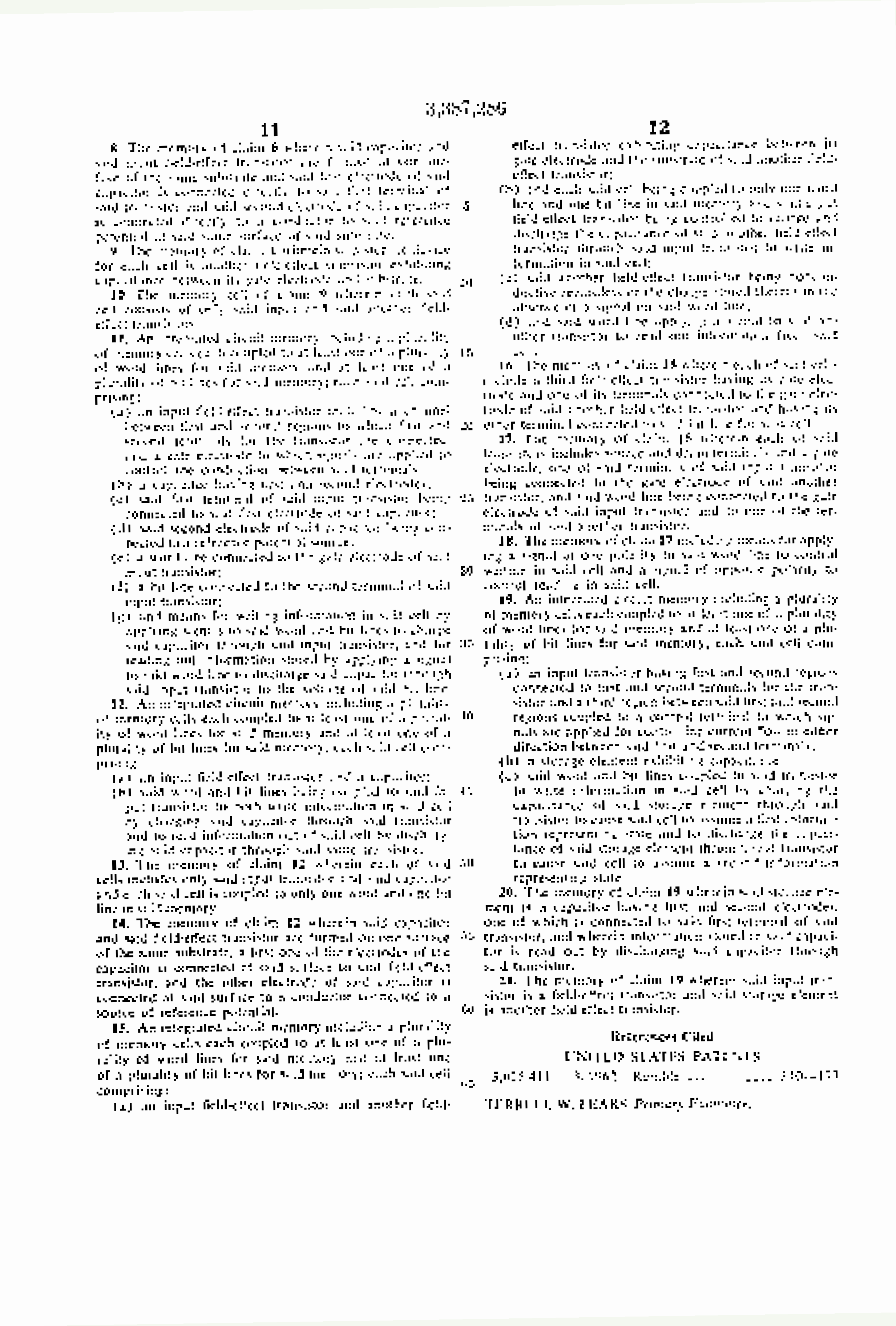
Another embodiment of an integrated cell structure is shown in the sectional drawing of FIG. 3. This structure differs from that of the embodiment of FIGS. 2 and 2A in the manner in which the connection is made between the drain 12D and the capacitor 14. In the embodiment of FIG. 2 this connection is formed by the continuous diffusion 38 which includes both the drain portion 12D of transistor 12, and the electrode portion 14C of capacitor 14. In the embodiment of FIG. 3, in which wherever possible the same reference numbers are employed, the drain diffusion 12D does not extend continuously to form one electrode of capacitor 14. Rather a metallized connection is made at 42 to drain diffusion 12D and this connection 42 is connected to the upper electrode 14A of capacitor 14. As before, a thin layer of oxide 14B separates electrodes 14A from an N+ diffused layer 14C which forms the other electrode for capacitor 14. The ground connection to the capacitor 14 is made by a metallized conductor 44 which contacts diffused region 14C.



7

8





3,387,286

11

8. The memory of claim 6 wherein said capacitor and said input field-effect transistor are formed at one surface of the same substrate and said first electrode of said capacitor is connected directly to said first terminal of said transistor and said second electrode of said capacitor is connected directly to a conductor held at reference potential at said same surface of said substrate.

9. The memory of claim 1 wherein said storage element for each cell is another field effect transistor exhibiting capacitance between its gate electrode and its substrate.

10. The memory cell of claim 9 wherein each of said cell consists of only said input and said another field effect transistors.

11. An integrated circuit memory including a plurality of memory cells each coupled to at least one of a plurality of word lines for said memory and at least one of a plurality of bit lines for said memory; each said cell comprising:

(a) an input field effect transistor having a channel between first and second regions to which first and second terminals for the transistor are connected and a gate electrode to which signals are applied to control the conduction between said terminals;

(b) a capacitor having first and second electrodes;

(c) said first terminal of said input transistor being connected to said first electrode of said capacitor;

(d) said second electrode of said capacitor being connected to a reference potential source;

(e) a word line connected to the gate electrode of said input transistor;

(f) a bit line connected to the second terminal of said input transistor;

(g) and means for writing information in said cell by applying signals to said word and bit lines to charge said capacitor through said input transistor, and for reading out information stored by applying a signal to said word line to discharge said capacitor through said input transistor to the [illegible] of said bit line.

12. An integrated circuit memory including a plurality of memory cells each coupled to at least one of a plurality of word lines for said memory and at least one of a plurality of bit lines for said memory, each said cell comprising

(a) an input field effect transistor and a capacitor;

(b) said word and bit lines being coupled to said input transistor to both write information in said cell by charging said capacitor through said transistor and to read information out of said cell by discharging said capacitor through said same transistor.

13. The memory of claim 12 wherein each of said cells includes only said input transistor and said capacitor and each said cell is coupled to only one word and one bit line in said memory.

14. The memory of claim 12 wherein said capacitor and said field-effect transistor are formed on one surface of the same substrate, a first one of the electrodes of the capacitor is connected at said surface to said field-effect transistor, and the other electrode of said capacitor is connected at said surface to a conductor connected to a source of reference potential.

15. An integrated circuit memory including a plurality of memory cells each coupled to at least one of a plurality of word lines for said memory and at least one of a plurality of bit lines for said memory; each said cell comprising:

(a) an input field-effect transistor and another field-effect transistor exhibiting capacitance between its gate electrode and the substrate of said another field-effect transistor;

(b) and each said cell being coupled to only one word line and one bit line in said memory, said input field effect transistor being controlled to charge and discharge the capacitance of said another field effect transistor through said input transistor to write information in said cell;

(c) said another field effect transistor being nonconductive regardless of the charge stored therein in the absence of a signal on said word line;

(d) and said word line applying a signal to said other transistor to read out information from said cell.

12

16. The memory of claim 15 wherein each of said cells includes a third field effect transistor having its gate electrode and one of its terminals connected to the gate electrode of said another field effect transistor and having its other terminal connected to said bit line for said cell.

17. The memory of claim 15 wherein each of said transistors includes source and drain terminals and a gate electrode, one of said terminals of said input transistor being connected to the gate electrode of said another transistor, and said word line being connected to the gate electrode of said input transistor and to one of the terminals of said another transistor.

18. The memory of claim 17 including means for applying a signal of one polarity to said word line to control writing in said cell and a signal of opposite polarity to control reading in said cell.

19. An integrated circuit memory including a plurality of memory cells each coupled to at least one of a plurality of word lines for said memory and at least one of a plurality of bit lines for said memory, each said cell comprising:

(a) an input transistor having first and second regions connected to first and second terminals for the transistor and a third region between said first and second regions coupled to a control terminal to which signals are applied for controlling current flow in either direction between said first and second terminals;

(b) a storage element exhibiting capacitance;

(c) said word and bit lines coupled to said transistor to write information in said cell by charging the capacitance of said storage element through said transistor to cause said cell to assume a first information representing state and to discharge the capacitance of said storage element through said transistor to cause said cell to assume a second information representing state.

20. The memory of claim 19 wherein said storage element is a capacitor having first and second electrodes, one of which is connected to said first terminal of said transistor, and wherein information stored in said capacitor is read out by discharging said capacitor through said transistor.

21. The memory of claim 19 wherein said input transistor is a field-effect transistor and said storage element is another field effect transistor.

References Cited

UNITED STATES PATENTS

3,025,411 3/1962 Rumble ---------- 340—173

TERRELL W. FEARS, *Primary Examiner.*

The History of DRAM Circuit Designs —At the Forefront of DRAM Development—

Kiyoo Itoh, Hitachi Ltd., kiyoo.itoh.pt@hitachi.com

1. Introduction

Dynamic random-access memory (DRAM) has been the only high-density RAM used for over 30 years despite many attempts to replace it. Still contributing to IT advances, it has achieved an unprecedented six-fold increase in memory capacity in the last three decades, from the 1-Kbit level in 1970 to the 1- to 4-Gbit level today, as shown in Figure 1 [1]. Such rapid progress, however, would have been impossible without the implementation of many inventions and innovative technologies and the efforts of many talented people. The one-transistor one-capacitor cell (the 1-T cell) invented by Robert Dennard [2], and supported by his scaling theory [3], has played a key role. Over my career, I have also contributed to this progress by being fully involved in developing DRAM technologies.

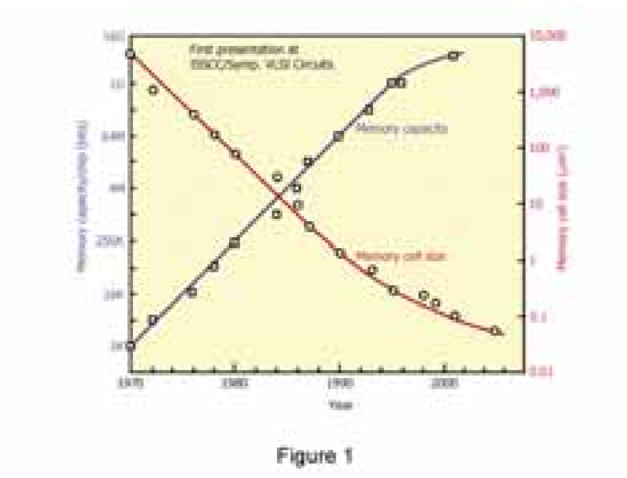


Figure 1. Trends in the memory cell size and memory capacity of DRAMs [1].

The first production of semiconductor memory announced by Intel and IBM in 1970 had a profound impact on my research at Hitachi Ltd. On the side, I bought the hottest DRAM samples and evaluated them to judge how DRAMs would impact Hitachi mainframe computers, while still being involved in magnetic memory device/system design. Eventually, however, I was forced to change my research field from magnetic thin-film memory to semiconductor memory. This change was so exceptionally sudden and difficult, I felt like a victim of fate. Looking back, however, I realize how fortunate I was to have witnessed such an advancement of DRAMs. In any event, I started my career as a DRAM designer at the end of 1972 with a 4-Kbit DRAM. Then, as the lead designer of the first prototype for each of eight successive generations of Hitachi DRAMs ranging from 4- Kbits to 64 Mbits, I was constantly faced with the challenge of breaking through the limits on each consecutive generation. Fortunately, we eventually overcame the difficulties with our best efforts. It is quite impressive that such painful and struggling developments can now be plotted as a smooth line on a graph like that shown in Figure 1.

This paper describes the history of DRAM circuit designs from its advent in 1970 to the present, based on my career at the forefront of DRAM development. More detail can be seen in references [4, 5].

2. In the Cradle of DRAM (1970s)

The 1970s was a decade in which MOS DRAM became firmly established as the technology for main memory, and also became the MOSFET technology driver. The dawn of the LSI era using MOSFET technology came in 1970, marked by the launch of the 1-Kbit DRAM, named 1103 by Intel Corporation. At that time, it was anticipated that magnetic memory, which had a large slice of the memory market, would eventually be replaced by DRAM. In the race to develop DRAM, companies enthusiastically aimed at developing products that would bring them wealth and success. However, it would not be until the mid-1970s that such products would start appearing on the market. It was normal in those early years to find a kaleidoscopic variety of product specifications and technologies provided by various manufacturers. For example, in the 1-Kbit generation, utilizing the high speed of n-channel MOSTFETs (nMOSTs) a manufacturer used a memory cell with four nMOSTs. In contrast, utilizing the low leakage of p-channel MOSFETs (pMOSTs), despite their slow speed, Intel used a memory cell with three pMOSTs. However, nMOS technology at that time had not matured, and production of this memory cell eventually halted due to an uncontrollable leakage problem in the cell. Moreover, samples were never released on time, and when they finally were released and evaluated, they were found to have a narrow voltage margin. In 1974, when nMOS 4-Kbit DRAM was starting to be developed, once a manufacturer switched to the 1-T cell offering a higher density, other manufacturers then immediately followed. Doubts soon began to arise about using this underdeveloped technology as a result of its problems, even though a method using a cross-coupled differential sense amplifier for sensing/restoring had been presented at the 1972 ISSCC [6].

In fact, sophisticated technology was necessary for the stable operation of the 1-T cell due to the cell's inherent features [5]. This is the case even for modern 1-T-cell DRAMs using a half-V_{DD} bit-line (BL) precharging scheme and a cross-coupled CMOS sense amplifier, as shown in Figure 2.

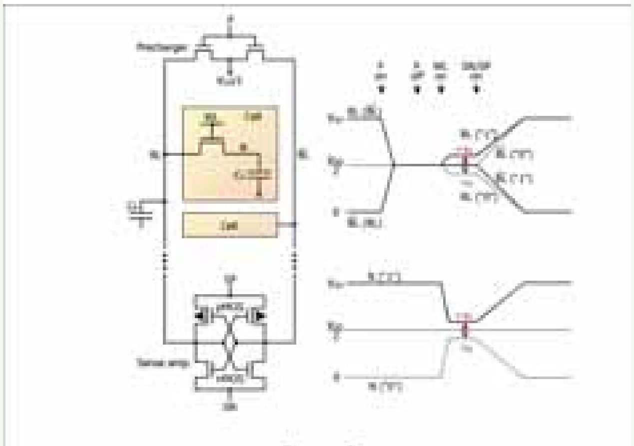


Figure 2

Figure 2. The read, amplification, and restoring of the 1-T cell. The signal voltage (v_S) is discriminated and amplified with another BL as a reference. The amplified signal is then restored at the cell node (N). $v_S = (V_{DD}/2)C_S/(C_S + C_B)$.

After precharging BLs at $V_{DD}/2$, the word-line (WL) is activated so that a signal voltage (v_S) is developed on the floating BL, as a result of charge sharing of the cell node and BL. Unfortunately, it is small (usually 100-200 mV) despite a high V_{DD} (1-5 V) because the cell capacitance (C_S = 20-50 fF) is much smaller than the BL capacitance (C_B = 50-600 fF). A small C_S and a large C_B result from the need for a small cell size and for connecting a large number (128-512) of cells to a BL, respectively. In addition, the signal voltage is floating. Thus, the operation is susceptible to noise. In any event, the original voltage (V_{DD} or 0 V) at the cell node collapses to around $V_{DD}/2$. The destructive readout characteristics thus necessitate successive amplification and restoring. The circuit for the operations must be simple enough to be laid out within the small pitch of BLs while minimizing noise generation from the circuit itself. In fact, for modern DRAMs it is the CMOS sense amplifier that meets the requirement. Here, the amplification and restoring are simultaneously performed on many BLs along the WL at a large voltage swing of $V_{DD}/2$, thus causing various kinds of noise in the memory-cell array via parasitic capacitances during the operations. In the early 1970s, circuit and noise-reduction techniques to cope with the problems were not available.

Just as feared, the resulting samples were not satisfactory for users. After many disappointments, it was not until the 16-Kbit generation, between 1976 and 1978, that the first acceptable samples appeared. Also, specifications were standardized (for example, the package pin-count was decreased from 22 to 16) and a considerable number of technologies were discarded. Consequently, the 1-T cell using double polysilicon layers [7], low-power dynamic circuit configurations for logic gates and sense amplifiers [8], and the address-multiplexing scheme (halving the address package pin-count) [7] became standard. Despite these steps forward, in 1978, the so-called "soft-error problem" (i.e., non-destructive failures of memory cells caused by alpha-particle irradiation or cosmic-ray irradiation) was revealed [9]. Even though a chip coating with polyimide and the purification of relevant materials partly resolved the problem, further technological development was needed. In addition, from the user viewpoint, the use of three external supply voltages (12, 5, and –5 V) remained unwieldy.

3. In the Rush of Innovative DRAM Technologies (1980s)

The 1980s brought an era in which proposals of breakthrough DRAM technologies were rushed, and the DRAM market was drastically larger than in the previous decade. During the 64-Kbit generation around 1980, there were major advancements in product specifications and technologies, and the above-mentioned three power supplies were replaced by a single 5-V power supply [10] by using an on-chip substrate bias generator. The folded-bit-line (BL) arrangement invented by K. Itoh [11] in 1974 (the de-facto standard cell nowadays) was introduced in order to cancel array noise. In the conventional open-BL arrangement, two BLs in a pair connected to a differential sense amplifier are implemented separately on two array conductors (see Fig. 3(a)), causing electrical imbalances between the lines. Moreover, if voltage bounces at the conductors are different, different voltages are coupled to the BLs via conductor-BL parasitic capacitances. Consequently, a differential noise that cannot be cancelled by the amplifier is generated between the pair of BLs. On the contrary, in the folded-BL arrangement, shown in Fig. 3(b), the two BLs run close to one another and are parallel on the same conductor, enabling the same voltage to be coupled to the BLs and thus cancelled by the amplifier.

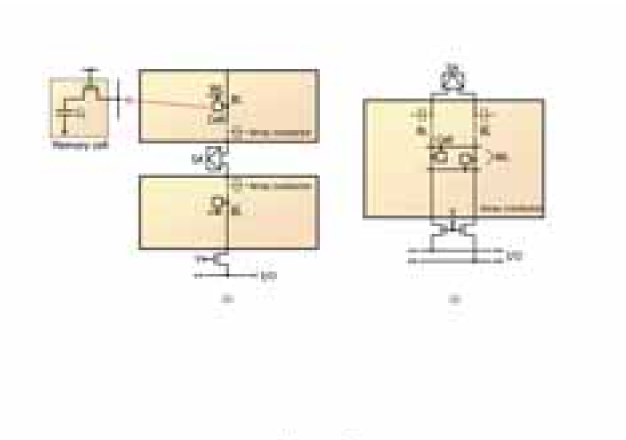


Figure 3

Figure 3. Configurations of (a) open BL arrangement and (b) folded-BL arrangement. SA; Sense amplifier, Y; Column select-line, I/O; Common data-in- and data-out-lines.

In the following 256-Kbit generation, "bootstrapping" and the redundancy technique [5] were rapidly accepted throughout the industry. During this generation, around 1985, prices of DRAMs collapsed because of fierce competition. Despite this problem, however, technical developments continued apace [5]. In particular, a partial activation of multi-divided BLs for low-power array, a highly reliable pMOST-output word driver, and a half-V_{DD} capacitor plate for doubling cell capacitance were introduced. Another significant introduction was a half-V_{DD} BL precharging scheme [5] for reducing power dissipation and array noise and for providing stable sensing without problematic dummy cells. Moreover, a milestone was the on-chip voltage down-converter (VDC) scheme [5, 12], which ensured reliability in scaled devices while reducing power dissipation and maintaining an external power supply for several generations. The details follow.

Standard power-supply voltage is dictated by system supply, which is not scaled down fast enough to equal advances in device miniaturization. Therefore, a voltage-down converter (see Fig. 4) that can bridge the supply gap between the system and internal core-circuit devices needs to be integrated on the chip. The converter can adjust the converted voltage (V_{DL}) in accordance with the breakdown voltage lowering of the ever-miniaturized devices, while maintaining the external power supply voltage (V_{DD}) for several generations. In practice, the aging (or burn-in) stress test, which enables us to quickly remove potential defects by applying a high stress voltage and high temperature, must be made possible by raising the V_{DD} above the normal operation voltage. The VDC was proposed for a 1-Mbit nMOS DRAM [12] in 1984. However, after taking into consideration the loop stability of the DRAM load that dynamically changes at a large voltage swing, the VDC could successfully be implemented in 16-Mbit DRAM products in the early 1990s. Nowadays, the VDC has become an industry standard for DRAMs as well as for microcontrollers. Another milestone in the 1980s was the use of CMOS technology, which enables us to use simple and low power circuits. Although the concept of CMOS DRAM [13] was proposed in 1980, it was not industrialized until the late 1980s for 1-Mbit DRAMs. CMOS technology has since been indispensable.

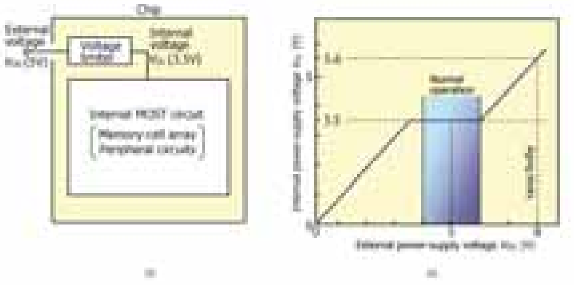


Figure 4

Figure 4. (a) On-chip voltage down-converter scheme, and (b) aging (burn-in) test with a high stress voltage [5].

4. Toward High-Speed and Low-Voltage DRAMs (1990s-present)

In the early 1990s, a major transition once again took place in the 4-Mbit generation with the introduction of vertical trench and stacked capacitors [5]. Both capacitors were, and still are, indispensable for providing a large signal voltage with a large cell capacitance, although there had been controversial arguments about their performance and scalability. Memory capacity continued to grow due to high-density fabrication process technology guided by Dennard's scaling theory. After memory capacity at the research and development level reached the 1-4Gbit level in the mid-1990s, however, high speed with doubled memory capacity per generation became the focus for the development of DRAM, rather than increase in memory capacity by quadrupling it in each generation. This focus resulted from the need for a small increment unit of memory capacity in PC systems, bridging the more prominent DRAM-processor performance gap, lower bit cost, and shorter lead-time required for advanced process technology. The result of these changes was the emergence of high-throughput DRAMs [5], as exemplified by a pipe-lined DRAM, block transfer oriented protocol DRAM (the so-called "Rambus DRAM"), and synchronous DRAM (SDRAM). Driven by increasing system clocks and scaled devices, high-throughput DRAM progress has continued into the 21st century. Pipe-lined/interleaving techniques with multi-bank, high-speed low-voltage swing I/O interfaces and wide I/Os combined with high-density packaging, a double data rate (DDR) technique that aligns read data at both edges of the external clock, a delay-locked loop (DLL) that aligns data with the external clock, and even on-chip termination have all been widely used in high-speed DRAM products. Consequently, by the end of 2007, DRAM evolved to a 1.5-V 1.6-Gbit/s/pin (800-MHz clock) 1-Gbit DDR SDRAM using an 80-nm triple-metal dual-gate poly CMOS process [17].

Even in the 1990s, DRAM was the technology driver of low-voltage CMOS circuits. The early 1990s saw the advent of low-voltage (≤1.5 V) CMOS circuits. Y. Nakagome et al. [14] pioneered the development of low-voltage CMOS LSIs with a 1.5-V 50-ns 64-Mbit DRAM. This was landmark work because the chip was not only the first 64-Mbit DRAM but also the first 1.5-V DRAM when 5 V was still the standard power being used. The 1.5-V DRAM was a major innovation, driven by a growing interest in portable and battery-operated systems. This DRAM required the use of many low-voltage circuits in order to resolve problems pertaining to low-voltage operations. One particular problem (and a major obstacle) was, and still is, the subthreshold current (leakage). This is because the threshold voltage (V_T) of MOSTs for low-voltage high-speed CMOS LSIs must be lowered by scaling down the MOSTs and lowering their operating voltage, causing an exponential increase in the leakage (i.e., the current flowing between the source and drain even though the gate voltage is lower than V_T). The resultant leakage currents flowing even in CMOS circuits unacceptably increase the stand-by current of a chip. Eventually, leakage dominates even the active current, as expected in Figure 5 [15], resulting in a loss of the low-power advantage of CMOS circuits that we take for granted today. Simple and effective schemes [1, 5] to reduce leakage are to back-bias the MOST in various ways, such as the offset gate-source driving and stacking of the switched-source impedance (SSI), and use of the power switch. In particular, the SSI is most suitable for a memory chip consisting of large number of iterative circuit blocks that dominate the total active leakage of the chip. As early as 1993, the SSI was expected to reduce the active current of a hypothetical 1.0-V 16-Gbit DRAM [15] dominated by leakage to one-tenth (1180 mA to 116 mA). Although these schemes were all proposed by DRAM designers, they have made a strong impact on subsequent developments of SRAMs and logic circuits in MPUs [16]. Lower-voltage DRAMs, however, are facing a challenge, as in other LSIs. This is the variability problem (e.g., speed variations due to V_T variations in a chip) that will become more prominent with device miniaturization, especially for many sense amplifiers consisting of small flip-flops.

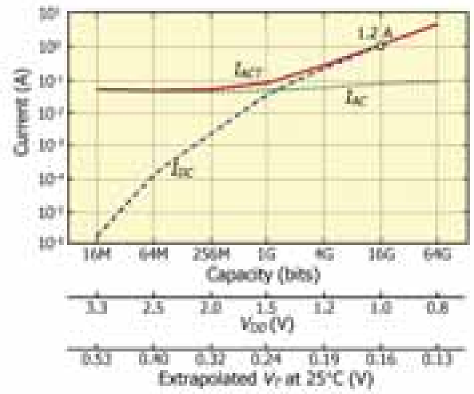


Figure 5

Figure 5 Trends in the estimated active current of DRAMs [15]. I_{DC}; Subthreshold current, I_{AC}; Charging current of capacitors, I_{ACT}; Total active current. Cycle time = 180 ns, T = 75_C, Subthreshold swing = 97 mV/decade.

A recent movement can also be seen in developments of high-density DRAM cell structures aiming at the $4F^2$ area (F = device feature size) instead of conventional 6-8F^2 cells. This trend is being driven by the objective of reducing bit cost as device scaling becomes more complicated and expensive for deep-sub-100-nm technologies. A good example is the floating-body silicon-on-insulator (SOI) one-transistor gain cell accepting logic compatible process [18]. The SOI cell consists of an nMOST built on a partially depleted SOI. The floating body is used as an electrical charge storage node.

5. Conclusion

In summary, DRAM has enabled us to fabricate computers, handheld equipment, and almost everything with electrical components with a dramatically low bit-cost and high performance. But how about the future? Can we overcome problems such as the ever-more difficult fabrication process and the variability issue in the deep-sub-100-nm era? How and when can we get the $4F^2$ DRAM cell? Moreover, how far can we go with the 1-T cell? Nobody knows for sure. But that is what makes integrated circuit research and development so exciting [19].

References

[1] K. Itoh, M. Horiguchi, and H. Tanaka, Ultra-Low-Voltage Nano-Scale Memories, Springer, Aug. 2007.

[2] R.H. Dennard, USP-3387286, June 4, 1968.

[3] R.H. Dennard, F.H. Gaensslen, H.N. Yu, V.L. Rideout, E. Bassous, and A.R. LeBlanc, "Design of Ion Implanted MOSFET's with Very Small Physical Dimensions", IEEE J. Solid-State Circuits, Vol. SC-9, pp. 256-268, Oct. 1974.

[4] L.M. Terman, "Memory at ISSCC", ISSCC Commemorative Supplement to the Digest of Technical Papers, pp.91-111, Feb. 1993.

[5] K. Itoh, VLSI Memory Chip Design, Springer-Verlag, NY, 2001.

[6] K.U. Stein, A. Sihling, E. Doering, "Storage Array and Sense/Refresh Circuit for Single-Transistor Memory Cells", ISSCC Dig. Tech. Papers. pp. 56-57, Feb. 1972.

[7] C.N. Ahlquist, J.R. Breivogel, J.T. Koo, J.L. McCollum, W.G. Oldham, and A.L. Renninger, "A 16K Dynamic RAM", ISSCC Dig. Tech. PapersÅCpp. 128-129, Feb. 1976.

[8] P.R. Shroeder and R.J. Proebsting, "A 16Kx1 Bit Dynamic RAM", ISSCC Dig. Tech. Papers, pp. 12-13, Feb. 1977.

[9] T.C. May, M.H. Woods, "A New Physical Mechanism for Soft Errors in Dynamic Memories", Proc. Reliability Physics Symp., pp. 33-40, April 1978.

[10] K. Itoh, R. Hori, H. Masuda, Y. Kamigaki, H. Kawamoto, and H. Katto, "A single 5V 64K dynamic RAM", ISSCC Dig. Tech. Papers, pp. 228-229, Feb. 1980.

[11] K. Itoh, USP-4044340, Dec.29, 1975.

[12] K. Itoh, R. Hori, J. Etoh, S. Asai, N. Hashimoto, K. Yagi and H. Sunami, "An Experimental 1Mb DRAM with On-Chip Voltage Limiter", ISSCC Dig. Tech. Papers, p. 282-283, Feb. 1984.

[13] K. Shimohigashi, H. Masuda, Y. Kamigaki, K. Itoh, N. Hashimoto, and E. Arai, "An n-well CMOS Dynamic RAM," IEDM Dig. Tech. Papers, pp. 835-836, Dec. 1980.

[14] Y. Nakagome, Y. Kawamoto, H. Tanaka, K. Takeuchi, E. Kume, Y. Watanabe, T. Kaga, F. Murai, R. Izawa, D. Hisamoto, T. Kisu, T. Nishida, E. Takeda, and K. Itoh, "A 1.5-V Circuit Technology for 64Mb DRAMs", Symp. VLSI Circuits Dig., Tech. Papers, pp. 17-18, June 1990.

[15] T. Sakata, K. Itoh, M. Horiguchi, and M. Aoki, "Two-Dimensional Power-Line Selection Scheme for Low Subthreshold-Current Multi-Gigabit DRAM's", IEEE J. Solid-State Circuits, Vol. 29, No. 8, pp. 887-894, August 1994.

[16] G. E. Moore, "No Exponential is Forever: But "Forever" Can Be Delayed!", ISSCC Dig. Tech. Papers, pp. 20-23, Feb. 2003.

[17] Y.K. Kim, Y.J. Jeon, B.H. Jeong, N.W. Heo, S.B. Chang, H.G. Jung, D.Y. Kim, H.J. Chung, C.S. Kim, S.B. Ko, K.H. Kyung, J.H. Yoo, and S.I. Cho, "A 1.5V, 1.6Gb/s/pin, 1Gb DDR3 SDRAM with an Address Queuing Scheme and Bang-Bang Jitter Reduced DLL Scheme", Symp. VLSI Circuits Dig. Tech. Papers, pp. 182-183, June 2007.

[18] T. Ohsawa, K. Fujita, T. Higashi, Y. Iwata, T. Kajiyama, Y. Asao, and K. Sunouchi, "Memory Design Using a One-Transistor Gain Cell on SOI", IEEE J. Solid-State Circuits, Vol.37, No.11, pp. 1510-1522, Nov. 2002.

[19] IEEE Spectrum, p.29, Oct. 2007.

About the Author

Kiyoo Itoh received the B.S. and Ph.D. Degrees in Electrical Engineering from Tohoku University, Japan, in 1963 and 1976. He is currently a Hitachi Fellow. He was a Visiting MacKay Lecturer at U.C. Berkeley in 1994, a Visiting Professor at the University of Waterloo in 1995, and a Consulting Professor at Stanford University in 2000-2001. He was a Member of the IEEE Fellow Committee from 1999 to 2002, and an elected AdCom Member of IEEE Solid-State Circuits Society from 2001 to 2003. He is a Distinguished Lecturer of the IEEE Solid-state Circuits Society.

Since 1972 he has led low-power/low-voltage RAM circuits at Hitachi Ltd: He was the lead designer of the first prototype for eight generations of Hitachi DRAMs ranging from 4-Kbits to 64-Mbits. In the course of these developments, in 1974 he invented the concept of the folded data-line (i.e., bit-line) arrangement, which uses a pair of balanced data lines to eliminate various noise components, and presented the architecture for a 64-Kbit DRAM at the 1980 ISSCC. This architecture has since been adopted for nearly all DRAM chips. He went on to develop high-density DRAM devices and low-power/low-voltage DRAM circuits and array architectures: triple-well substrate structures, advanced three-dimensional capacitors, pipe-lined DRAMs, on-chip substrate-bias generators, half-V_{DD} sensing, on-chip voltage-down converters enabling the aging (burn-in) stress test, the PMOS word driver, so-called direct sensing, multi-divided data-line architectures, transposed data-lines, low-voltage charge pump, and stress-voltage tolerated I/O circuits. Many of them have become de-facto standards. In addition, as a pioneer he initiated circuit inventions and developments as early as 1988 to reduce the subthreshold current of MOSFETs even for the active mode, which is highlighted today in low-voltage CMOS LSI designs. Typical examples of the reduction circuits are multi-threshold (V_T) CMOS logic, various gate-source (self and offset) back-biasing schemes, multi-divided power line schemes, and power switches that we take for granted today.

Dr. Itoh holds over 420 patents in Japan and the US. He has authored four books and three book chapters on memory designs, and contributed over 130 technical papers and presentations, many of them invited, to IEEE journals and conference proceedings.

Dr. Itoh has won many honors, including the IEEE Paul Rappaport Award in 1984, the Best Paper Award of ESSCIRC90, the 1993 IEEE Solid-State Circuits Award, and the 2006 IEEE Jun-ichi Nishizawa Medal. He is an IEEE Fellow. In Japan, his awards include the National Invention Award Prize of the Patent Attorney's Association of Japan 1989, the Commendation by the Minister of State for Science and Technology (Person of Scientific and Technological Merits 1997), and the National Medal of Honor with Purple Ribbon from the Japanese Emperor (2000).

Introduction to “In Quest of the Joy of Creation”

Kiyoo Itoh. December 17, 2007

This article covers my life of research spanning 42 years and emphasizes DRAM developments since the early 1970s. I have been lucky in consistently driving cutting-edge technologies with my continuous and deep dedication to influential developments.

Looking back, the announcement of the first production of semiconductor memory by Intel and IBM in 1970 had a profound impact on my research. At the young age of thirty, I was entrusted with developing a 4-Kbit DRAM for Hitachi Ltd. in 1972 without any knowledge about semiconductors, and had to change my research field from magnetic thin-film memory to semiconductor memory. As the lead designer of the first prototype for each of eight successive generations of Hitachi DRAMs ranging from 4 Kbits to 64 Mbits, I was constantly faced with the challenge of breaking through the limits on each consecutive generation. After failing four times in the face of global competition, Hitachi finally won the race with our 64-Kbit DRAM. We eventually overcame the difficulties with our best efforts.

This article also covers my way of thinking about invention, exemplified by three representative technologies that I and my team invented and brought up to product applications under severe competition during different phases of growth in our relative technological power compared to our competitors. These technologies are

- the folded data-line arrangement cell (which was invented in the era when we were catching up with others in terms of technology);
- the voltage-down converter (which was invented in the era when we were getting stronger enough to compete as equal with others);
- the leakage-reduction circuits (which was invented in the era when we had taken the lead of the pack).

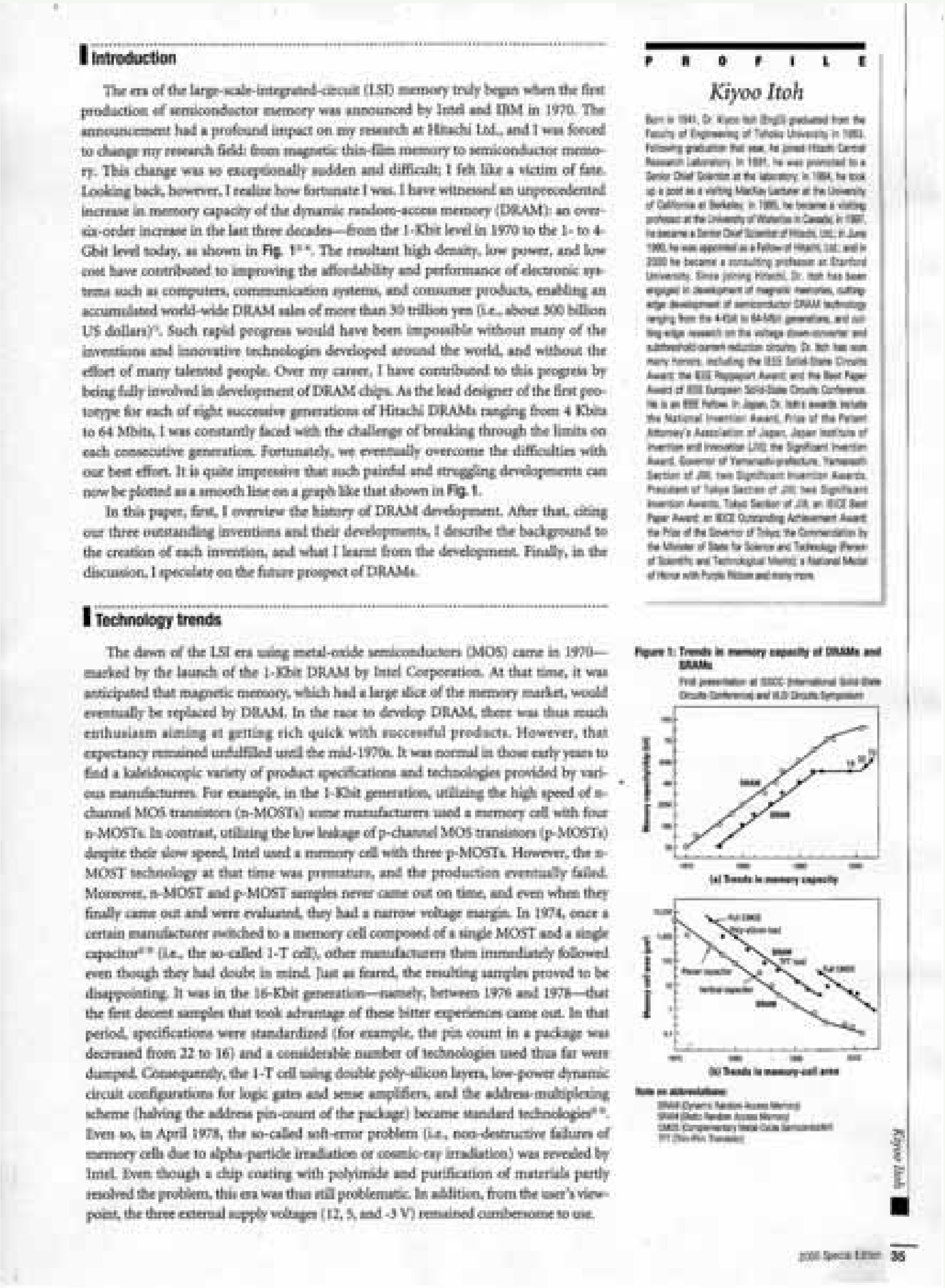
This article also includes how joyous technological creation was for me. Without question, this “joy of creation” exists in our everyday struggles through trial and error in the work place. When a small idea is born in a flash under the utmost stress, and it is successively polished up and incorporated into finished products, one feels a sense of unquestionable joy and fulfillment. Moreover, when such ideas are objectively recognized throughout society, our job satisfaction is maximized. To sum up, starting with a challenge, then by focusing on solutions and putting them into practice, anyone can capture this joy.

I will be delighted if this article based on my personal experience inspires engineers and managers facing challenges in the future.

In Quest of the Joy of Creation

Kiyoo Itoh, Hitachi, kiyoo.itoh.pt@hitachi.com

Reprinted from "Innovate the Future," 2005 Hitachi Hyoron Special Edition, pp. 34-39, Hitachi Hyoronsha, Tokyo, Japan.



Introduction

The era of the large-scale-integrated-circuit (LSI) memory truly began when the first production of semiconductor memory was announced by Intel and IBM in 1970. The announcement had a profound impact on my research at Hitachi Ltd., and I was forced to change my research field: from magnetic thin-film memory to semiconductor memory. This change was so exceptionally sudden and difficult; I felt like a victim of fate. Looking back, however, I realize how fortunate I was. I have witnessed an unprecedented increase in memory capacity of the dynamic random-access memory (DRAM): an over-six-order increase in the last three decades—from the 1-Kbit level in 1970 to the 1- to 4-Gbit level today, as shown in **Fig. 1**[1)-4)]. The resultant high density, low power, and low cost have contributed to improving the affordability and performance of electronic systems such as computers, communication systems, and consumer products, enabling an accumulated world-wide DRAM sales of more than 30 trillion yen (i.e., about 300 billion US dollars)[5)]. Such rapid progress would have been impossible without many of the inventions and innovative technologies developed around the world, and without the effort of many talented people. Over my career, I have contributed to this progress by being fully involved in development of DRAM chips. As the lead designer of the first prototype for each of eight successive generations of Hitachi DRAMs ranging from 4 Kbits to 64 Mbits, I was constantly faced with the challenge of breaking through the limits on each consecutive generation. Fortunately, we eventually overcome the difficulties with our best effort. It is quite impressive that such painful and struggling developments can now be plotted as a smooth line on a graph like that shown in **Fig. 1**.

In this paper, first, I overview the history of DRAM development. After that, citing our three outstanding inventions and their developments, I describe the background to the creation of each invention, and what I learnt from the development. Finally, in the discussion, I speculate on the future prospect of DRAMs.

Technology trends

The dawn of the LSI era using metal-oxide semiconductors (MOS) came in 1970—marked by the launch of the 1-Kbit DRAM by Intel Corporation. At that time, it was anticipated that magnetic memory, which had a large slice of the memory market, would eventually be replaced by DRAM. In the race to develop DRAM, there was thus much enthusiasm aiming at getting rich quick with successful products. However, that expectancy remained unfulfilled until the mid-1970s. It was normal in those early years to find a kaleidoscopic variety of product specifications and technologies provided by various manufacturers. For example, in the 1-Kbit generation, utilizing the high speed of n-channel MOS transistors (n-MOSTs) some manufacturers used a memory cell with four n-MOSTs. In contrast, utilizing the low leakage of p-channel MOS transistors (p-MOSTs) despite their slow speed, Intel used a memory cell with three p-MOSTs. However, the n-MOST technology at that time was premature, and the production eventually failed. Moreover, n-MOST and p-MOST samples never came out on time, and even when they finally came out and were evaluated, they had a narrow voltage margin. In 1974, once a certain manufacturer switched to a memory cell composed of a single MOST and a single capacitor[6),7)] (i.e., the so-called 1-T cell), other manufacturers then immediately followed even though they had doubt in mind. Just as feared, the resulting samples proved to be disappointing. It was in the 16-Kbit generation—namely, between 1976 and 1978—that the first decent samples that took advantage of these bitter experiences came out. In that period, specifications were standardized (for example, the pin count in a package was decreased from 22 to 16) and a considerable number of technologies used thus far were dumped. Consequently, the 1-T cell using double poly-silicon layers, low-power dynamic circuit configurations for logic gates and sense amplifiers, and the address-multiplexing scheme (halving the address pin-count of the package) became standard technologies[8),9)]. Even so, in April 1978, the so-called soft-error problem (i.e., non-destructive failures of memory cells due to alpha-particle irradiation or cosmic-ray irradiation) was revealed by Intel. Even though a chip coating with polyimide and purification of materials partly resolved the problem, this era was thus still problematic. In addition, from the user's viewpoint, the three external supply voltages (12, 5, and -3 V) remained cumbersome to use.

P R O F I L E

Kiyoo Itoh

Born in 1941, Dr. Kiyoo Itoh (Eng.D) graduated from the Faculty of Engineering of Tohoku University in 1963. Following graduation that year, he joined Hitachi Central Research Laboratory. In 1981, he was promoted to a Senior Chief Scientist at the laboratory. In 1984, he took up a post as a visiting Mackay Lecturer at the University of California at Berkeley. In 1985, he became a visiting professor at the University of Waterloo in Canada. In 1997, he became a Senior Chief Scientist of Hitachi, Ltd. In June 1999, he was appointed as a Fellow of Hitachi, Ltd., and in 2000 he became a consulting professor at Stanford University. Since joining Hitachi, Dr. Itoh has been engaged in development of magnetic memories, cutting-edge development of semiconductor DRAM technology ranging from the 4-Kbit to 64-Mbit generations, and cutting-edge research on the voltage down-converter and subthreshold-current reduction circuitry. Dr. Itoh has won many honors, including the IEEE Solid-State Circuits Award, the IEEE Rappaport Award, and the Best Paper Award of IEEE European Solid-State Circuits Conference. He is an IEEE Fellow. In Japan, Dr. Itoh's awards include the National Invention Award, Prize of the Patent Attorney's Association of Japan, Japan Institute of Invention and Innovation (JIII); the Significant Invention Award, Governor of Yamanashi-prefecture, Yamanashi Section of JIII; two Significant Invention Awards, President of Tokyo Section of JIII; two Significant Invention Awards, Tokyo Section of JIII; an IEICE Best Paper Award; an IEICE Outstanding Achievement Award; the Prize of the Governor of Tokyo; the Commendation by the Minister of State for Science and Technology (Person of Scientific and Technological Merit); a National Medal of Honor with Purple Ribbon and many more.

Figure 1: Trends in memory capacity of DRAMs and SRAMs

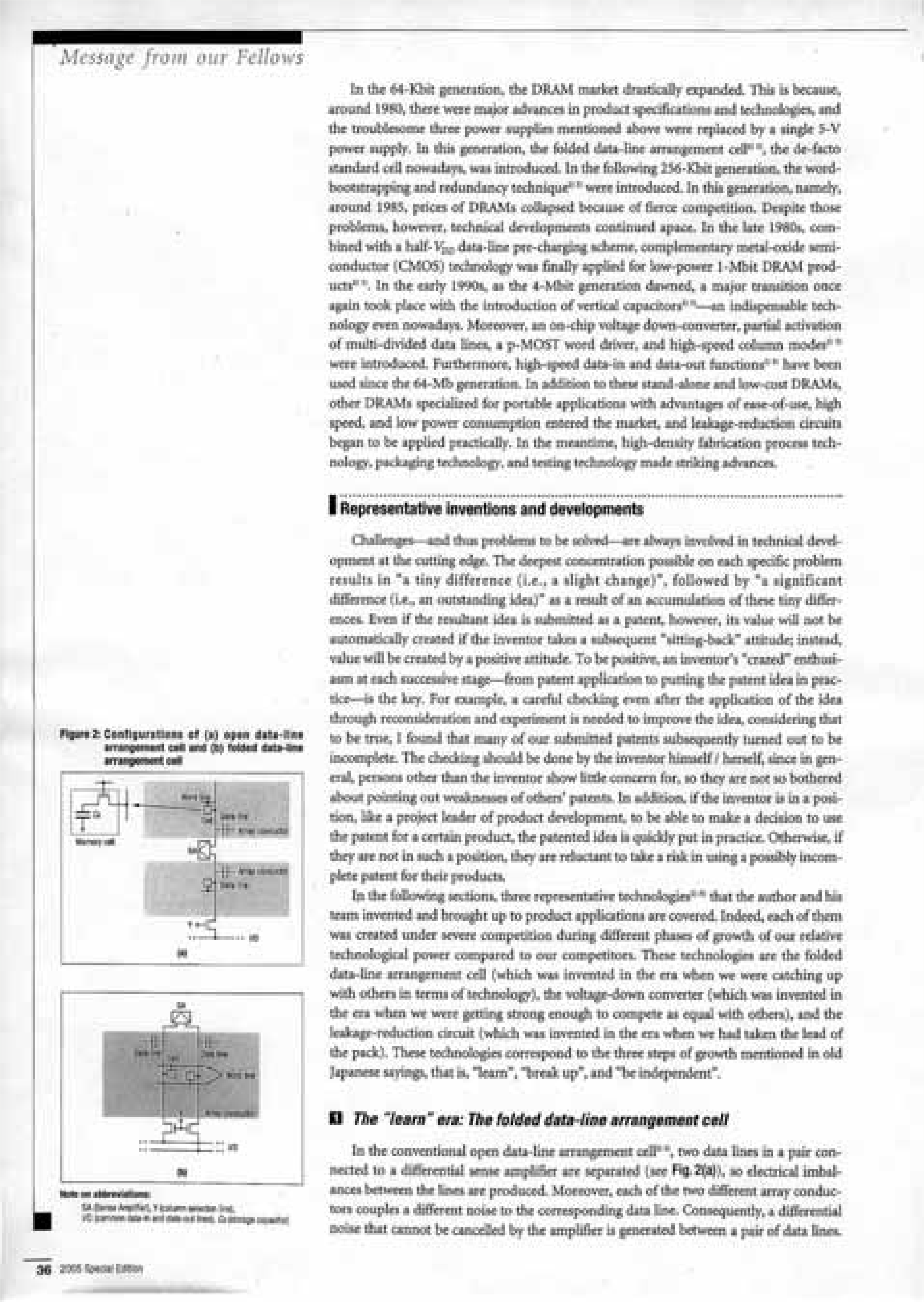
First presentation at ISSCC (International Solid-State Circuits Conference) and VLSI Circuits Symposium

(a) Trends in memory capacity

(b) Trends in memory-cell area

Note on abbreviations:

DRAM (Dynamic Random-Access Memory)
SRAM (Static Random-Access Memory)
CMOS (Complementary Metal-Oxide Semiconductor)
TFT (Thin-Film Transistor)



In the 64-Kbit generation, the DRAM market drastically expanded. This is because, around 1980, there were major advances in product specifications and technologies, and the troublesome three power supplies mentioned above were replaced by a single 5-V power supply. In this generation, the folded data-line arrangement cell, the de-facto standard cell nowadays, was introduced. In the following 256-Kbit generation, the word-bootstrapping and redundancy technique were introduced. In this generation, namely, around 1985, prices of DRAMs collapsed because of fierce competition. Despite those problems, however, technical developments continued apace. In the late 1980s, combined with a half-V_{DD} data-line pre-charging scheme, complementary metal-oxide semiconductor (CMOS) technology was finally applied for low-power 1-Mbit DRAM products. In the early 1990s, as the 4-Mbit generation dawned, a major transition once again took place with the introduction of vertical capacitors—an indispensable technology even nowadays. Moreover, an on-chip voltage down-converter, partial activation of multi-divided data lines, a p-MOST word driver, and high-speed column modes were introduced. Furthermore, high-speed data-in and data-out functions have been used since the 64-Mb generation. In addition to these stand-alone and low-cost DRAMs, other DRAMs specialized for portable applications with advantages of ease-of-use, high speed, and low power consumption entered the market, and leakage-reduction circuits began to be applied practically. In the meantime, high-density fabrication process technology, packaging technology, and testing technology made striking advances.

Representative inventions and developments

Challenges—and thus problems to be solved—are always involved in technical development at the cutting edge. The deepest concentration possible on each specific problem results in "a tiny difference (i.e., a slight change)", followed by "a significant difference (i.e., an outstanding idea)" as a result of an accumulation of these tiny differences. Even if the resultant idea is submitted as a patent, however, its value will not be automatically created if the inventor takes a subsequent "sitting-back" attitude; instead, value will be created by a positive attitude. To be positive, an inventor's "crazed" enthusiasm at each successive stage—from patent application to putting the patent idea in practice—is the key. For example, a careful checking even after the application of the idea through reconsideration and experiment is needed to improve the idea, considering that to be true, I found that many of our submitted patents subsequently turned out to be incomplete. The checking should be done by the inventor himself / herself, since in general, persons other than the inventor show little concern for, so they are not so bothered about pointing out weaknesses of others' patents. In addition, if the inventor is in a position, like a project leader of product development, to be able to make a decision to use the patent for a certain product, the patented idea is quickly put in practice. Otherwise, if they are not in such a position, they are reluctant to take a risk in using a possibly incomplete patent for their products.

In the following sections, three representative technologies that the author and his team invented and brought up to product applications are covered. Indeed, each of them was created under severe competition during different phases of growth of our relative technological power compared to our competitors. These technologies are the folded data-line arrangement cell (which was invented in the era when we were catching up with others in terms of technology), the voltage-down converter (which was invented in the era when we were getting strong enough to compete as equal with others), and the leakage-reduction circuit (which was invented in the era when we had taken the lead of the pack). These technologies correspond to the three steps of growth mentioned in old Japanese sayings, that is, "learn", "break up", and "be independent".

1 The "learn" era: The folded data-line arrangement cell

In the conventional open data-line arrangement cell, two data lines in a pair connected to a differential sense amplifier are separated (see Fig. 2(a)), so electrical imbalances between the lines are produced. Moreover, each of the two different array conductors couples a different noise to the corresponding data line. Consequently, a differential noise that cannot be cancelled by the amplifier is generated between a pair of data lines.

Figure 2: Configurations of (a) open data-line arrangement cell and (b) folded data-line arrangement cell

Note on abbreviations:
SA (Sense Amplifier), Y (column selection line),
I/O (common data-in and data-out lines), Cs (storage capacitor)

On the contrary, in the folded data-line arrangement cell[1-3], shown in **Fig. 2(b)**, the two data lines are running closely and in parallel on the same conductor, enabling the same noise to be coupled to the data lines and thus be cancelled by the amplifier. Coupled with a half-V_{DD} data-line pre-charging scheme, the cell halves the data-line charging and discharging power while maintaining low noise. The cell is so superior that it has been used for the last 25 years for almost all DRAMs.

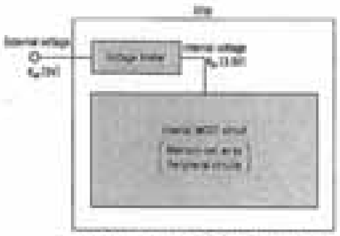
The cell invention I described above is evidence that even a late comer could become the top dog with exceptional inventions and developments. In 1974, the year I started to design DRAM as a team leader, a formidable technology gap in DRAMs existed between Japan and overseas. Under these circumstances, how did such an idea come up to me despite being a novice regarding semiconductors? The answer is that in addition to a sense of crisis caused by the technology gap and a sense of responsibility as a leader, my previous experience was favored. At that time, I had already been deeply involved in memory-device and system design using magnetic thin-film memory, and I had struggled with the poor signal-to-noise-ratio (S/N) of such a memory. On the contrary, other people did not possess such experience. Thus, applying my rich knowledge of the S/N, in the cradle of the DRAM era, I could quickly spot that a high S/N design is also important for DRAMs because it is common to any kind of memory. Subsequently, taking an analogy with the magnetic memory, I invented the folded-data-line arrangement cell as a solution. Therefore, despite having a solution for a hypothetical S/N problem in DRAMs without any experimental data on DRAMs, I could still fill out a patent application form including concrete and almost perfect descriptions of problems and solutions. Even during the then economic recession of Japan, I succeeded in persuading Hitachi to submit the patent in the US. Thanks to rapid patent processing inside Hitachi, the patent application was six months ahead of other companies' similar patents. Four years later, we had split the patent into 11 sub-patents, so we could cover more technical applications. Fortunately, I succeeded in persuading our managers to apply my patent idea to our 64-Kbit products despite some strong oppositions due to the lack of experimental data, since I was the leading expert on this technology for these products. It was the 64-Kbit DRAM that took the lion's share of the world market. After this success, the cell became firmly established throughout the world as the only memory-cell arrangement for subsequent DRAM products. This sequence of lucky events was quite simply miraculous.

■ *The "break up" era: The voltage-down converter*

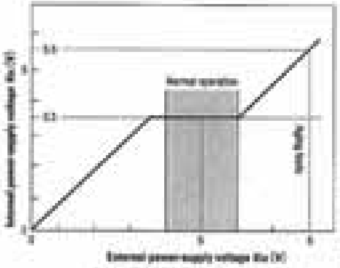
The standard power-supply voltage is dictated by the system supply that is not scaled down fast enough to keep up with advances in device miniaturizations. A voltage-down converter[4-6] (see **Fig.3**) that can bridge the supply gap between the system and internal core-circuit devices in a chip therefore needs to be integrated on the chip. The converter can adjust the converted voltage (V_{DL}) in accordance with the lowering of breakdown voltage of the ever-miniaturized devices, while keeping the external power supply voltage (V_{DD}) the same as long as possible. In practice, the aging (or burn-in) stress test, which quickly gets rid of potential defects by applying a high stress voltage and high temperature, must be made possible by raising V_{DD} above the normal operation voltage. In fact, starting with an n-MOS 1-Mbit DRAM in 1984, my group spent 11 years in successively improving the design to the perfect solution, resulting in as many as 33 international conference presentations and 32 related patents. And at the beginning of the 1990s, we finally succeeded in using the converter in our 16-Mbit DRAM. Nowadays, the converter and relevant technology has become an industry standard for DRAMs as well as microcomputers.

This development is a good example showing what the research and patent activities should be. If we had not been at the forefront of development of cutting-edge products, I could have not spotted the trend in the ever-larger supply-voltage gap mentioned above. Moreover, if we had not had constant experience of commercializing products up till then, I would not have realized the importance of the aging test. And if I had not been convinced of the importance of the basic concept of the converter, I would not have spent as long as 11 years with successive improvements of the invention through experiments. If I had not recognized that no one but the inventor can recognize the real value of a patent, I would not have dedicated to solving the problem when infringements occurred. The inventor knows or must know everything about his patents.

Figure 3: On-chip voltage down-converter enabling aging (i.e., burn-in) test with a high stress voltage

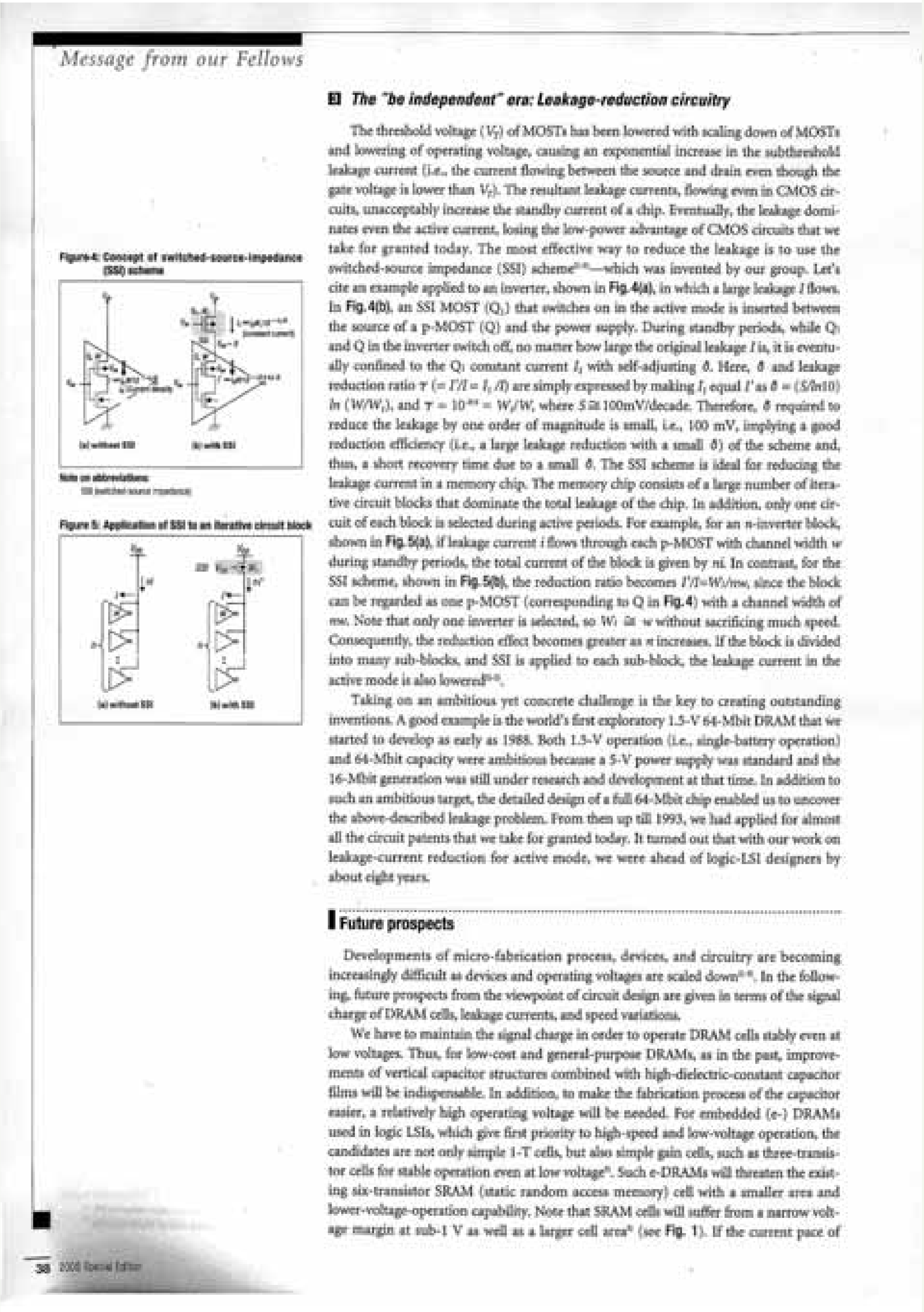


(a) On-chip voltage down-converter scheme



(b) Internal voltage characteristics

Kiyoo Itoh



Message from our Fellows

The "be independent" era: Leakage-reduction circuitry

The threshold voltage (V_T) of MOSTs has been lowered with scaling down of MOSTs and lowering of operating voltage, causing an exponential increase in the subthreshold leakage current (i.e., the current flowing between the source and drain even though the gate voltage is lower than V_T). The resultant leakage currents, flowing even in CMOS circuits, unacceptably increase the standby current of a chip. Eventually, the leakage dominates even the active current, losing the low-power advantage of CMOS circuits that we take for granted today. The most effective way to reduce the leakage is to use the switched-source impedance (SSI) scheme[2-8]—which was invented by our group. Let's cite an example applied to an inverter, shown in **Fig.4(a)**, in which a large leakage I flows. In **Fig.4(b)**, an SSI MOST (Q_1) that switches on in the active mode is inserted between the source of a p-MOST (Q) and the power supply. During standby periods, while Q_1 and Q in the inverter switch off, no matter how large the original leakage I is, it is eventually confined to the Q_1 constant current I_1 with self-adjusting δ. Here, δ and leakage reduction ratio τ ($= I'/I = I_1/I$) are simply expressed by making I_1 equal I' as $\delta = (S/\ln 10)\ \ln (W/W_1)$, and $\tau = 10^{-\delta/S} = W_1/W$, where $S \cong 100$mV/decade. Therefore, δ required to reduce the leakage by one order of magnitude is small, i.e., 100 mV, implying a good reduction efficiency (i.e., a large leakage reduction with a small δ) of the scheme and, thus, a short recovery time due to a small δ. The SSI scheme is ideal for reducing the leakage current in a memory chip. The memory chip consists of a large number of iterative circuit blocks that dominate the total leakage of the chip. In addition, only one circuit of each block is selected during active periods. For example, for an n-inverter block, shown in **Fig.5(a)**, if leakage current i flows through each p-MOST with channel width w during standby periods, the total current of the block is given by ni. In contrast, for the SSI scheme, shown in **Fig.5(b)**, the reduction ratio becomes $I'/I = W_1/nw$, since the block can be regarded as one p-MOST (corresponding to Q in **Fig.4**) with a channel width of nw. Note that only one inverter is selected, so $W_1 \cong w$ without sacrificing much speed. Consequently, the reduction effect becomes greater as n increases. If the block is divided into many sub-blocks, and SSI is applied to each sub-block, the leakage current in the active mode is also lowered[5-8].

Taking on an ambitious yet concrete challenge is the key to creating outstanding inventions. A good example is the world's first exploratory 1.5-V 64-Mbit DRAM that we started to develop as early as 1988. Both 1.5-V operation (i.e., single-battery operation) and 64-Mbit capacity were ambitious because a 5-V power supply was standard and the 16-Mbit generation was still under research and development at that time. In addition to such an ambitious target, the detailed design of a full 64-Mbit chip enabled us to uncover the above-described leakage problem. From then up till 1993, we had applied for almost all the circuit patents that we take for granted today. It turned out that with our work on leakage-current reduction for active mode, we were ahead of logic-LSI designers by about eight years.

Figure-4: Concept of switched-source-impedance (SSI) scheme

(a) without SSI (b) with SSI

Note on abbreviations:
SSI (switched-source impedance)

Figure 5: Application of SSI to an iterative circuit block

(a) without SSI (b) with SSI

Future prospects

Developments of micro-fabrication process, devices, and circuitry are becoming increasingly difficult as devices and operating voltages are scaled down[1-8]. In the following, future prospects from the viewpoint of circuit design are given in terms of the signal charge of DRAM cells, leakage currents, and speed variations.

We have to maintain the signal charge in order to operate DRAM cells stably even at low voltages. Thus, for low-cost and general-purpose DRAMs, as in the past, improvements of vertical capacitor structures combined with high-dielectric-constant capacitor films will be indispensable. In addition, to make the fabrication process of the capacitor easier, a relatively high operating voltage will be needed. For embedded (e-) DRAMs used in logic LSIs, which give first priority to high-speed and low-voltage operation, the candidates are not only simple 1-T cells, but also simple gain cells, such as three-transistor cells for stable operation even at low voltage[8]. Such e-DRAMs will threaten the existing six-transistor SRAM (static random access memory) cell with a smaller area and lower-voltage-operation capability. Note that SRAM cells will suffer from a narrow voltage margin at sub-1 V as well as a larger cell area[8] (see **Fig. 1**). If the current pace of

38 2008 Special Edition

device miniaturization and voltage reduction continues, however, the signal charge will deteriorate to an unacceptably low level at some point in the future. The pace of voltage reduction will thus slacken, accompanied by developments of stress-voltage-immune MOSTs. In the long run, new memory cells that do not rely on the signal charge will be necessary. Candidates for these memory cells are high-speed, non-volatile RAMs such as phase-change or magnetic RAM.

As for the leakage current of MOSTs, there are two kinds of major leakage: gate tunneling current (not mentioned in this paper) and subthreshold current. To reduce gate-tunneling current, developing a gate-oxide film with a low tunneling current is more effective than developing new circuit techniques. This is because leakage current is not sensitive to gate voltage (which can be controlled by circuit techniques) but is sensitive to gate-oxide thickness. In contrast, circuit techniques are more effective for reducing subthreshold current than device techniques, because leakage current is sensitive to V_T and gate voltage (which can be controlled by circuit techniques), but is insensitive to the MOST structure. The above-described SSI scheme is thus a good solution for this leakage reduction. The variation in inter-die speed, which is caused by chip-to-chip variations of V_T and temperature, can be compensated for with an on-chip substrate-bias (V_{BB}) generator through changing V_{BB} in response to variations of V_T and temperature. The intra-die speed variation, however, cannot be managed with circuit techniques; thus, new MOSTs with low V_T variations, exemplified by a fully-depleted double-gate silicon-on-insulator MOST, are called for.

Conclusion

"It's been tough, but our hard work's been worth it!" That's how I feel about a life of research work spanning 42 years. The reason I feel so is that I have been so lucky in consistently driving cutting-edge technologies with my continuous and deep dedication to influential developments. This luck is owed not only to a rich research environment but also to our many enlightened managers and my research colleagues. Looking back, I realize it was a research life with lots of ups and downs. That is to say, at the dawn of the DRAM era in the early 1970s, and at the young age of thirty, the author was entrusted with developing a 4-Kbit DRAM. From then onwards, after failing four times in the face of global competition, we finally won the race with our 64-Kbit DRAM. At that time, in complete contrast to my thinking up till then that "research is painstaking," I changed my way of thinking to "research is not for the sake of struggle; it gives joy through creation. And only researchers benefit from this joy." After this change in my thinking, I set my challenges higher, and I began to savor the joy of my research. Without question, this "joy of research" exists in our everyday struggles through trial and error in the work place. When a small idea is born in a flash under the utmost stress, and it is successively polished up and incorporated into finished products, one feels a sense of unquestionable joy and fulfillment. Moreover, when such ideas are objectively recognized throughout society, our job satisfaction is maximized. To sum up, starting with a challenge, then by focusing on solutions and putting them into practice, anyone can capture this joy.

Individual Bibliography

(1) Author's estimation based on data from Data Quest
(2) K. Itoh, VLSI memory, Baifukan Co., Ltd. (1994)
(3) K. Itoh: VLSI Memory Chip Design, Springer-Verlag (2001)
(4) K. Itoh, "*Kenkyu Bakka ga Shusse suru*," (R&D Story of A Research Fanatic), Hitachi Intermedia Co., Ltd. (2005)
(5) Y. Nakagome, M. Horiguchi, T. Kawahara, and K. Itoh: Review and Future Prospects of Low-voltage RAM Circuits, IBM J. R&D, Vol. 47, No. 5/6, pp. 525-552 (Sep./Nov. 2003)

Kiyoo Itoh

The Stacked Capacitor DRAM Cell and Three-Dimensional Memory

Mitsumasa Koyanagi, Department of Bioengineering and Robotics, Tohoku University, Japan

koyanagi@sd.mech.tohoku.ac.jp

Device scaling and the DRAM cell

The key component in a computer system is memory, since both data and instructions in a stored-program-type computer are stored in main memory. Magnetic core memories, used in the early stages of computers, were replaced by semiconductor memories early in the 1970's. The first high density semiconductor memory was 1-Kbit dynamic random access memory (DRAM), developed by Intel. Since the advent of this 1-Kbit DRAM, the packing density and capacity of DRAM have continued to increase to today's 4Gbit. Such increases were achieved by the evolution of the memory cell from a four-transistor-type, three-transistor-type to a one-transistor- type. The invention of the one-transistor-type cell (1-T cell) by Robert Dennard especially accelerated the evolution of DRAM in conjunction with his device scaling theory [1, 2].

Scaling limitation of the planar (2D) DRAM cell

The one-transistor-type cell (1-T cell) consists of one transistor and one capacitor. A transistor acts as a switch, and the signal charges are stored in a capacitor. The first 1-T cell was realized using one switching transistor and one MOS capacitor. The number of signal charges stored in the storage capacitor has to be maintained at almost a constant, or can be only slightly reduced, as the memory cell size is scaled down. However, MOS capacitor value -- and hence the amount of signal charges – is significantly reduced as the memory cell size is reduced, even if the capacitor oxide thickness is scaled-down. Therefore, I forecast in 1975 that the 1-T cell with a two-dimensional (2D) structure using a planar MOS capacitor eventually would encounter a scaling-down limitation because we cannot reduce the MOS capacitor area according to scaling theory. In addition, I pointed out that the use of a MOS capacitor in the 1-T cell would be a problem because the signal charges are seriously reduced due to the influence of the minority carriers generated in a silicon substrate. An inversion layer capacitance and a depletion layer capacitance are connected with the gate oxide capacitance in parallel in the MOS capacitor. The charges in the inversion layer and the depletion layer are easily affected by the minority carriers, which are thermally or optically generated or generated by the irradiation of energetic particles in a silicon substrate. Therefore, I predicted that the 1-T cell using an MOS capacitor would encounter a scaling-down limitation due to the influence of the minority carriers as well.

Invention of the three-dimensional (3D) DRAM cell

In my Ph.D. research during 1971-1974 [3], I had commented on the silicon surface and the inversion layer in MOS structures. To evaluate the electrical properties of the interface states and the inversion layer, I myself built an impedance analyzer with the frequency range of 0.01Hz to 100MHz. I examined various kinds of capacitors, including high-k (high dielectric constant) capacitors as a reference capacitor of this impedance analyzer. Eventually, I made a vacuum capacitor for a reference capacitor in which fin-type capacitor electrodes were encapsulated in a vacuum container. From these studies, I learned that an ideal capacitor with low loss should consist of metal electrodes and a low loss insulator (MIM structure); a three-dimensional structure of capacitor electrodes is effective to increase the capacitance value, and there is a trade-off between high-k and loss in the capacitor insulator. In addition, I knew through my Ph.D. research that the charges in the inversion layer and the depletion layer are easily influenced by the minority carriers. Therefore, I questioned why the MOS capacitor with inversion capacitance and the depletion capacitance was used as the storage capacitor in the 1-T cell when I first knew about it in 1975. Then, I tried to eliminate the inversion capacitance and the depletion capacitance by employing a passive capacitor such as the MIM as a storage capacitor and thus proposed a three-dimensional (3D) cell in 1976 [4, 5]. I called this new 3D memory cell a stacked capacitor cell (STC).

Fabrication and evaluation of the three-dimensional stacked capacitor cell

Figure 1 shows the basic structure of a stacked capacitor cell (STC) where the storage capacitor is three-dimensionally stacked on a switching transistor [6, 7]. A passive capacitor with the structure of an electrode-

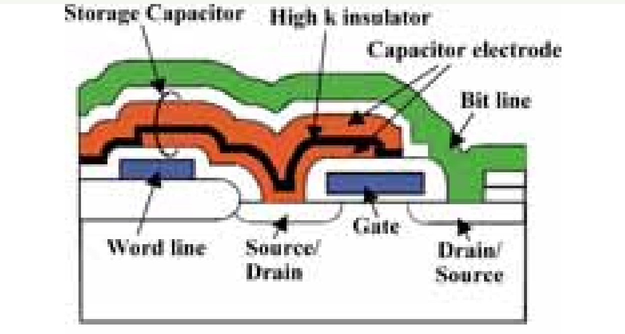


Fig. 1. Basic structure of stacked capacitor cell (STC).

insulator-electrode is used as a storage capacitor. The bottom electrode of the storage capacitor is connected to the source/drain region. I proposed to use self-aligned contacts to connect the bottom electrode of the storage capacitor and a bit line to the source/drain of the switching transistor. This self-aligned technique was also used for the formation of capacitor electrodes. By three-dimensionally stacking the storage capacitor on the switching transistor we can dramatically reduce the memory cell area. In addition, we can use a high-k material as a capacitor insulator to increase the storage capacitance, since a passive capacitor is used as a storage capacitor. This is also useful for reducing memory cell size. Furthermore, we can solve the problem that the signal charges in the inversion layer and depletion layer are influenced by the minority carriers since an inversion capacitance is not used in a stacked capacitor cell. In 1977, I fabricated the first DRAM test chip with a stacked capacitor cell using 3μm NMOS technology and presented a paper on the stacked capacitor cell in 1978 IEDM (IEEE International Electron Devices Meeting) [6]. Figure 2 shows the SEM cross section of a stacked capacitor cell fabricated using 3μm NMOS technology.

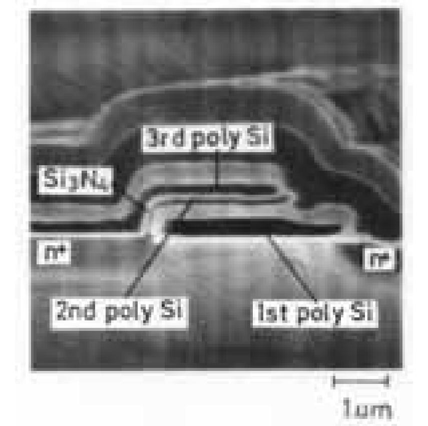


Fig. 2. SEM cross section of a stacked capacitor cell fabricated using 3um nMOS technology.

In this figure it is clearly shown that a storage capacitor is stacked on a switching transistor and a self-aligned contact is successfully formed, although plasma etching and RIE (reactive ion etching) were not available at the time. The self-aligned contact is widely used in today's memory LSI's. In this stacked capacitor cell, I employed polycrystalline silicon (poly-Si)- Si_3N_4 - polycrystalline silicon (poly-Si) as a storage capacitor. Thermal SiO_2 had been used as a capacitor insulator in a conventional 1-T cell with a MOS storage capacitor. In the stacked capacitor cell, I used Si_3N_4 instead of SiO_2 as a capacitor insulator to increase the storage capacitance. The dielectric constant of Si_3N_4 is approximately two times larger than that of SiO_2. I found that the leakage current of Si_3N_4 was significantly reduced by oxidizing its surface, as shown in Fig.3.

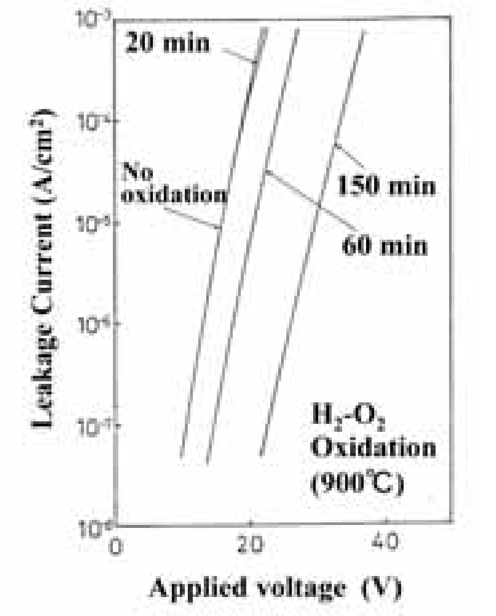


Fig. 3. Leakage-current versus applied-voltage characteristics for Si_3N_4 films with thin oxides on their surfaces.

I also used a Ta_2O_5 film as a capacitor insulator for the first time [7]. Ta_2O_5 has a dielectric constant five or six times larger than that of SiO_2. Therefore, we can greatly increase the storage capacitance, although the leakage current is larger compared to those of SiO_2 and Si_3N_4, as shown in Fig.4.

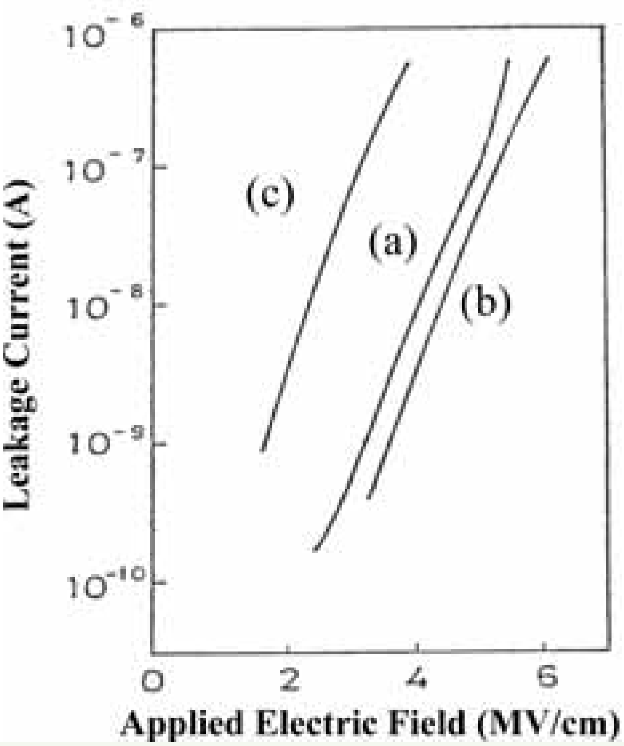


Fig. 4. Leakage current – applied electric field characteristics of storage capacitors. (a) poly-Si–SiO_2–poly-Si, (b) poly-Si–SiO_2 /Si_3N_4 (ON)–poly-Si, (c) poly-Si/Ta–Ta_2O_5–poly-Si.

In 1978, when I presented the first stacked capacitor cell paper in IEDM, it was revealed that the data retention characteristics of DRAM are seriously degraded due to “soft-error,” which is caused by the carriers generated by alpha-particle irradiation in the silicon substrate. At that time, I believed that a stacked capacitor cell is tolerant of soft-error, since the signal charges stored in the passive capacitor are not influenced by the carriers generated in the substrate. Figure 5 shows the dependence of soft-error rate on cycle time in a DRAM test chip [8]. As I expected, the soft-error rate was dramatically reduced by employing a stacked capacitor cell.

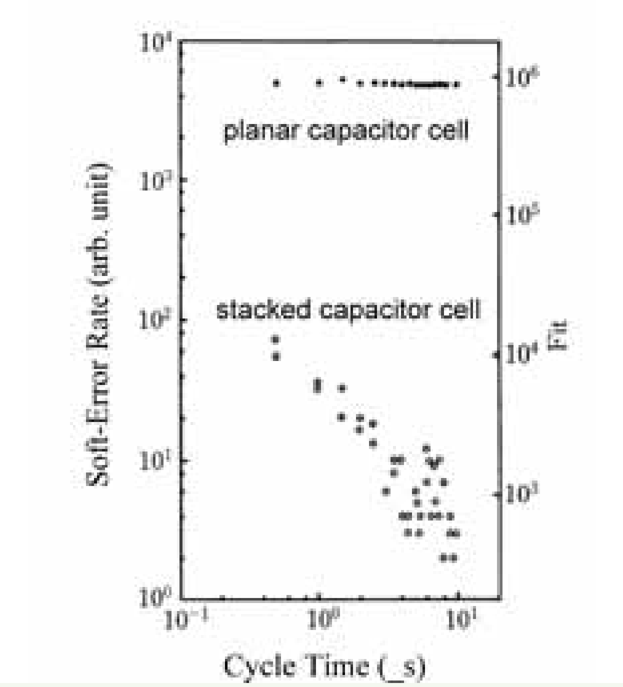


Fig. 5. Dependence of soft-error rate on cycle time in 16 K-bit DRAM test chip.

Eventually I proposed three types of stacked capacitor cells as shown in Fig.6 [9].

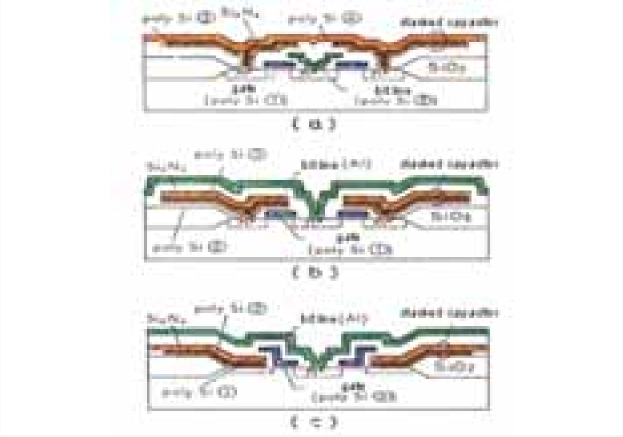


Fig. 6. Cross-sectional configuration of three types of stacked capacitor cells. (a) top-capacitor-type cell, (b) intermediate-capacitor-type cell, (c) bottom-capacitor-type cell.

A storage capacitor is stacked on the switching transistor and the bit line in a top-capacitor-type cell, on the switching transistor in the intermediate-capacitor-type cell (original stacked capacitor cell) and on the isolation oxide (LOCOS) in the bottom-capacitor-type cell. The top-capacitor-type STC cell is another name for the capacitor-over-bit line (COB) stacked capacitor cell and widely used in current DRAM [10]. We can use various kinds of materials for the capacitor insulator and electrodes, and can employ low temperature processes in the formation of the storage capacitor in the COB-type stacked capacitor cell since the storage capacitor is formed on the top of the memory cell.

Evolution of the three-dimensional (3D) memory cell and future memory

In 1979, I fabricated 16K-bit DRAM using a stacked capacitor cell with the oxidized Si_3N_4 (O/N) capacitor insulator [9]. Then I tried to introduce a stacked capacitor cell in 64K-bit DRAM production. However, it was too early to do this due to cost. As a result, the oxidized Si_3N_4 (O/N) capacitor insulator was employed in 64K-bit DRAM production. Since then, the oxidized Si_3N_4 (O/N) capacitor insulator has been widely used for DRAM production. A stacked capacitor cell was employed in a 1Mbit DRAM production for the first time by Fujitsu [11]. Hitachi also employed a stacked capacitor cell in 4Mbit DRAM production [12]. Many other DRAM companies used a trench capacitor cell in the early stage of 4Mbit DRAM production. However, the stacked capacitor cell, which eventually came to occupy a major position in 4Mbit to 4Gbit DRAM’s, has evolved by introducing the three-dimensional capacitor structures with fin-type electrode [13] and cylindrical electrode [14] in conjunction with a capacitor electrode surface morphology of hemi-spherical grain (HSG) [15]. In addition to the introduction of the three-dimensional capacitor structure, a storage capacitor insulator with high dielectric constant (high-k) was employed in high density DRAM’s. In general, the leakage current of high-k material increases by high temperature processing. Therefore, a COB-type stacked capacitor cell is suitable for introducing a high-k capacitor insulator since the storage capacitor can be formed by a lower temperature process. Thus, the Ta_2O_5 capacitor insulator was employed in 64Mbit and 256Mbit DRAM’s with a COB-type stacked capacitor cell. Since then, various kinds of high-k materials have been studied as storage capacitor insulators in high density DRAM’s beyond 1Gbit. The concept of the COB-type stacked capacitor cell -- that various kinds of materials can be stacked on the switching transistor using a lower temperature process -- has been carried on in new memories with a three-dimensional structure such as Fe-RAM (Ferroelectric RAM), P-RAM (Phase Change RAM), R-RAM (Resistive RAM) and M-RAM (Magnetic RAM).

In a high density stacked capacitor DRAM beyond 16 Gbit, a twitching transistor with a three-dimensional structure such as a Fin-FET and a vertical transistor

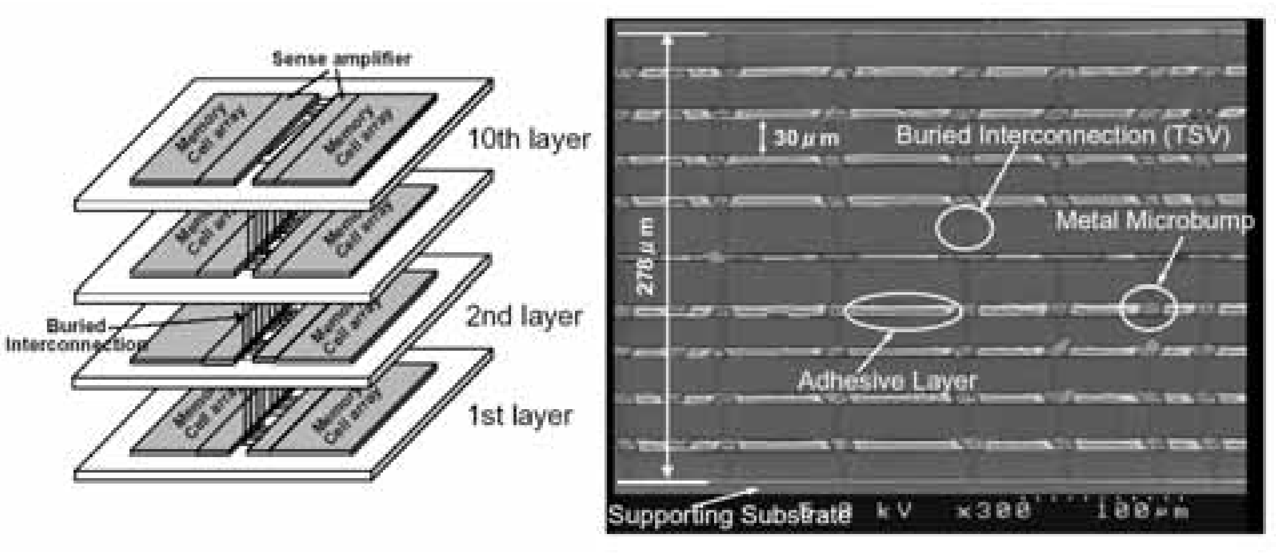


Fig. 7. SEM cross section of 3D-DRAM test chip with ten memory layers fabricated by wafer-on-wafer bonding technology with through-silicon-vias (TSV's).

will be employed together with a cylindrical capacitor and high-k capacitor insulator. Furthermore, many DRAM chips eventually will be vertically stacked to realize 3D-DRAM in which the memory capacity dramatically increases. We have already succeeded in fabricating a 3D-DRAM test chip with ten memory layers as shown in Fig.7 [16, 17].

This 3D-DRAM test chip was fabricated using a newly developed wafer-on-wafer bonding technology with through-silicon-vias (TSV's) [18-20]. Such a 3D-DRAM can be directly stacked on a microprocessor chip to realize a 3D-microprocessor and to solve the problems of memory data-bandwidth between the memory and the processor. We also fabricated a 3D-microprocessor test chip in which a DRAM chip is stacked on a processor chip, as shown in Fig.8 [21].

In the future, various kinds of LSI chips, sensor chips and MEMs chips will be vertically stacked into an ultimate 3D-LSI which we call a super-chip [17, 22]. We have developed a new super-chip integration technology using a novel self-assembly method.

References

[1] R.H. Dennard, USP-3387286, June 4, 1968.

[2] R.H. Dennard, F.H. Gaensslen, H.N. Yu, V.L. Rideout, E. Bassous, and A.R. LeBlanc, "Design of Ion Implanted MOSFET's with Very Small Physical Dimensions", IEEE J. Solid-State Circuits, Vol. SC-9, pp. 256-268, Oct. 1974.

[3] J. Nishizawa, M. Koyanagi and M. Kimura, "Impedance Measurements to Study Semiconductor Surface and Thin Insulating Films on Its Surface", Japanese J. Applied Phys., Suppl. 2, pp.773-779, 1974.

[4] M. Koyanagi and K. Sato, Japanese patent application, Tokugansho 51-78967, 1976.

[5] M. Koyanagi and K. Sato, USP-4151607, Jan. 5, 1977.

[6] M. Koyanagi, H. Sunami, N. Hashimoto and M. Ashikawa, "Novel High Density, Staked Capacitor MOS RAM", IEDM Tech. Dig., pp. 348-351, Dec. 1978.

[7] M. Koyanagi, H. Sunami, N. Hashimoto and M. Ashikawa, "Novel High Density, Staked Capacitor MOS RAM", Extended Abstracts of the 10th Confer-

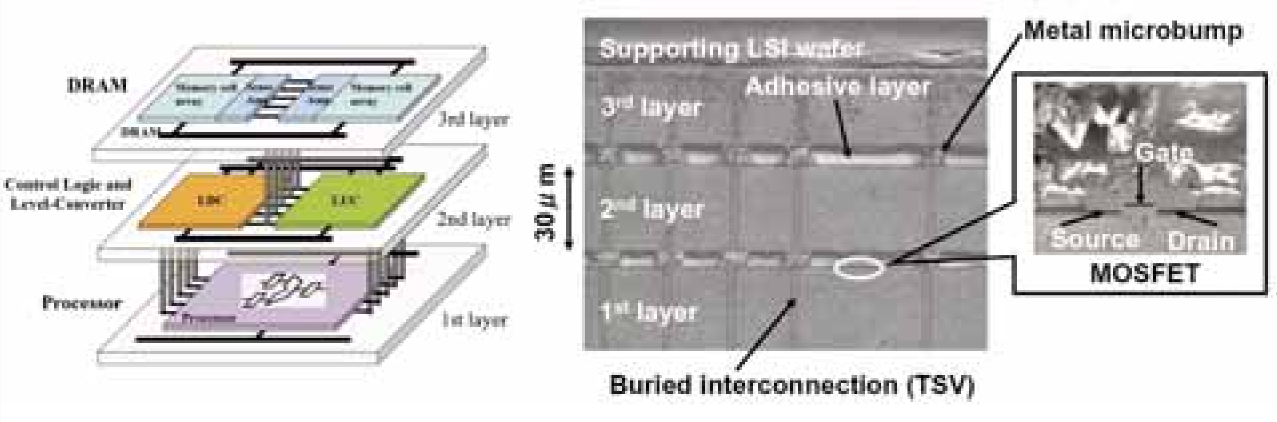


Fig. 8 SEM cross section of a 3D-microprocessor test chip fabricated by wafer-on-wafer bonding technology with through-silicon-vias (TSV's).

ence on Solid State Devices, 1978.

[8] M. Koyanagi, Y. Sakai, M. Ishihara, M. Tazunoki and N. Hashimoto, "16-kbit Stacked Capacitor MOS RAM", IEICE Technical Report (Japanese), SSD80-30, 1980.

[9] M. Koyanagi, Y. Sakai, M. Ishihara, M. Tazunoki and N. Hashimoto, "A 5-V Only 16-kbit Stacked Capacitor MOS RAM", IEEE Trans. on Electron Devices, ED-8, pp.1596-1601, 1980/ IEEE J. Solid-State Circuits, SC-15, pp.661-666, 1980.

[10] S. Kimura, Y. Kawamoto, T. Kure, N. Hasegawa, J. Etoh, M. Aoki, E. Takeda, H. Sunami and K. Itoh, "A New Stacked Capacitor DRAM Cell Characterized by a Storage Capacitor on a Bit-line Structure", IEDM Tech. Dig., pp. 596-599, Dec. 1988.

[11] Y. Takemae, T. Ema, M. Nakano, F. Baba, T. Yabu, K. Miyasaka, K. Shirai, "A 1Mb DRAM with 3-Dimensional Stacked Capacitor Cells", ISSCC Dig. Tech. Papers, pp. 250-251, Feb. 1985.

[12] K. Kimura, K. Shimohigashi, J. Etoh, M. Ishihara, K. Miyazawa, S. Shimizu, Y. Sakai, and K. Yagi, "A 65-ns 4-Mbit CMOS DRAM with a Twisted Driveline Sense Amplifier", IEEE J. Solid-State Circuits, SC-22, pp.651-656, 1987.

[13] T. Ema, S. Kawanago, T. Nishi, S. Yoshida, H. Nishide, T. Yabu, Y. Kodama, T. Nakano, M. Taguchi, "3-Dimensional Stacked Capacitor Cell for 16M and 64M DRAMs", IEDM Tech. Dig., pp. 592-595, Dec. 1988.

[14] W. Wakamiya, Y. Tanaka, H. Kimura, H. Miyatake and S. Satoh, "Novel Stacked Capacitor Cell for 64Mb DRAM", Symposium on VLSI Technology Dig. Tech. Papers, pp. 69-70, 1989.

[15] H. Watanabe, T. Tatsumi, S. Ohnishi, T. Hamada, I. Honma, T. Kikkawa, "A New Cylindrical Capacitor Using Hemispherical Grained Si (HSG-Si) for 256Mb DRAMs," IEDM Tech. Dig., pp. 259 - 262, Dec. 1992.

[16] K.W. Lee, T. Nakamura, T. Ono, Y. Yamada, T. Mizukusa, H. Hashimoto, K.T. Park, H. Kurino and M. Koyanagi, "Three-Dimensional Shared Memory Fabricated Using Wafer Stacking Technology", IEDM Tech. Dig., pp. 165-168, Dec. 2000.

[17] T. Fukushima, Y. Yamada, H. Kikuchi, and M. Koyanagi, "New Three-Dimensional Integration Technology Using Self-Assembly Technique", IEDM Tech. Dig., pp. 359-362, Dec. 2005.

[18] M. Koyanagi, "Roadblocks in Achieving Three-Dimensional LSI", 8th Symposium on Future Electron Devices Tech. Dig., pp.55-60, 1989.

[19] H. Takata, T. Nakano, S. Yokoyama, S. Horiuchi, H. Itani, H. Tsukamoto and M. Koyanagi, "A novel fabrication technology for optically interconnected three-dimensional LSI by wafer aligning and bonding technique," Proc. Int. Semiconductor Device Research Symposium, pp.327-330, 1991.

[20] M. Koyanagi, T. Nakamura, Y. Yamada, H. Kikuchi, T. Fukushima, T. Tanaka, and H. Kurino, "Three-Dimensional Integration Technology Based on Wafer Bonding With Vertical Buried Interconnections", IEEE Trans. on Electron Devices, vol.53, pp. 2799-2808, 2006.

[21] T. Ono, T. Mizukusa, T. Nakamura, Y. Yamada, Y. Igarashi, T. Morooka, H. Kurino and M. Koyanagi, "Three-Dimensional Processor System Fabricated by Wafer Stacking Technology", IEEE COOL Chips V Tech. Dig., pp.186-193, 2002.

[22] T. Fukushima, Y. Yamada, H. Kikuchi, T. Konno, J. Liang, K. Sasaki, K. Inamura, T. Tanaka, and M. Koyanagi, "New Three-Dimensional Integration Technology Based on Reconfigured Wafer-on-Wafer Bonding Technique", IEDM Tech. Dig., pp. 985-988, Dec. 2007.

About the Author

Mitsumasa Koyanagi was born in 1947 in Hokkaido, Japan. He received the B.S. degree from Department of Electrical Engineering, Muroran Institute of Technology, Japan in 1969 and the M.S. and Ph.D. degrees from Department of Electronic Engineering, Tohoku University in 1971 and 1974, respectively.

He joined the Central Research Laboratory, Hitachi Co. Ltd. in 1974 where he had engaged in the research and development of DRAM and ASIC process and device technologies and invented a Stacked Capacitor DRAM memory cell which has been widely used in DRAM production. In 1985, he joined Xerox Palo Alto Research Center, where he was responsible for research on submicron CMOS devices, poly-Si TFT devices and analog/digital sensor LSI design. In 1988, he became a professor in the Research Center for Integrated Systems, Hiroshima University, Japan where he engaged in the research of sub-0.1um device fabrication and characterization, device modeling, poly-Si TFT devices, 3-D integration technology, optical interconnection and parallel computer system. He proposed a 3-D integration technology based on wafer-to-wafer bonding and through-Si vias (TSVs) in 1989. Since 1994, he has been a professor in the Intelligent System Design Lab., Department of Machine Intelligence and Systems Engineering, and is currently a member of the Department of Bioengineering and Robotics, Graduate School of Engineering, Tohoku University, Japan. His current interests are 3-D integration technology, optical interconnection, nano-CMOS devices, memory devices, parallel computer system specific for scientific computation, real-time image processing system, artificial retina chip and retinal prosthesis chip, brain-machine interface (BMI) and neural prosthesis chip, brain-like computer system.

Dr. Koyanagi was awarded the IEEE Jun-Ichi Nishizawa Medal (2006), the IEEE Cledo Brunetti Award (1996) and Japan's Ministry of Education, Culture, Sports, Science and Technology Award (2002), in addition to the Ohkouchi Prize (1992), SSDM (Solid-State Devices and Materials Conf.) Award (1994) and the Opto-Electronic Integration Technology (Izuo Hayashi) Award in 2004. He is an IEEE fellow.

The Role of the Trench Capacitor in DRAM Innovation

Hideo Sunami, Research Center for Nanodevices and Systems, Hiroshima University, sunami@sxsys.hiroshima-u.ac.jp

Advent of DRAM

The advent of dynamic-random-access memory (DRAM) is recognized to have been in 1970, when Intel introduced a 1-Kbit chip using three-transistor DRAM cells. A few years later, 4-Kbit DRAM using the one-transistor cell[1] was being widely manufactured, its low cost contributing to the development of the personal computer. This was just the time when metal-oxide-semiconductor (MOS) devices were proven to deserve application as highly reliable main memory in mainframes.

Since then, DRAM capacity has been increasing by a factor of four every three years until today. As modern computers are based on von Neumann's architecture, main memory is a key device together with processor. Along with the prosperity of computing, the demand for memory has increased to produce a world-wide 30-B$ market for DRAM. Even if the main customer is still personal computers, various applications such as cell phones, game machines, personal audio, and video machines are extending DRAM's usage.

Key factor of cost

The strongest driving force for growing the DRAM market is undoubtedly "cost." Therefore, various development efforts have focused on the reduction of manufacturing cost. The bit cost has decreased by a factor of 10^6 since 1970, and the 1-Gbit product will soon be sold at the same price as 1-Kbit. Since die cost is closely related to number of dies on a wafer, wafer size has continually increased to be such as 2", 3", 4", 5", 6", 8", and now 12" in diameter. Together with the diameter increase, memory cell size has been reduced to be one-third for each DRAM generation in volume production to absorb die size increase. Consequently, the die size has been enlarged at most up to 10 times despite a bit increase by 10^6 from 1-Kbit to 1-Gbit, while the memory cell size decreasesd by 10^5 times as shown in Fig. 1.

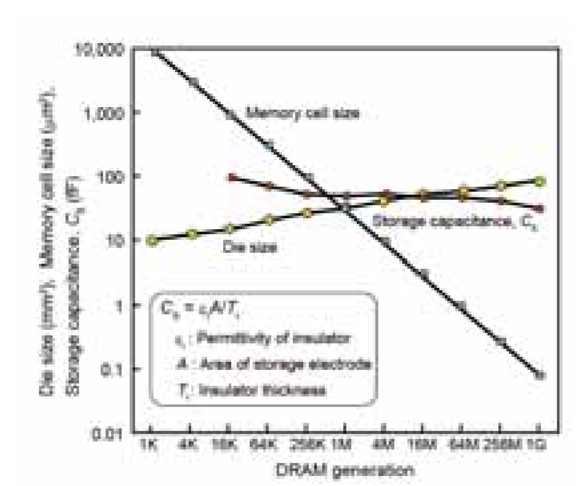


Fig. 1 Memory cell size shrinkage at DRAM in volume production.

One of the key processes to achieve cell size reduction is patterning technology, including photolithography and dry etching. Pattern size has been reduced to 1/100 from 10 μm to 100 nm since 1970. For a long time until the late 1990's, DRAM was a unique vehicle to develop finer patterning technologies. As far as isolated patterns such as transistor gate length are concerned, high-end microprocessors incorporate smaller dimensions than DRAM. But half-pitch of dense wiring still denotes difficulty of overall patterning technologies. Transistor density of DRAM is more than 10 times larger than that of microprocessor.

Invention of the trench cell

In response to die size reduction to cope with a 4-fold increase in memory capacity, memory cell size has been reduced by almost one-third for each generation, previously shown in Fig. 1. The so-called 1-transistor DRAM cell[1] consists of one cell transistor and one storage capacitor. Key specifications in DRAM operation, such as noise margin, soft-error durability, operational speed, and power consumption, strongly depend on the storage capacitor[2]. The capacitance value, C_S is expressed as $C_S=\epsilon_i A/T_i$, where ϵ_i, A, T_i, are permittivity of storage insulator, area of capacitor electrode, and insulator thickness, respectively. Therefore, cell size reduction through scaling alone leads to area reduction and a subsequent decrease in capacitance value.

To cope with the dilemma of size vs. capacitance, insulator thickness was reduced by a factor of 10 from 100 nm in 1-Kbit chips to 10 nm in 1-Mbit chips, getting dangerously close to dielectric field breakdown. When the author took a glimpse at some conference presentations in 1974 from Texas Instruments introducing a highly efficient silicon solar cell with a steep trench and forecasting the upcoming issue of cell size vs. capacitance, he got an idea of a trench capacitor DRAM cell. Even though his job at that time was to characterize the silicon surface with photoemission spectroscopy, his amateur-radio hobby connected the shape of a trimmer condenser, which has two coaxial cylindrical opposite electrodes as seen in Fig. 2, with the needs of a 1-transistor cell. From that idea, he invented the trench capacitor cell and applied for a Japanese patent[3] in 1975. Due to its low score of assessment, this was not applied to any overseas patent.

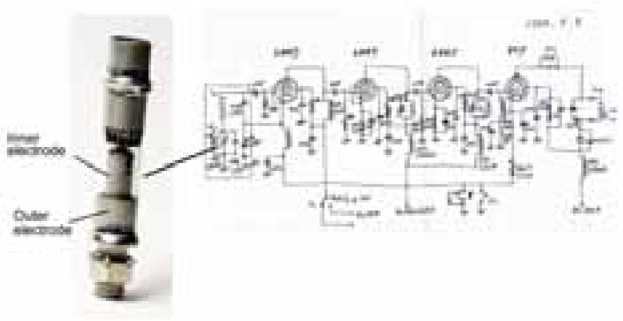


Fig. 2 An amateur-radio transmitter circuit designed by the author in 1960 and a photograph of a trimmer condenser.

After Hitachi had won a leader's position in 64-Kbit products with a 5-V single power supply and folded bit-line arrangement[4], it's research and development group could afford to challenge for novel cell development. After several years' development, the first 1-Mbit level trench cell in trial production was implemented and presented in 1982 IEDM[5]. Its journal paper won the 1984 Paul Rappaport Award[6]. An SEM cell cross-section is shown in Fig. 3.

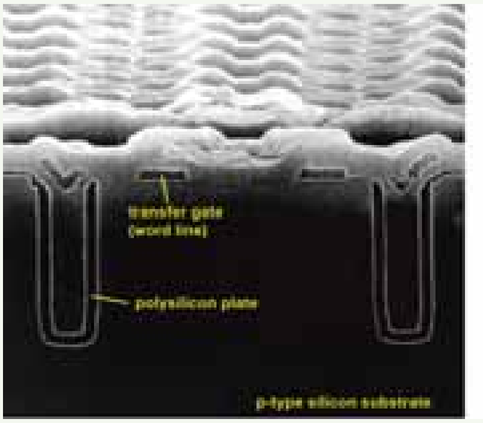


Fig. 3 First 1-Mbit DRAM with trench capacitor cell.

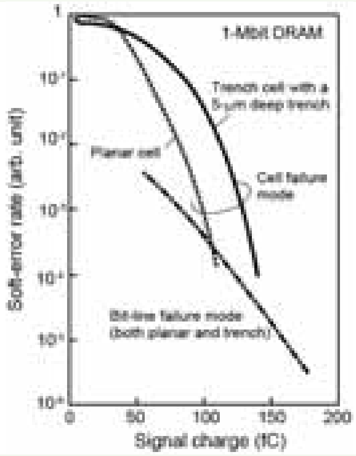


Fig. 4 Soft error rates of planar and trench cells.

Changes of trench cell employment

In the first trench cell in trial production, a serious problem of soft-error was found caused by alpha-particle hit as shown in Fig. 4.

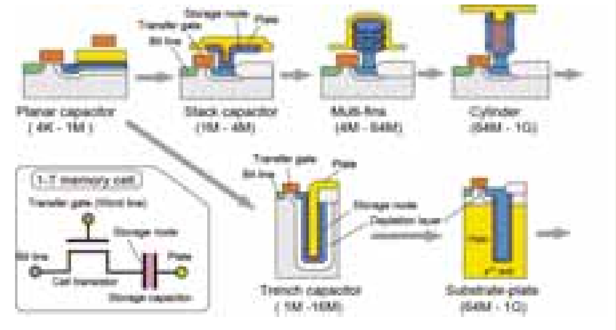


Fig. 5 Major advancement in DRAM cell innovation.

One alpha particle at maximum 5-MeV energy generates almost one million electron-hole pairs. One million electrons is about 190 fC, which is almost equivalent to signal charges stored in one storage capacitor of a 1-Mbit DRAM cell. Due to extended depletion layer of the storage capacitor in the trench cell, it "effectively" collects generated electrons. In addition to the soft-error problem, it was predicted that punch-through current between any two adjacent capacitors would soon limit further shrinkage of the cell. Whether the trench cell should be improved or abandoned was a serious decision point.

In those days, most DRAM manufacturers made efforts to supply their DRAM products to very limited leading mainframe makers. That was a kind of certificate that their products achieved first-rate reliability. The certificate surely made their business fruitful. Even with a half-year delay in product development, they might lose their business in the mainframe market. There is some evidence that the leading maker has changed with each DRAM generation, from 1-K, Intel, TI, MOSTEK, Hitachi, NEC, Toshiba, NEC, and Samsung.

Being both a DRAM manufacturer and main frame maker, Hitachi focused keenly on the mainframe application with highest-grade reliability. Thus, Hitachi had abandoned the trench cell, despite device development group proposals for several improved structures to reduce the soft-error problem. Additional development was thought to need more than half a year. An invention of half-V_{cc} plate configuration which had a potential of storage-capacitance doubling could prolong the conventional planar cell. This might also have influenced Hitachi's decision.

However, several major manufacturers employed the trench and have been improving the structure until today. Major advancement in cell innovation is shown in Fig. 5.

Together with the trench, the stacked capacitor cell was also applied in products. The substrate-plate trench cell amazingly improves soft-error tolerance due to its highly shrunk depletion layer. In addition to these cell structure innovations, the hemi-spherical grain (HSG) structure[7] was an inevitable technique to double the storage capacitance due to increased surface area. Cylinder-type stack and substrate-plate trench, both with HSG, are the major cells being produced today.

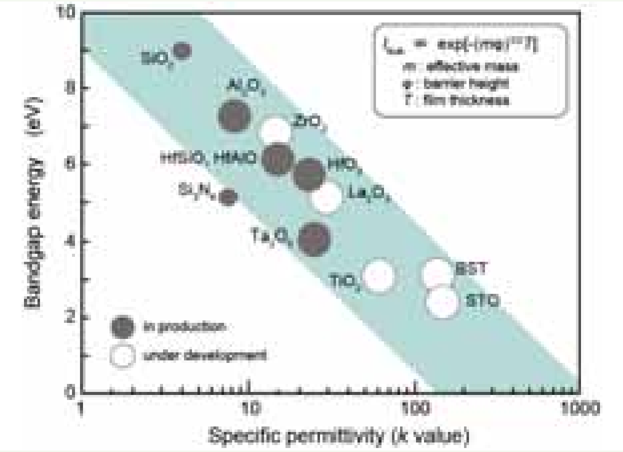


Fig.6 Relation between bandgap energy and permittivity of high-*k* insulating films.

Material revolution

From 1 K to 1 M, shrinking dimensions was the key issue. The storage capacitance value was kept almost the same over several DRAM generations by reducing insulator thickness. Consequently, the reduced thickness made the electric field across the insulator close to 5 MV/cm, a value which was recognized to be an upper limit for keeping insulator integrity and refresh time in DRAM operation. Thus, innovative technique other than thickness reduction was strongly required.

In response, three-dimensional structures were proposed. From 1 M to 1 G, three-dimensional structure innovation has been achieved as previously shown in Fig. 4. However, as the aspect ratio of the storage capacitor exceeds more than 10, manufacturability will be a much more serious issue. The final parameter to be handled in the relation of $C_S=\epsilon_i A/T_i$ is permittivity, ϵ_i. Thus, various kinds of high-*k* materials have been developed as shown in Fig. 6. But there is a serious fact that the thinner the thickness is, the less its permittivity is. There may not be a unique ultimate solution at this moment. Material revolution with ultra high-*k* material is solicited to extend DRAM further toward terabit DRAM.

To summarize innovation achieved in the past and requirements for the future, there are three eras for DRAM development:

- 1-K to 1-M ---- dimension improvement (smaller cell, reduced insulator thickness)
- 1-M to 1-G ---- structure innovation (stack and/or trench cells)
- 1-G to 1-T ---- material revolution (ultra high-*k* films)

The final parameter which affects advanced shrinkage of the cell should be the insulator thickness itself. If the insulator is thick enough to fill the internal hole of the trench of the trench cell or the cylinder of the stacked cell, the plate of the capacitor cannot penetrate inside the trench or the cylinder, resulting in no capacitor formation[8]. In this sense, high-*k* films should be thin enough, simultaneously keeping their high-*k* value. This may be the deadlock for realizing smaller cells of the 1-T type DRAM cell. Even utilizing cutting-edge high-*k* films at present, 32 or 64-Gbit DRAM will be the biggest capacity without die stack. We would like to expect novel main memory candidates in the near future.

References

1) R. H. Dennard, U. S. Patent 3,387,286, 1968.
2) R. H. Dennard, “Evolution of the MOSFET Dynamic RAM-A Personal View,” IEEE Trans. Electron Devices, ED-31, pp. 1549-1555, 1984.
3) H. Sunami and S. Nishimatsu, Japanese patent application, Tokugansho 50-53883, 1975.
4) K. Itoh, R. Hori, H. Masuda, Y. Kamigaki, H. Kawamoto, and H. Katto, “A single 5V 64K dynamic RAM,” ISSCC Dig. Tech. Papers, pp. 228-229, Feb. 1980.
5) H. Sunami, T. Kure, N. Hashimoto, K. Itoh, T. Toyabe, and S. Asai, IEDM Tech. Dig., pp. 806-808, December, 1982.
6) H. Sunami, T. Kure, N. Hashimoto, K. Itoh, T. Toyabe, and S. Asai, “A Corrugated Capacitor Cell (CCC),” IEEE Trans. Electron Devices, ED-31, No. 6, pp. 746-753, 1984.
7) H. Watanabe, T. Tatsumi, S. Ohnishi, T. Hamada, I. Honma, and T. Kikkawa, “A new cylindrical capacitor using hemispherical grained Si (HSG-Si) for 256Mb DRAMs,” IEDM Tech. Dig., pp. 259 - 262, December 1992.
8) K. Itoh, H. Sunami, K. Nakazato, and M. Horiguchi, “Pathways to DRAM Design and Technology for the 21st Century,” Proc. the 8th Internat. Symp. Silicon Materials Science and Technology, Volume 98-1, pp. 350-369, 1998.

About the Author

Hideo Sunami (Fellow, IEEE) received the B.S., the M. S., and the Ph. D. Degrees in Electrical Engineering all from Tohoku University, Japan, in 1967, 1969, and 1980, respectively. He is currently a Professor with Special Appointment in Interdisciplinary Research on Integration of Semiconductor and Biotechnology, Hiroshima University and a Technical Advisor to Consortium for Advanced Semiconductor Materials and Related Technologies.

From 1998 to 2007, he was a Professor at Research Center for Nanodevices and Systems in Hiroshima University working on three-dimensional MOS devices and silicon optical modulator. From 1969 to 1998, he has been doing R&D on multi-level metallization, CCD, DRAM, three-dimensional devices, and process CAD, mainly in Central Research Laboratory, Hitachi Ltd.

He has published 113 papers both in technical journals and international conferences and authored and coauthored 16 books. He has held 115 Japanese and US patents. He was awarded the 1985 Paul Rappaport Award, the 1991 Cledo Brunetti Award, the 1998 Tokyo Governor’s Distinguished Inventor Award, and the 2006 Jun-ichi Nishizawa Medal. He is a Fellow of Japan Society of Applied Physics and a Fellow of the Institute of Electronics, Information and Communication Engineers of Japan.

The Remarkable Story of The DRAM Industry

Randy Isaac, Executive Director, American Scientific Affiliation, Randy@asa3.org

INTRODUCTION

Computing systems depend on the ability to move vast amounts of data to and from the processor itself. Early in the development of computers, it was recognized that a hierarchy of memory was essential to enable timely access to data.

Most computing systems have three basic categories of memory: On-chip memory is the fastest and most expensive, dedicated to the immediate needs of the processor. Main memory stores the software and data for quick access when needed. It is often hundreds of times larger in capacity than on-chip memory and about a tenth to a hundredth the speed. “Storage” is the term used for non-volatile memory, including hard-disc drives, solid-state flash devices, and/or magnetic tape for vast amounts of data when fast access times are less important.

Dynamic Random Access Memory (DRAM) technology has had a virtual monopoly on the main memory segment. Its relatively low cost and high access speed are well-suited for computing system needs. The origin of DRAM technology and the invention of the one-transistor DRAM cell are addressed in other articles in this issue. This article looks at the overall DRAM industry since its beginnings in 1970 and examines some of the key factors that determined its success.

Figure 1 shows a graph of the number of DRAM bits shipped per year since the first DRAM chips were sold by Intel in mid-1970. In every year, the number of bits shipped has been greater than the previous year; there has been no downturn in volume: The annual growth rate in shipped volume of bits was an incredible 150% in the first 15 years of the industry, an impressive 70% in the next 15 years and a still respectable 50% since then.

DRAM products are typically identified by the number of bits per chip, sometimes called its “granularity.” The first products had 1,024 bits of storage and were dubbed 1K DRAM’s. Subsequent products increased the amount of storage by a factor of 4.

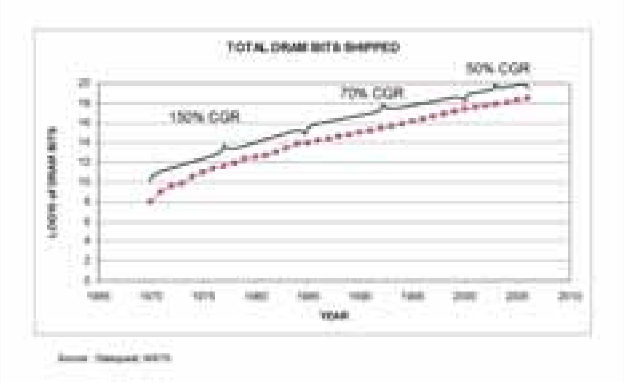


Figure 1: Volume of DRAM bits shipped per year.

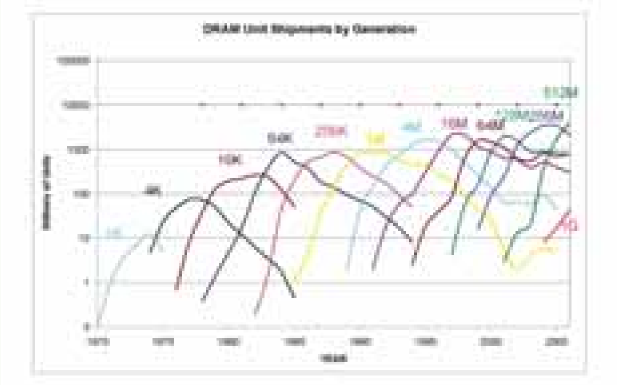


Figure 2: Volume of DRAM bits shipped per year by chip granularity.

Figure 2 shows the volume of units shipped for all granularities of DRAMs since 1970. The 4X increase in bits per chip per product generation was sustained in the industry until the introduction of the 128Mb product, after which a 2X increment became the rule.

MOORE’S UBIQUITOUS LAW

In 1975, Gordon Moore reported that his prediction[1] in 1965 of an annual doubling of transistors per die was remarkably accurate.[2] He also claimed the doubling rate would slow down to something less than two years. The relatively new DRAM industry, led by Moore’s own company, latched onto his scenario and followed it more closely than any other product line. DRAM products were subsequently developed at a pace of a 4X increase in bits per chip every three years, a trend dubbed “Moore’s Law.” Figure 3 shows the total number of bits shipped divided by the total number of chips shipped, yielding an effective average bit per chip. In recent years the trend has clearly slowed down.

Another analysis considers the first year of manufacturing for a given granularity. Figure 4 shows that while DRAM introduction maintained the 4X/3yr pace until the latter part of the 90’s, the rate has slowed

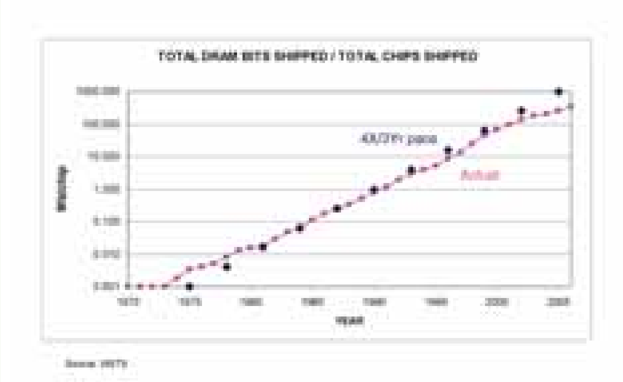


Figure 3: Average DRAM bits per chip shipped per year.

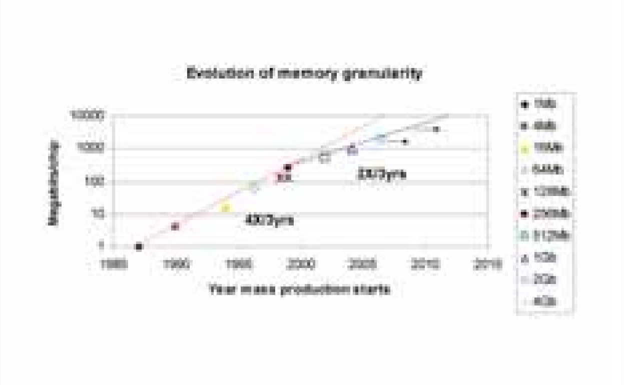


Figure 4: Trend of introduction of DRAM chips into manufacturing.

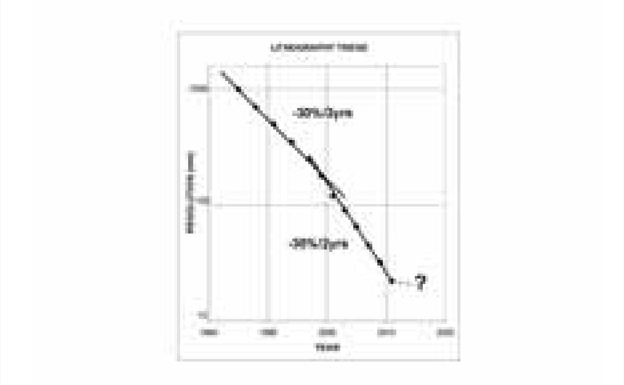


Figure 5: Trend of lithography resolution for chip manufacturing.

considerably since then to approximately 2X/3yr. Projecting from the trend of the 80's and 90's, a 16Gb DRAM chip would have been expected to be manufactured in 2007. Instead, it is a 2Gb chip that is making its debut.

The importance of Moore's Law is not so much the doubling rate, which has varied from the beginning. Rather, Moore's keen insight was the root cause of an increase in transistors on a die and its economic effects. In his 1975 article, Moore identified three major factors that enabled such a rapid increase in transistors per chip: Improvements in manufacturability leading to larger die sizes; innovation in cell layout for more efficiency; and higher resolution lithography for increased density. He attempted to quantify the relative contributions of each factor. The DRAM industry settled into a slightly different balance of contributions with 50% due to lithography, 25% due to an increase in die size manufacturability, and 25% due to innovative reductions in cell size per bit. This fundamental recipe guided the industry for several decades. To discover the reasons for the recent shift in the trend line, we need to look at these underlying factors in more detail.

The near-mythic popularity of Moore's Law was a boon to the development of the DRAM industry. The underlying principles were fundamentally sound and resonated with the technology community. The trend lines were clear targets for all suppliers, customers, and developers. Infrastructure needs could be identified well in advance so that equipment suppliers were able to develop the necessary equipment in time. Innovative ideas were stimulated by the challenge of sustaining the rapid pace of exponential improvement.

Lithography was the dominant factor in improving bits per chip. The recipe cited above is equivalent to a 30% improvement in linear resolution for each 3-year cycle. That pattern was sustained as technology migrated from broadband mercury illumination to g-line, h-line, i-line, and then DUV excimer laser technologies at 248nm and now 193nm capabilities. Remarkably, the pace seems to have accelerated since the late 90's with the introduction of DUV, when the pace increased to 30% every 2 years, as shown in Fig. 5. It is possible that this rate of progress will continue to the 22nm generation using 193nm lithography. No economically feasible technology has yet been identified beyond that level.

The more rapid increase in lithography progress would normally have been expected to increase the pace of progress of DRAM granularity. However, the improvement in bits per chip of DRAM products actually slowed down at the same time that lithography speeded up. To understand this contrasting trend, we need to understand the other two driving forces in DRAM density.

DRAM cell innovation was a creative aspect of product development. Dennard's invention of the one-transistor cell[3] stimulated a critical improvement in areal bit density. Subsequently, each product reflected a more efficient layout of the key elements defining the transistor, the capacitor, and the necessary contacts.

A major split in the DRAM industry occurred with the 4Mb products. To achieve the improvement mandated by the recipe, the cell needed to become 3-dimensional. The two obvious choices were placing the capacitor above the transistor vs. placing the capacitor below the transistor. The industry split into a stacked capacitor path vs. a trench capacitor approach. A key innovation at IBM was the substrate plate trench capacitor in which the charge was stored inside the trench capacitor with the substrate grounded, as opposed to other approaches where the charge was stored outside the trench. The latter approach was not able to scale to smaller dimensions as the trenches came closer together and the charge from neighboring cells began to merge. This innovative cell became the only successful trench approach and was widely deployed via IBM's alliance with Siemens and Toshiba. The rest of the industry placed the capacitor on top of the transistor. To this day, both approaches persist in the industry with neither ceding ground to the other in extensibility.

However, in the last half of the 1990's, both approaches reached a limit in area of approximately 6-8F^2 where F is the smallest lithographic feature size. A simple cross-point cell has a minimum area of 4F^2. An area of 6F^2 is felt to be the approximate limit of memory cells without going to multiple bit-per-cell technologies which trade off access speed. As a result, cell size innovation became a much smaller factor in the improvement of bit density at about the same time that lithography moved faster.

Die size is perhaps the most difficult parameter to track. Silicon area is the single most important factor in manufacturing cost. As soon as a product is introduced, competitive survival requires a rapid reduction in die size. A rough indicator is to consider the die size of the first volume shipments of a particular product line. This die size increased according to the recipe until approximately the 64Mb generation. By that time, the DRAM market was dominated by the PC industry. Memory was being sold primarily through memory modules rather than as individual packaged die. The most rapidly growing portion of that market was laptops, which constrained the physical size of these modules. As module size became standardized, larger modules were not accepted in the marketplace. This limitation meant that new DRAM product introductions needed to meet the module size constraints. Hence, an increase in die size was no longer a viable option for increasing DRAM granularity at about the same time that lithography moved faster.

Cost reduction played a major role in reducing die size. DRAM prices have historically dropped approximately 27% a year, though with significant fluctuations due to supply and demand variation. Accordingly, the manufacturers must drop costs by at least 27% a year. The most important parameter for cost is die size which determines the number of die per wafer. Competitive pressures led to a rapid reduction of die size to approximately the same size, independent of granularity. Consequently, die size could no longer contribute significantly to an increase in bits per chip.

Of the three technical factors identified by Moore, only lithography remained a major factor in improving the number of DRAM bits per chip by the end of the 20th century. The faster rate of introduction of lithographic resolution in the late 90's was more than offset by the lack of increase in die size and the stable normalized cell sizes. The migration of the DRAM industry from a 4X/3 year pace to a 2X/3 year pace can be understood from these technology considerations.

THE ECONOMICS OF DRAM's

Market demand must also be noted as an important factor in the changing pace of DRAM products. In the late 80's and most of the 90's, the PC was the dominant market for DRAM's. Approximately 75% of DRAM's were sold to PC clients or servers. For most of that period, memory upgrades were a critical way to improve PC performance and to enable the use of new applications. By the end of the 90's, however, the sizes of operating systems and of applications were no longer growing as rapidly. The amount of main memory per PC was not required to increase as quickly as it did in earlier years. Consequently, the dominant market for DRAM's did not demand as fast an increase in bits per chip.

The high-performance computing industry had no such letdown in demand. Its insatiable appetite for performance demanded more memory with very high bandwidth. However, as a DRAM customer, its volumes were a small fraction of those represented by PC's – not a large enough market to drive the development of more bits per chip. Since attention must be directed to more efficient packaging to reduce the physical size of a large main memory, innovative ways of stacking DRAM die with through vias are being pursued to reduce overall costs.

So far, our discussion has focused on the physical size of DRAM chips. A few words about performance, namely write time, access time and power are in order. The physical reduction of memory cell size does not automatically lead to better performance. Only a well-designed balance of improved transistor characteristics and matching capacitor capabilities can enable proper scaling with performance benefits. The DRAM industry as a whole has always valued cost more than performance. As a system house, IBM was a DRAM manufacturer with a captive market for many years. It had the luxury of optimizing its main memory design to enhance system performance. As a result, IBM's first 1Mb offering continued to use metal gate technology and an NMOS technology. Reliability and power considerations drove the migration to CMOS with polysilicon gates. Only in its 16Mb and 64Mb DRAM products, developed in an alliance with Siemens, now Qimonda, and Toshiba did IBM move to industry-standard products for cost reasons. Proposals for high-speed DRAM's dotted the DRAM literature, but the market simply did not bear any additional cost per bit.

Power consumption has always been of some concern due to the large number of DRAM chips normally used in a system, especially in high-performance systems. As channel lengths have decreased and standby power increased, these concerns have grown. Future development will need to concentrate more on ways to reduce leakage and power required to write and access bits. The ability to fully leverage improvements in lithography will depend on innovative ways to scale the transistor and capacitor while decreasing leakage such as pass gate devices with 3D structures.

The business and economic aspects of the DRAM industry are every bit as influential as the technology elements. As the DRAM product grew in demand, many companies jumped at the opportunity to participate. In the late 80's there were as many as 30 companies worldwide that were producing DRAM memory chips. But the torrid pace of increasing bits/chip with its demands of competitive technology took its toll. The cost of technology development was estimated at half a billion dollars by the early part of the 90's, with a comparable or larger capital investment for a manufacturing facility. Today the development costs exceed a billion dollars and a fab investment is in the ballpark of 2 to 3 billion dollars. Such a vast investment of money and time with high risk chased most players out of the business. In the 90's, the industry moved to alliances. IBM worked with Siemens and then with Toshiba to share development expertise and costs. That highly successful model migrated to a broad logic technology development that still leads the industry. At the beginning of the 21st century there were only eight significant players remaining in the DRAM business.

Any business built around a core concept of rapid reduction in unit cost must realize a market growing faster than the price reduction if the industry revenue is expected to increase. As seen in Fig. 1, the DRAM bit volume market increased very rapidly for the first three decades. Today that pace is much slower. If the rate of increase in volume of bits slows to below the average rate of bit price reduction (historically 27% per year), overall industry revenue will drop. The industry would then have a most difficult time funding the critical research and development necessary to make technical improvements.

The cost per bit of DRAM production is primarily set by areal bit density, assuming that high yield can be achieved and that the economic scale is large enough to amortize the investment costs. The market price, however, is dominated by supply and demand. In a field of such high investment with a long time of implementation and return on investment, the stage is set for great volatility. The DRAM industry has therefore been marked by major swings. This unpredictability was a key reason for major companies such as Intel and IBM to move away from the DRAM business, leaving it to companies able to risk major resources.

The relationship between DRAM technology and logic technology has also gone through a major shift. In the 70's, most logic was built in bipolar technology. As NMOS, and then CMOS, grew popular as a cost-performance technology, DRAM became a technology driver. It had the volume scale and the requirements to enable an effective investment for technology development. The resulting transistor was then used as a low cost logic element. As the opportunity grew for higher performance CMOS logic, the requirements for logic and DRAM transistors began to diverge. Low leakage, high threshold voltage devices were needed for DRAM applications while lower threshold voltage transistors were necessary for logic performance. Gradually, the technologies were decoupled, though DRAM's were still viewed as a driver for process equipment, particularly lithography, and defect reduction.

THE FUTURE OF DRAM'S

Today the lithography technology driver role has largely migrated to non-volatile flash memory. The flash memory industry is remarkably similar to the DRAM industry, with about a 16 year lag. It is currently growing much faster than DRAM's and the market is demanding a more rapid increase in bits per chip for flash compared to DRAM's. With less demand for performance, flash can tolerate multiple bits per cell, helping to reduce effective cell size. Flash chips with 64Gb of memory are now in development.

At each generation of DRAM development, immense technical difficulties have led to doubts about future scaling. So far, all hurdles have been met but no exponential continues forever. Dielectric films on the order of a few atomic layers thick seem to be as thin as could ever be achieved. Transistors are so difficult to turn off that further scaling seems likely to lead to unacceptable leakage. Yet, innovation continues to thrive. Young engineers who don't know the

CROSS-CULTURAL DRAM DEVELOPMENT

One of the most rewarding experiences of my career was the privilege of leading the joint 64Mb DRAM development project with IBM, Siemens, and Toshiba from 1990 to 1995. Skyrocketing development costs forced DRAM manufacturers to join forces, sharing process lines and skilled engineers as well as costs.

Global alliances were already common, but forging a close-knit team for an aggressive chip development project was a much greater challenge. Cultural differences were most obvious and had to be addressed explicitly. Language issues were immediately resolved with education and careful explanation of all unfamiliar terms. Only later did we observe the insidious danger of multiple meanings or alternative connotations of words that slipped by with no awareness of the lack of understanding.

The problem of corporate cultural differences was less anticipated. We learned by experience that each company's employees brought a different expectation of the way in which decisions were made and reported. Democratic, autocratic, and oligarchic approaches to authority had to be blended and respected. Communication styles varied widely. Americans preferred bullets in a slide show; Germans preferred technical memos with infinite detail, while Japanese excelled in personal behind-the-scenes conversations. Corporate priorities also differed. Americans emphasized good news and progress; Germans wanted a focus on issues and remaining problems, and the Japanese valued public consensus.

Each company derived significant benefit from the joint development program that transcended cost reduction. Sharing the skills and experience of engineers from three different DRAM manufacturers led to an effective collective wisdom. IBM's penchant for in-house tools and solutions came to be reconciled with Siemens' and Toshiba's preference for industry-standard methods. Vigorous debates on strategic directions for DRAM's were sharpened by our global perspective.

On a personal level, all engineers from the three companies expressed appreciation for the value derived from their experience. Befriending and working with colleagues from other cultures shaped our lives in a most positive way. I found the experience to be stimulating on many levels. Beyond the business and technical value, the friendships forged during our common focus on product development remain to this day.

meaning of “impossible” seem to find new ways of solving what appear to be intractable problems.

Competing technologies must provide superior performance and lower cost to be seriously considered as a DRAM replacement. Magnetic tunnel junctions have been touted for their speed, but have not yet met cell size requirements. Phase-change memory is a research candidate that might meet both speed and size requirements, but no technology has yet matched CMOS DRAM’s in reliability. The DRAM industry has nearly 40 years of experience in learning how to meet rigorous reliability criteria. New technologies are likely to be tested first in applications with less stringent requirements. The computer industry cannot afford to jump into a new technology until all aspects have been clearly demonstrated in volume.

DRAM memory cells are now being deployed as embedded memory in logic technology, offering a lower cost, lower power alternative to SRAM memory cells. The greater soft-error immunity of DRAM’s give them an edge as well as superior density. On-chip performance has been demonstrated that nearly matches SRAM speed. DRAM and logic technologies have been largely decoupled as specialization demands fine-tuned process technology. Though the technology differences mean that additional process steps and costs are required to embed DRAM cells, in many cases higher performance is worth the extra cost. Embedded DRAM arrays are ideal for growing demands for directory and cache applications on microprocessors. The DRAM industry therefore has the opportunity to branch into new applications.

DRAM played a critical role in establishing Moore’s Law, leading the industry in technology development and enabling major improvements in computing systems. The DRAM industry is far from over, even though its leadership role is no longer as strong.

Although the pace of increase of bits per chip may have slowed down, the pace of progress continues and the enduring legacy of DRAM technology will never disappear.

References

[1] Moore, Gordon E., **Electronics**, Vol **38**, No. 8, April 19, 1965.

[2] Moore, Gordon E., **Proceedings of IEDM**, 1975, p. 11

[3] “Field-Effect Transistor Memory DRAM" (U. S. Patent No. 3,387,286. 1968)

About the Author

Randall D. Isaac became Executive Director of The American Scientific Affiliation after his retirement from IBM in 2005. He was previously Vice President of Strategic Alliances for the IBM Systems & Technology Group. From 1996 to 2003 he served as the Vice President, Science and Technology, for the IBM Research Division where he had worldwide responsibility for semiconductor, packaging, and communications technologies.

In 1995 he was the founder and Director of the IBM Austin Research Laboratory in Austin, Texas which focuses on high-performance microprocessor design. From 1990 to 1995, Dr. Isaac was a senior manager in the Semiconductor Research and Development Center of the IBM Microelectronics Division in Burlington, Vermont. In this capacity, he was the project manager for the 64Mb DRAM development joint program with Siemens and Toshiba. From 1987 to 1990, he was Director of Silicon Technology in IBM Research in Yorktown.

Dr. Isaac received his B.S. degree in physics from Wheaton College in Wheaton, Illinois in 1972 and his M.S. and Ph.D. degrees in physics from the University of Illinois at Urbana-Champaign in 1974 and 1977, respectively. Dr. Isaac joined IBM in 1977 at the IBM Thomas J. Watson Research Center at Yorktown as a Research Staff Member in silicon technology.

Dr. Isaac is a Senior Member of IEEE , a Fellow of the American Physical Society, and a Fellow of the American Scientific Affiliation.

DRAM – A Personal View

R.C. Foss, Founder and Retired Chair, Mosaid Technologies, Inc., dickottawa@rogers.com

Foreword. This article charts the story of Dynamic Random Access Memory and its crucial role in the inter-twined development of both the computer and semiconductor industries. It is based on the work of the author in the design, specification and test of DRAM over more than thirty years. During this time, it evolved from a chip with 1024 (1K) bits to parts in production having 256 *mega* bits. This bit density increased by a factor of 4 every three years or so, partly as a result of design sophistication, process complexity and an increase in chip (die) size. But mostly it came from the reductions in feature sizes from 10 microns or so to around 0.1 micron. Over the years the trend has been known as “Moore’s Law” after an observation by Gordon Moore. Apart from driving the semiconductor industry, it has been the single most important enabling technology of the computer world and its tentacles reach into every aspect of modern life.

The Beginnings. From the earliest machines up to today’s PC’s, the usefulness of computers has been dependent on the size and performance of their memories. The first machine ever to run a program stored in its memory, the Manchester “Baby,” had an advanced memory (for its day), storing 1K and later 2K bits in a “Williams tube”.[1] Fig.1.

(As a personal aside, its inventor (to credit Tom Kilburn) was this author’s external examiner for the doctorate!) It had a pleasing link to the DRAM in that each serial word could be randomly accessed and was stored as an electron charge which needed to be refreshed every 300 to 400 microseconds. The charge was stored on the face of a Cathode Ray Tube (CRT), as vacuum tubes had yet to be supplanted by transistors, never mind silicon chips, in 1947. Machines using the Williams tube included the IBM 701 and 702. The idea surfaced again in the “BEAMOS,” a device from GE with an electron beam in a vacuum and an unstructured silicon target.[2]

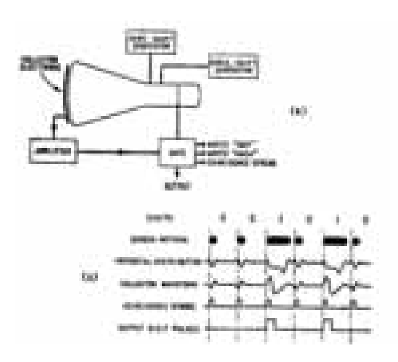


Fig.1 Operation of Williams Tube Memory.

The next standard approach to building memory was the magnetic core.[3] Fig.2. In one respect, that was a step backwards as each bit required threading wires through miniature toroids. When silicon chips using Metal-Oxide-Silicon (MOS) technology could be packed with hundreds and then thousands of transistors, memory could get back to having individual bit storage locations that did not need separate assembly.

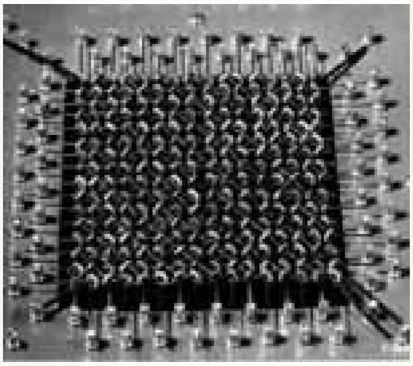


Fig.2 16 x 16 Core Memory (1951).

IBM did pioneering work aimed principally at improving the speed of memories in its own computers. However, it was Intel, founded by Bob Noyce and Gordon Moore to make memory chips, that in 1972 made and sold in volume a chip that is sometimes called after a famous aircraft, “the DC 3” of the industry.[4] The i1103 was a 1K DRAM chip made with silicon-gate p-channel technology. It had 32 rows and 32 columns of memory cells, each having three MOS transistors. Fig.3.

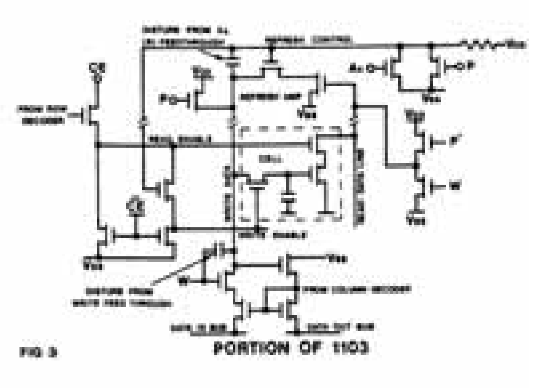


Fig.3 i1103 : Sources of Pattern Sensitivity.

When charge was stored on the gate of an inverter transistor, it turned it “on” and the remaining transistors were used to write in the data signal and to subsequently read it out. Thus, the bit state was “refreshed” every 2ms with a “refresh amplifier” at the top of each column. The chip ran on a comparatively high drain voltage of -17V and it was found to need a bias supply of +3V between the n substrate and the p-channel sources to ensure minority carriers in the substrate did not attack the stored charge in the cells. Substrate bias was to play a key role in all DRAM history, and the need for an extra pin made 18 pin dual-in-line packages a memory standard (rather than the then-standard 14 pins for logic).

Being on the edge of process feasibility, the i1103 was difficult to manufacture. It also suffered a number of “pattern sensitivity” problems because its write columns floated, rather than being held to a set state at key moments.[5] These issues and the need for buffers to drive high level inputs, made it hard to use as well. Despite this, its cost fell below 1 cent/bit, which seems ridiculously high now but started to compete with the core memories of the day at the system level. A factor in its acceptance was a second-source, licensed by Intel to MicroSystems International in Ottawa, Canada (where the author worked up until its closure in 1975). A few other companies offered their own independently developed parts, but the manufacturing difficulties led to few successes.

Intel followed the i1103 with an n-channel 4K bit device, the i2107. This retained the 3T cell, putting it at a density and cost disadvantage compared to the then-emerging single transistor (1T) cell device (next section). However, it did have lower power than the first 1T cell parts and so found a niche market with Bell Labs. As they remained responsible for paying the power (and air conditioning) bills, the device's initial cost was only one consideration. The charge stored on the now still-smaller gate was such that it became the first part to show "soft errors." (See "Soft Errors" sidebar, pg 55.)

The emergence of the single-transistor cell DRAM. The idea of using just one transistor to both write charge into a capacitor and then read it out when accessed, emerged well before the first commercial parts. IBM's Dennard is credited with realizing the merits of the cell in a patent in 1968. [6] In the late 60's, an early custom MOS company (AMI), undertook work for Shell Oil, which needed denser memory for its transportable computers used in seismic analysis. As a result, Shell finished up owning some DRAM patents which it used to collect royalties! A key paper published by Stein of Siemens [7] introduced the idea of dividing the bit line and placing a flip-flop in the center. This served as a differential sense amplifier for the modest signal developed as the small cell capacitance shared its charge with larger capacitance of the bit line on one side, with the bit line on the other side serving as a reference. As the sense amplifier developed a full logic swing, it automatically restored the signal back in the cell. Fig.4.

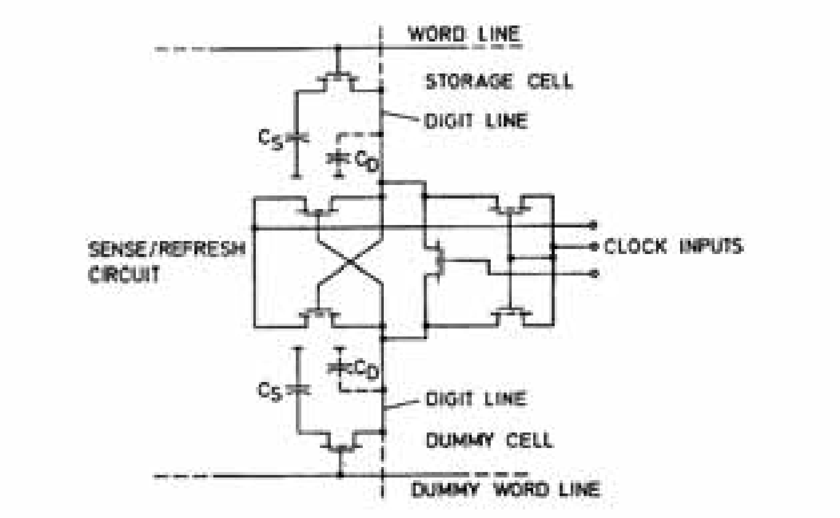


Fig.4 One-Transistor Cell with Sense/Restore.

The first commercial part featuring this cell and sense amplifier arrangement was the n-channel TMS 4030 from Texas Instruments. This used a 12V supply and a –3V (later –5V) substrate bias and consumed significant power. Like the subsequent i2107A from Intel and some other contemporary 4K parts, the sense amplifier flip-flop had pull-up loads that drew current during the active cycle. Thus, there was a trade-off between the power drawn and the cycle time as the bit line was restored high. Although the supply was 12V, the part could accept standard TTL (Transistor-Transistor-Logic) logic levels, although the poor design of the address input buffer meant it still really needed a special driver. The package standard for this generation was a 22-pin 0.4" pin spacing dual-in line (DIP), though this was later reduced to an 18-pin 0.3" DIP to compete with the newly emerging multiplexed address parts.

Address Multiplexing. The next milestone in the DRAM story was the establishment of the address-multiplexed part which set the basic functional standard specification for some two decades. [8] This is credited to Bob Proebsting of Mostek, who had introduced the idea to the market around 1975 in its MK4096 4K part. The key concept was that in the operation of a DRAM, the ***row*** address was required first to select all the cells on one column. Only ***after*** sensing would the column address be needed to select which column was to be written into or read out so that a Row Address Strobe (RAS bar as it was active low) could time the row addresses and a corresponding CAS bar would follow to feed in the Column addresses. RAS/CAS memories would go though multiple generations for the next two decades until the Synchronous DRAM (SDRAM) would be standardized by JEDEC (Joint Electron Device Engineering Council), the industry standardizing body. Even then, the command signals , would keep RAS and CAS names to ease understanding. Multiplexing the address pins in this way not only reduced the pin count needed but offered other functions. For refreshing the cells, no column address was needed, hence "RAS-only refresh." After a row was selected defining a "page" of data, several columns could be rapidly selected in "page mode," although the pioneering part, the MK4096 was only a limited success as it used a more complex process than its competitors and did not use the emerging standard circuit approach of a balanced sense amplifier. This was all to change with the circuit genius of Paul Schroeder. The MK4027 replaced the earlier 4K and a closely related 16K, the MK4116 was to be a land-

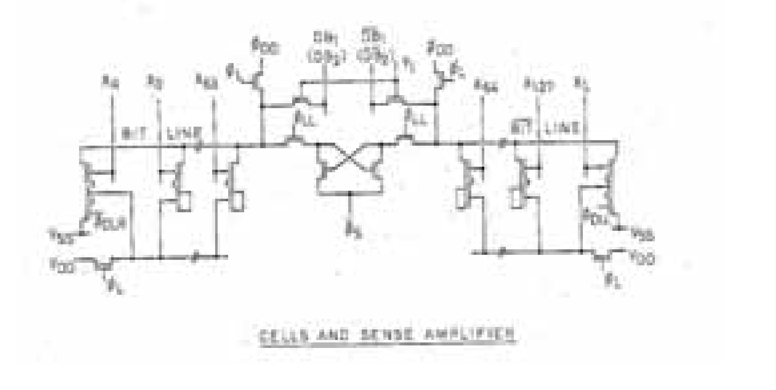


Fig.5 4116 : Precharged High Bit Line.

mark part in the industry.[9,10] Fig.5.

The 16K and the MK 4116. The MK4116 was the definitive design of the 16K generation. Every part made by every maker was either an exact copy or at least owed a great deal to its design, with the sole exception of Fujitsu. The author's company, MOSAID, alone sold its own version of the design to four companies and in the process standardized its nomenclature for the internal interfaces of the part. Cell size was reduced by the introduction of a second layer of polysilicon. Fig. 6.

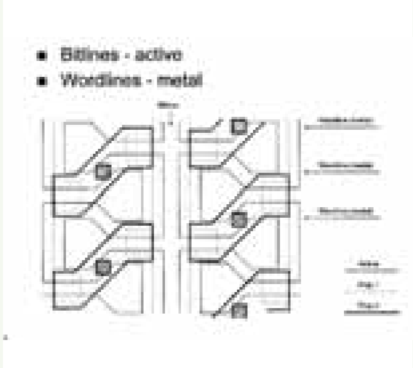


Fig.6 MK4116 Double-poly Cell.

Power was minimized by eliminating sense amplifier pull-ups and instead precharging bit lines to the full 12V-supply level. The column decoder was placed symmetrically in the center to give balanced access to both halves of the bit line. A novel clock buffer design minimized the power consumed in establishing charge on the "bootstrap" capacitor. Fig.7.

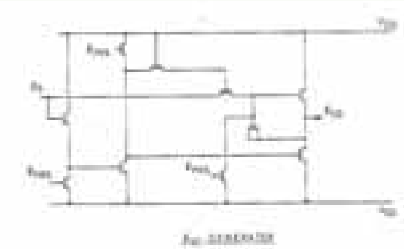


Fig.7 Schroeder Clock Buffer, Delay Stage, Dynamic R-S Flip-Flop used in MK 4027 4K and MK4116 16K.

This further increased speeds in the peripheral circuits. These clock buffers also drove the address input buffers that were themselves internally multiplexed to save silicon area. To ease debug testing, an ingenious "margin test" mode switched the internal write drivers from operating with the 12V drain voltage supply, VDD, to the 5V TTL I/O supply, Vcc, but only when an "illegal" low CAS bar input level was used. This allowed exploration of the cell operating margins by varying the levels written into the cell.[11]

The 4116 would be developed though "shrinking" the die in revisions A through G, each revision giving further improvements in cost and performance. The "F" version was found to have enhanced soft-error issues. The 16K generation was to be the last to use 12V, 5V and –5V supplies and was the last generation to be dominated by US semiconductor companies serving the merchant market.

Achieving a 5V-only part. The next generation, 64K chips, needed line widths that could not allow transistors to operate on 12V supplies. Attempts were made by Bell Labs[12] and IBM to establish supply levels around 8 volts but there was no market acceptance as the next lower voltage was seen as the 5V supply, already in widespread use for logic devices such as TTL. Taking such a big jump was seen as a difficult design problem. The transistor threshold voltage could not be scaled proportionately and so the cell "one" level would become an issue. Indeed, the MK4116 running with its bit line precharged to 12V could have as little as only 8V as a cell "one" level. This was due to the back-gate effect of source to substrate potential enhanced by the narrow channel effect in the access transistor with its gate at 12V. The eventual solution to this problem was to bootstrap the word line level by at least a threshold voltage above the new 5V supply. A less obvious difficulty became evident in eliminating the –5V substrate bias supply. A "pumped" supply was possible but created new problems. One was the risk that a diode between the pumping transistor and the substrate would conduct and inject minority carriers into the substrate. The other was peculiar to 4116-type circuits, with the common source point of the sense amplifier flip-flop floating just one threshold voltage lower than the bit lines. With no decoupling capacitor on the substrate supply, the unselected row decoders kicked their diffusion capacitance low. The substrate level then fell. This in turn coupled into the sense amplifiers, sufficient to have them start to sense their own unbalance before any signal to sense existed! Fig.8.

Solving all the 5V supply problems took a little longer than the usual three-year generation gap and in that time, Japanese makers would emerge as major players.[13,14]

Mostek would design a part radically different in its circuit design from the MK4116 aimed at fixing some of its problem points. Many people moved from Mostek including a talented designer, Dennis Wilson, who went to a new company in Boise, Idaho, Micron Technology. Its first product was a

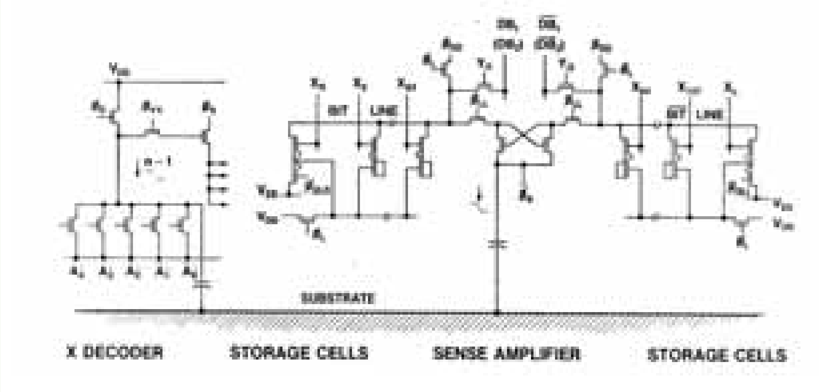


Fig.8 Coupling via a floating Substrate.

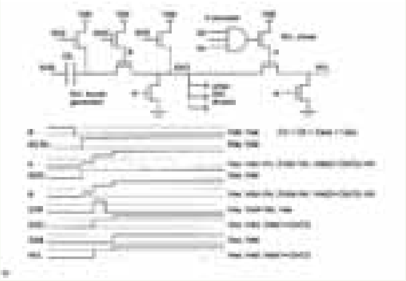


Fig.9 Double-Bootstrapping a Word Line.

successful 64K, subsequently also built under license by Samsung, ITT Semiconductor and Commodore personal computers.

Japanese Design Approaches. A quite different design philosophy was to become evident in Japanese 64K designs and generations. The MK4116 had spotlighted the success of highly original designs. Indeed, a designer's career would get a boost from an original paper at the International Solid State Circuits Conference (ISSCC). Culturally, the Japanese emphasized a team approach and showed less tendency to suffer from NIH (Not-Invented-Here!) syndrome. Unfairly seen as just copyists in this as in other areas, they would start with a successful concept and then further develop and improve it.[15] So, for example, the Hitachi 64K [16] used a folded bit line but still used scaled 4116 style circuits.

The folded bit line had been invented in at least three companies in the 4K era. By "folding" the balanced bit line halves to lie parallel, several advantages accrued. Better balance, even to noise from substrate coupling and also simpler column access and simpler column shorting for precharge set up, were key benefits. Despite this, the Hitachi 64K design retained the more complex circuitry that had been used in the MK 4116 to effectively tie together the bit line halves! As will be seen, when Complementary MOS (CMOS) using both n and p-channel transistors became the normal way of building DRAM, the Japanese, by then dominant, were to still retain the old n-channel bootstrap approach to having the word line driven above the supply voltage.

Early CMOS Work. The 256K generation was still n-channel, with Fujitsu a leader surprisingly not using the folded bit line as it had in its 16K. However, two companies pioneered the use of CMOS. One was Intel in its last attempt at the DRAM market. A key feature of Intel's 256K was its use of redundancy. Spare rows and columns to replace defective ones or defective cells were selected by blowing fuses at wafer probe. Redundancy was to become universally adopted for yield improvement, despite early misgivings on reliability. Intel however, abandoned the DRAM market and moved to become the world's leading microprocessor house while continuing memory work only for non-volatile products. The other CMOS pioneer was INMOS, a company funded by the British Government with its memory development team in Colorado. That group was headed up by Paul Schroeder. Its innovative CMOS 256K was licensed to Hyundai and the Japanese company Nippon Miniature Bearings (NMB). As a newcomer to semiconductors, NMB evidently saw its business in electromechanical products evolving in other directions! INMOS had management problems not unrelated to the geographic split and their backers ! So it was that CMOS processing had to wait for the 1M generation.

The CMOS 1M. All the major (and several smaller) Japanese semiconductor makers were now the dominant suppliers of DRAM. The leading 1M was clearly that built by Toshiba. Its design was solid and conventional and, as already noted, was to keep the n-channel approach to boosting the word line. Fig.9. It was licensed to Motorola and also to Siemens, and the form of its CMOS process inspired several other houses.

As something of a standard process now existed to work with, MOSAID began work on a design better utilizing CMOS capabilities. The difficulty with using a bootstrap approach to driving the word line was in designing a circuit giving a high enough level without over-driving nodes to where the level was greater than could safely be maintained. While this was not insoluble with 1M parts, it would clearly be an issue in later generations as feature sizes were reduced. The solution was found in using a pumped supply at a level set by feedback-control to be used by the word line driving circuits.[17] This required significant departures from established circuits in several areas.[18] However, a successful 1M chip was built and the use of feedback control allowed it to subsequently scale unchanged to 4M processing. Fig.10.

In fact, with some enhancements reducing standby power, it has been successfully used right through to the current generation. As had been foreseen, with variations, the use of a pumped supply replacing the bootstrap technique became the industry's standard approach.

Process sophistication. The addition of the second layer of polysilicon in the 16K had marked

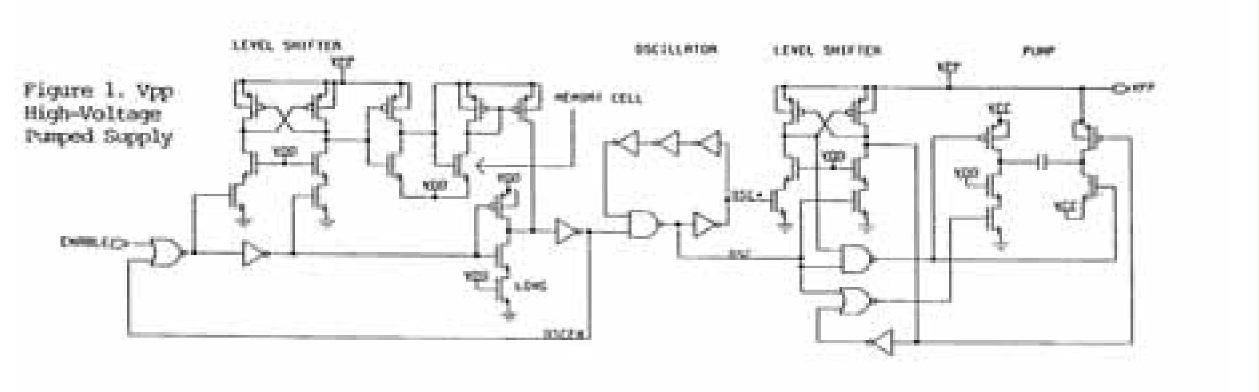


Fig.10 Regulated Supply System for Word Line.

an early departure from processing used in other products. This allowed more capacitance in a smaller cell area. Capacitance as determined by the square of linear dimension and oxide thickness, was falling relatively faster than simple feature size scaling. A fixed-target value was set in the range 30 to 50 fF to both ensure an adequate ratio between cell and bit line capacitance (to achieve enough signal sensing margins) and, as was being discovered, for enough stored charge to resist soft error effects. By the time 4M densities were reached, new approaches were needed to achieve sufficient capacitance. As in construction work, the only possibilities were to dig down or build up! Both approaches are still used. One involves etching a hole in the substrate to build a "Trench" capacitor. Fig.11.

This figure shows the early version, whose problem was that depletion regions around the trench could reach an adjacent structure. This was fixed by arranging for the cell stored charge to be on the *inside* of the trench. The alternative was to use more layers of conductor and dielectric *above* the surface, a "Stacked" capacitor. This requires additional processing to restore a reasonably flat surface topology.

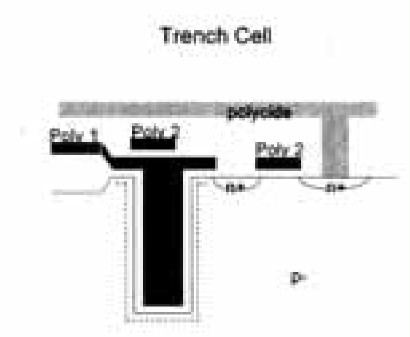


Fig.11 Cross Section (Stored Charge on Outside).

With the increase in mask layer numbers (6 for a 4K to around 30 for a 256M), far smaller feature sizes, bigger diameter wafers (10 going to 30cm) and cleaner environments to achieve yields of good die, the cost of manufacturing facilities has increased exponentially. $30 million would buy a fabrication line for 4K parts. Today, a fab line costs upwards of $5 billion. Not surprisingly, the industry has consolidated to the extent that only a handful of DRAM suppliers remain.

The change to Synchronous DRAM (SDRAM). Starting from the pioneering 4K DRAM right up to 16M (six generations!), the basic RAS/CAS specification had remained the industry standard. Numerous additions had been made over the generations. For example, on-chip row-address counters were added to allow the DRAM chip to refresh itself. Nevertheless, the pressure to maintain back compatibility of function with at least the previous density was very strong. Pushing standard DRAM to the limits of performance and functionality is illustrated in an IBM paper describing a 16M. This had both redundancy and error correction as well as a mode register to define additional functions. [19] Although density (and so cost) and power consumption per bit had all improved by orders of magnitude, there was remarkably little improvement in speed performance. Access time to a random bit of data, about 150 ns in a 4K, was improved by only a factor of three in the 16M.

In part this was due to the retention of the TTL interface standard whose interface specifications had been set in the mid 1960's! The independent asynchronous timings of the inputs and outputs timed to 10% and 90% levels were difficult to marry with increasing system clock speeds. In the early 1990's, the issues were all addressed in the JEDEC standards committee. This resulted in a new standard for Synchronous DRAM issued in November, 1993 as part of JEDEC standard JC21. Contributions made by representatives of suppliers and users from many companies had been incorporated. All signals were timed with reference to a single clock which could operate at frequencies of up to around 100Mz.[20] To allow for operation at a range of frequencies and for various bit counts in bursts of data, on-chip registers could be programmed in a set-up mode. All this was a huge change in the complexity and sophistication of DRAM functioning, but eased the task of system designers as computer speeds were increasing dramatically. Without the change to SDRAM, memory performance would limit what processors could achieve even when using cache memory architectures to speed access to frequently used data.

Double Data Rate SDRAM (DDR SDRAM). As SDRAM was widely adopted, it became clearer that there were some changes needed in the basic specification. The challenge of a proprietary specification promoted by RAMBUS and supported for a while by Intel had been fought off by the performance of SDRAM, but further speed enhancements were needed. DDR matched the frequency of the basic clock with the frequency of 10101…. data streams by synchronizing to *both* edges of the clock. A delay-locked loop matched the timing of the output data and its matching data strobe to the input clock. [21] The JEDEC standard for DDR appeared in June 2000, JESD - 79. Most importantly, an interface specification appropriate to the high speeds was standardized. An earlier arrangement using a symmetrical drive around a mid-point level had been standardized as "CTT" in JESD - 8-4 in November 1993. However, the contemporary SDRAM's still retained a TTL specification. CTT was improved and standardized by EIAJapan and then adopted by JEDEC as JESD- 8-8 "SSTL." This had the same symmetrical drive around a mid-point level but added Series Stub Terminating resistors (hence SSTL) to suppress transmission line reflection effects. Present DDR2 memories, JESD-79-2, represent further enhancements in speed performance and avoid the need for separate external discreet resistors in the data-path. DDR3 is now expected to become a mainstream part in 2008. Interestingly, progress in bit density is no longer the main thrust in DRAM development: densities now double rather than quadruple each generation, from 128M to 256M to 512M. Instead, the driving forces are performance and power (DDR3 operates on 1.5V).

Conclusions. In the broad field of silicon chip circuit design, the sheer scale of modern parts has forced increasingly structured design methodologies with Computer-Aided-Design tools taking over virtually all the traditional tasks of the circuit designer. Exceptionally, over the decades, DRAM design has remained a pinnacle of the circuit designer's art. New circuits interacting with creative layout combined with a deep understanding of transistor behavior have been involved at every stage and in every generation. The competitive pressure to better performance and lower costs in high volumes has been, in this author's view, the key driver for the semiconductor industry. Often it has been creative individuals with broad multi-disciplinary backgrounds who have, in turn, driven DRAM advances. Just a few have been cited in this piece. But this author is proud to have met and known many of them from many companies in many countries.

Soft Errors. Starting most famously with the 1K 1103, early DRAM designs, showed that errors could be found that depended on certain patterns of data or address. Tests were created to screen for such errors and many test patterns carried over to later parts with quite different problems. Of course, manufacturing defects were also detected by the general test sequences that were used. Bit-map testing allowing an engineer to see error patterns helped greatly in understanding what had gone wrong in a specimen chip.

The discovery that DRAM's could exhibit "soft errors," in which random bit locations could lose their stored contents caused great concern. There was no way to test for susceptibility, and a bad bit in a stored program could and did cause a system crash. The source of the problem was discovered by Intel and published by May and Woods in a classic paper. [22,23] An alpha particle (helium nucleus) striking the silicon did not permanently damage the crystal structure but did create hole-electron pairs. These occurred along the ionization track, concentrated as the particle came to a stop. The million or so electrons thus created as minority carriers in the p-type substrate represented a charge of around 150 fC. These could be attracted to either a cell or an n-diffusion in the bit-line/sense amplifier structure. Given a 3V signal margin in a 50 fF cell (a charge of150fC), signal could be lost, particularly if the particle had struck a glancing blow. Even a Static RAM using high resistance loads was found to be vulnerable with even less "stored" charge. Fig. 12.

With a single particle sufficient to cause a data loss, even minimal radio-active contamination was a serious concern. A particularly bad material was gold with a thorium contamination. Packaging with a wire bond termination pad at just a higher elevation than the chip made for a prolific source, but just about any material could serve, including material of the chip itself.

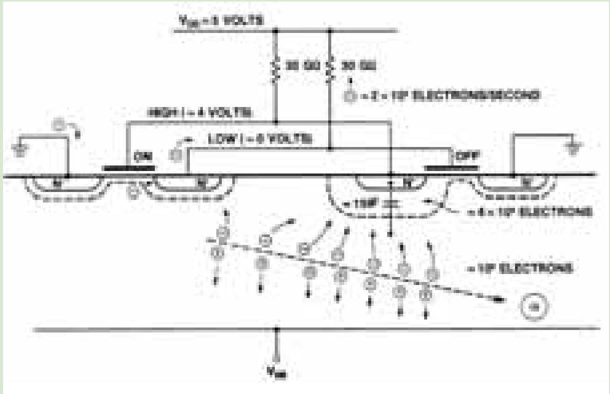


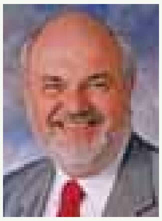
Fig.12 Alpha Strike on R-Load Static RAM

The counter-measures were to ensure a minimum cell capacitance, control of materials and modifications of the substrate doping profiles to help repel wandering minority carriers. As geometries shrunk, there was also a fortunate tendency for a single cell to have a smaller cross-section capture area, minimizing the collected charge. In the context of a personal computer using no error-correction, common experience suggests that a data error or crash is much more likely to be a software problem. After the publication by May and Woods, one computer company executive noted that both his hardware designers and his programmers would each have matching complementary excuses!

References

1) ”A storage system for use with binary digital computing machines” F.C. Williams and Tom Kilburn. Proc. IEE Vol.96 Pt II April 1949 pp 183 – 202
2) “BEAMOS. A new Electronic Digital Memory” W.C.Hughs et al. ational computer conference, Anaheim, May 1975
3) “Digital Storage Techniques” W. Renwick. Proc. of the 2nd. Oxford Electronics Lecture Course, 1966. pp 100 -106
4) “A 3-transistor cell 1024 bit 500 ns MOS RAM” W.M. Regitz and J. Karp. Digest of Technical papers ISSCC 1970
5) “MOS Memory cells and their engineering implications” R.C. Foss and J. Monico. Colloque international sur les circuits integres complexe Paris Dec. 3 – 6th. 1974. pp 233 - 239
6) US Patent 3,387,286 Denard
7) “Storage array and sense/refresh circuit for single-transistor memory cells” K.U. Stein et al. Digest of technical papers ISSCC 1972. pp 56 -57
8) “A TTL compatible 4096-bit n-channel RAM’ R. Proebsting and R. Green. Digest of technical papers ISSCC 1973. pp 28 – 29
9) “A 16K x 1 Bit dynamic RAM” Paul R. Schroeder and Robert J. Proebsting. Digest of technical papers ISSCC 1977 pp 12 – 13
10) US Patent 4,061,954 Proebsting and Schroeder
11) “Margins and margin testing in dynamic RAM” R.C. Foss. 1980 IEEE Test conference. Pp 4 – 6
12) “A fault-tolerant 64K dynamic RAM” Ronald P. Cenker et al. Digest of technical papers ISSCC 1979
13) “The 64 Kb RAM teaches a VLSI lesson” R.C. Foss (interview). IEEE Spectrum June 1981. pp 38 – 42
14) “Rethinking the 256 Kb RAM” Robert Bernhard. IEEE Spectrum. May 1982. pp 46 – 51
15) “VLSI memory: a designer’s view point” R.C. Foss. Proc. conference on advanced research in VLSI. Massachusetts Institute of Technology, Cambridge . Jan.25-27. 1982 pp 94 - 96
16) “A single 5V 64K Dynamic RAM’ Kiyoo Itoh et al. 1980 IEEE International Solid-State Circuits Conference pp 228 – 229
17) “High-Reliability circuit design for megabit DRAM” P. Gillingham et al. IEEE JSSCC, Vol.26, No.8 Aug. 1991. pp 1171 – 1175
18) US Patent 5,267,201 R.C.Foss
19) “A 50ns 16Mb DRAM with a 10ns data rate” Howard Kalter et al. 1990 IEEE International Solid-State Circuits Conference pp 232 –233
20) “High-speed circuits for Mega-bit Synchronous DRAM’s Tomasz Wojcicki and R.C. Foss. 4th. International conference on VLSI and CAD Oct.15- 18th. 1995, Seoul Korea.
21) US Patent 5,796,673 Foss et al.
22) “new physical mechanism for soft errors in dynamic memories” T.C. May and M.H. Woods. Proc. of the 1978 International reliability physics symposium and IEEE Trans. Electron devices Ed – 26 No.1 Jan. 1979
23) “Soft error testing” T.C.May et al. 1980 IEEE test conference. pp 137 - 149

About the Author



Richard C. (Dick) Foss, Founder and Retired Chairman of the Board of MOSAID Technologies Incorporated, was born in 1936 and educated in the U.K. He joined the EMI group as an apprentice in 1952 and worked on the design of the first EMI business computer – a vacuum tube machine. Simultaneously, he studied for a higher National Certificate in Electrical Engineering and Graduate Membership of the IEEE, passing with distinction in 1956.

A scholarship then took him to the University of Durham, where he studied for his B.Sc. in Electrical Engineering (awarded with First Class Honours in 1959) and his Ph.D. in Electronics (awarded in 1964 after the work was used in missile telemetry systems by EMI). His career then turned to microelectronics with the Plessey Company, where he led a pioneering circuit design group with many creative successes in linear ICs, high speed counters (the subject of a 1968 International Solid-State Circuits Conference paper) and early MOS devices.

In 1970, Dr. Foss left the U.K. to join Microsystems International (MIL), a Canadian company located in Ottawa, Ontario and worked in various positions including head of design, MOS engineering manager and new products manager. Together with a colleague, Robert Harland, he worked on a trend-setting 4K DRAM that was the subject of a 1975 ISSCC paper. At its closure in 1975, MIL had become the second largest supplier in the world (after Intel) of MOS memory and microcomputers.

Richard Foss and Robert Harland founded MOSAID in 1975. Dr. Foss held various positions with the company, including President and Chief Executive Officer. He served as a Director from 1975 and was Chairman of the Board from 1984 until his retirement at the end of 2001. He currently serves on the Technical Advisory Boards of MOSAID and Innovative Silicon in Lausanne. He also assists in the licensing of key memory patents granted to him while active in MOSAID. Many major companies in the industry are now licensed under these patents.

Dr. Foss has published numerous papers pertaining to semiconductor design, including invited papers at major conferences. He was also elected a fellow of the IEEE for “leadership in the design and testing of memory circuits.”

Asad Abidi Recognized for Work in RF-CMOS

Anne O'Neill, Executive Director of SSCS, a.oneill@ieee.org

Asad Abidi will be recognized at the ISSCC Plenary in February with the IEEE Donald O. Pederson Award in Solid-State Circuits "for pioneering and sustained contributions in the development of RF-CMOS." This recognition, within a 20-year history of circuit designer greats, is the highest IEEE technical field award for Solid-State Circuits.

Abidi's award has generated responses from many experts in the field, not only for his early and steadfast advocacy of RF CMOS but also for his fundamental development work on the problems essential to making RF CMOS a product for broadly used consumer applications.

According to Akira Matsuzawa, previously general manager for System On Chip development at Panasonic and now a faculty member at Tokyo Institute of Technology, "Abidi prepared the needed technical solutions to help industry apply the technology. He also prepared the professionals that industry needed to develop the solutions." Abidi has delivered many technical seminars in Japan. "When he teaches," says Matsuzawa, "he starts by explaining seemingly strange phenomena and their basic underlying mechanisms. Then he follows up with the solutions that are fundamental and yet the smartest."

Richard Spencer of UC Davis and primary author of *Introduction to Electronic Circuit Design* (Prentice Hall, 2003) calls Abidi a consummate engineer. "He has always placed the highest priority on coming up with truly useful solutions to significant problems, rather than succumbing to the temptation of working on projects that would maximize his publication rate."

Asad Abidi, IEEE Fellow, member of the National Academy of Engineering and Professor for 22 years at UCLA, is now the first Dean of a new School of Science & Engineering in Pakistan. LUMS is a private endowment-based university modeled after MIT and Caltech.

Tom Lee of Stanford and author of *The Design of CMOS Radio-Frequency Integrated Circuits* (2E, Cambridge University Press) counts Abidi as an inspiring pioneer. "My own thesis work on RF CMOS in the 1980s interested absolutely no one at the time," he says. "Professor Abidi was the first expert I encountered -- in academia or industry -- who not only expressed interest, but felt certain that RF CMOS had a bright future. His steadfast advocacy of this position -- despite the negative view held by almost every other expert -- went a long way toward establishing CMOS not only as a credible RF medium, but in many cases, superior."

Payam Heydari, whose JSSC article this fall on "Design and Analysis of a Performance-Optimized CMOS UWB Distributed LNA" was among the top 100 downloads in Xplore, points to Abidi as a "role model to many younger faculty members" including himself. But Abidi's continuing and current work on software–defined radio is Heydari's "ah-ha" moment, particularly research published in the JSSC (December 2006 and May 2007) that "lays the groundwork for future development of multi-standard programmable transceivers."

Teacher of the teachers

World class teachers Matsuzawa and Spencer recall Abidi helping them to better understand concepts with lessons lasting a lifetime. Matsuzawa remembers how impressed he was when Abidi showed him "the mechanism of AM-PM conversion and frequency conversion in a voltage controlled oscillator and the appearance of 1/f noise in a mixer." A vivid memory for Spencer from his graduate work on relaxation oscillators at Stanford is Abidi's "very clean geometric picture of how noise on the threshold was converted into jitter and how that conversion depended on the bandwidth of the noise relative to the slope of the waveform."

New Path As Dean at LUMS

Abidi is leaving his LA home and a settled 22 year existence at UCLA to begin what he calls an adventure to serve humanity as the first Dean of a new School of Science & Engineering in Pakistan (sse.lums.edu.pk). LUMS is a private endowment-based university modeled after MIT and Caltech, with an advisory group drawn from those and other reputable institutions.

Nominations Open for 2010 Recipients

Nominations for the 2009 recipient of the Pederson Award close 31 January 2008. The nomination and reference process takes some thought and effort. So begin now with the inspiration of this year's recipient fresh in your mind. Discuss with your colleagues, your ideas for potential nominees for this achievement award. Prepare to advance a nominee for the January 2009 deadline. Review the process online. sscs.org/awards/Fieldawards.htm

The Career of Asad Abidi

Asad Abidi is an IEEE Fellow and a Member of the National Academy of Engineering. He received the 1997 IEEE Donald G. Fink Award, the 1997 ISSCC Jack Raper Outstanding Technology Directions Paper Award, and the IEEE Millennium Medal and was named a top-ten author by the ISSCC. The UCLA Henry Samueli School of Engineering and Applied Science recognized him in 2007 with the Lockheed-Martin Award for Excellence in Teaching.

Dr. Abidi obtained the BSc (Hon.) degree from Imperial College of Science & Technology, London, England in 1976, and the MS and PhD degrees from the University of California, Berkeley, in 1978 and 1981, all in Electrical Engineering.

He worked at Bell Laboratories, Murray Hill, NJ from 1982 to 1985, when much of the basic technology of submicron MOS VLSI was being developed there in the Advanced LSI Development Lab led by Marty Lepselter (inventor of the beam lead -- perhaps the first example of silicon micromachining), George Smith (co-inventor of the CCD), and Harry Boll (inventor of the standard cell and of the auto-refreshed dynamic RAM cell). As one of the few circuit designers in that lab, Abidi's task was to demonstrate the potential of the newly emerging submicron NMOS IC technology in high-speed communication circuits. This led to the first MOS amplifiers developed for Gb/s data rates in the then-important optical fiber receivers. Based on the belief that the speeds of simple MOSFETs would continue to scale upwards with shrinking dimensions, and that good circuits could be devised around the peculiar characteristics of these transistors, this work was carried out amidst much skepticism from proponents of GaAs and BJT ICs, the dominant technologies then for high-speed circuits. Years later, this experience would shape the genesis and development of RF-CMOS.

In 1985 Asad Abidi joined the Electrical Engineering faculty at the University of California, Los Angeles (UCLA). In 1989, he took a year leave as a Visiting Researcher at Hewlett-Packard Laboratories to investigate A/D conversion at ultrahigh speeds. At UCLA, Abidi and his students have researched analog signal chains for disk drive read channels, high-speed A/D conversion, and various analog CMOS circuits for signal processing and communications.

As mobile telephones entered widespread use in the mid 1990s and it became apparent that they would soon lead to an era of untethered computers networked with wireless devices, the research community identified many of the important hardware and software challenges ahead: low power circuits and systems to conserve battery life, miniaturization of antennas, the challenges of transmitting high data rates over unpredictable wireless channels, new networking algorithms, and so on. The RF circuits in the mobile telephones of those days comprised mainly discrete circuits with a mix of technologies. Abidi's research with his graduate students at UCLA was among the earliest to recognize how single-chip integration would bring about miniaturization, thus lowering power, and adding sophistication and adaptive functionality to radios in mobile devices. Furthermore, he was convinced that CMOS was the right technology for integrated radios. Practicing RF circuit designers of the time did not share this view.

The earliest research in RF-CMOS circuits, as they soon were labeled, proved that it was possible to build fully integrated amplifiers, mixers, oscillators, and filters with configurations devised to exploit the unique properties of MOSFETs that achieved performance levels only slightly inferior to the well-optimized discrete or semi-integrated circuits in the mainstream bipolar or GaAs technologies.

Had its role remained limited to a cheap replacement of legacy RF circuits, RF-CMOS would not have made much impact on industry. What drove Abidi's research at UCLA was his belief that the next generation of low power, adaptive, manufacturable radios could only be realized when RF and analog circuits were intimately embedded into digital circuits to tune their performance, correct their imperfections, adapt or control their characteristics, and otherwise unburden difficult analog signal processing. This is what had happened in wireline modems, the most sophisticated communication circuits of the day, and it was clear that only full CMOS realizations afforded the mixed-signal integration being sought.

Progress in RF-CMOS evolved along these lines. As circuit building blocks grew into integrated receivers and transmitters, the unique needs of integration led to new, or at least at that point not widely used, architectures such as zero IF receivers, constant-envelope transmitters based on fractional-N phase-locked loops, and so on. The newest generation of RF-CMOS circuits is so much shaped by digital paradigms that much of the analog portion of the receiver uses discrete-time multirate signal processing, while in the transmitter, which is today all-digital, analog waveforms appear only at the power amplifier's output that drives the antenna.

As a result of these advances in RF-CMOS, a new paradigm ---the software defined radio-- is taking practical form, bringing to a conclusion the long-standing quest for a universal radio device which tunes, or transmits, any channel carrying any modulated waveform in any radio band.

The radio transceivers for all wireless networking devices and for the new generation of mobile phones are mass produced today as RF-CMOS devices. These realizations are a far cry from the discrete component realizations of the 1990s; CMOS has enabled, and market forces have compelled, the integration of processors and memory on the same chip as the radio.

R. Jacob Baker Honored at FIE Conference in October

Dr. R. Jacob Baker was presented with the Hewlett-Packard Frederick Emmons Terman Award on 14 October at the meeting of the Frontiers in Education Conference in Milwaukee. The award, conferred by Wayne C. Johnson on behalf of the Electrical and Computer Engineering Division of the American Society for Engineering Education, lauds Dr. Baker as "*an outstanding young electrical engineering educator in recognition of his contribution to the profession.*"

Wayne C. Johnson, a Vice President of Hewlett Packard (right) presented Dr. R. Jacob Baker with a parchment certificate for this year's Frederick Emmons Terman Award.

Russel Jacob (Jake) Baker was born in Ogden, Utah, on October 5, 1964. He received his B.S. and M.S. degrees in electrical engineering from the University of Nevada, Las Vegas, and a Ph.D. degree in electrical engineering from the University of Nevada, Reno.

From 1981–1987, he was in the U.S. Marine Corps Reserves. From 1985–1993, he worked for E. G. & G. Energy Measurements and the Lawrence Livermore National Laboratory designing nuclear diagnostic instrumentation for underground nuclear weapons tests at the Nevada test site. During this time, he designed over 30 electronic and electro-optic instruments including high-speed (750 Mb/s) fiber-optic receiver/transmitters, PLLs, frame- and bit-syncs, data converters, streak-camera sweep circuits, micro-channel plate gating circuits, and analog oscilloscope electronics. From 1993–2000, he was a faculty member in the Department of Electrical Engineering at the University of Idaho. In 2000, he joined a new electrical and computer engineering program at Boise State University where he was Department Chair from 2004 to 2007. Also, since 1993, he has consulted for various companies and laboratories including Micron Technology, Amkor Wafer Fabrication Services, Tower Semiconductor, Rendition, Lawrence Berkeley Laboratory, and the Tower ASIC Design Center.

Dr. Baker holds over 200 granted or pending patents in integrated circuit design. He is a member of the electrical engineering honor society Eta Kappa Nu, a licensed Professional Engineer, and the author/coauthor of the books: *CMOS: Circuit Design, Layout, and Simulation, CMOS: Mixed-Signal Circuit Design,* and *DRAM Circuit Design: Fundamental and High-Speed Topics.* His research interests are in the areas of CMOS mixed-signal integrated circuit design and the design of memory in new and emerging fabrication technologies. He was also a co-recipient of the 2000 Prize Paper Award of the IEEE Power Electronics Society.

About the Terman Award

The Frederick Emmons Terman Award is presented annually to an outstanding young electrical engineering educator by the Electrical and Computer Engineering Division of theAmerican Society for Engineering Education. The Terman Award, established in 1969 by the Hewlett-Packard Company, consists of $5,000, an engraved gold-plated medal, a bronze replica of the medal mounted on a walnut plaque, and a parchment certificate. The recipient must be an electrical engineering educator who is less than 45 years old on June 1 of the year in which the award is presented and must be the principal author of an electrical engineering textbook published before June 1 of the year of his/her 40th birthday. The book must have been judged by his/her peers to be an outstanding original contribution to the field of electrical engineering. The recipient must also have displayed outstanding achievements in teaching, research, guidance of students, and other related activities.

About Frederick Emmons Terman

Frederick Emmons Terman received his A.B. degree in chemistry in 1920, the degree of Engineer in electrical engineering in 1922 from Stanford University, and his Sc.D. degree in electrical engineering in 1924 from Massachusetts Institute of Technology. From 1925–1965 he served as Instructor, then Professor of Electrical Engineering, Executive Head of Electrical Engineering Department, Dean of the School of Engineering, Provost, Vice-President, and, finally, as Acting President of Stanford University.

Among the many honors bestowed upon him were: the IEEE Medal of Honor; the first IEEE Education

Medal; the ASEE's Lamme Medal; the 1970 Herbert Hoover Medal for Distinguished Service to Stanford University; an honorary doctor's degree by Harvard; a decoration by the British government; the Presidential Medal for merit as a result of his war work; and the 1976 National Medal of Science from President Ford at a White House ceremony. Dr. Terman was a professor at Stanford University when William Hewlett and Dave Packard were engineering students there. It was under Dr. Terman's guidance in graduate work on radio engineering that Mr. Hewlett built the first tunable and automatically stabilized Weinbridge oscillator. Partially through Dr. Terman's urging, Hewlett and Packard set up their partnership in an old garage with $538 and the oscillator as their principal assets.

Dr. Terman died in December 1982. It is in appreciation of his accomplishments and guidance that Hewlett-Packard is proud to sponsor the Frederick Emmons Terman Award.

More information about the Frontiers in Education Conference may be obtained at http://fie.engrng.pitt.edu/fie2007/.

Van der Spiegel Acclaimed for Educational Innovation at IEEE EAB Meeting

Katherine Olstein, SSCS Administrator, k.olstein@ieee.org

SSCS Chapters Chair Jan Van der Spiegel of the University of Pennsylvania received the IEEE 2007 EAB Major Educational Innovation Award "for his efforts in promoting undergraduate research and creating robust opportunities for undergraduate students to enrich their education through integrative research experiences."

His nominator, IEEE Fellow Kenneth R. Laker said, "Professor Van der Spiegel is a highly accomplished scholar and educator in electrical engineering who has dedicated his career to successfully bridging research and teaching. He has won all of the University teaching awards for which he was eligible."

According to IEEE President Leah Jamison, education is a high IEEE priority. In her remarks at the EAB ceremony, she said, "In a recent "pulse" survey, a representative panel of IEEE members ranked "Growth and nurturing of the profession: encouraging educa-

Dr. Moshe Kahn, IEEE Educational Activities Vice President (left) and Dr. Bruce Eisenstein, Chair of the EAB Awards and Recognition Committee (right) presented Jan Van der Spiegel with the IEEE 2007 EAB Award for Educational Innovation in a ceremony at the IEEE Educational Activities Board Awards Dinner in Boston, MA on 16 November, 2007.

> **“Encouraging education and ensuring a pipeline of students to preserve the profession is the most important of our core values.”**
>
> ***Leah Jamison, IEEE President***

tion as a fundamental activity of engineers, scientists and technologists at all levels and at all times; ensuring a pipeline of students to preserve the profession” as the most important of our core values, with 92% agreement.”

When Dr. Van der Spiegel was Undergraduate Curriculum Chair in 1994 – 1997, he led the development of a new computer and telecommunications engineering (CTE) degree program that was one of the first to integrate computer engineering with telecommunications and networking. He also created one of the first FPGA-based digital systems courses for sophomore engineering, computer science, and telecommunications majors.

In 1986, Prof. Van der Spiegel established the Summer Undergraduate Fellowships in Sensor Technologies (SUNFEST) program at Penn and has been its director and champion ever since. Over the past ten years, nearly seventy percent of SUNFEST’s 190 students have gone on to graduate school. The program became a model for the National Science Foundation’s Research Experience for Undergraduates (REU) program, and has received continuous NSF funding since it began in 1987. The Penn Microfabrication Facility, directed by Dr. Van der Spiegel in the past, and the Center for Sensor Technologies directed by him today, contribute resources to SUNFEST students.

The ten-week SUNFEST experience provides students with an opportunity to work on an interdisciplinary research project under the guidance of a Penn faculty member and alongside other graduate students. In addition to doing research, the students participate in workshops on how to give effective presentations, write technical reports, and apply for graduate school. They also learn about ethics in engineering and science. The program makes a special effort to include students from colleges with little or no opportunity for undergraduate research activities, and also focuses on attracting students from groups underrepresented in research fields in engineering.

In addition to SUNFEST, Professor Van der Spiegel has brought undergraduates into his research projects though Penn’s capstone senior design course. Over the past ten years, he and his graduate students have mentored more than forty-three senior design projects, often advising three or more design teams in a given year. “As the instructor in charge of senior design, I know first hand how students working with Professor Van der Spiegel have developed and matured under his mentorship,” Dr. Laker said. “More than one-half of his senior design teams have won senior design awards at the Department and School of Engineering and Applied Science levels.”

Professor Van der Spiegel developed courses on Microelectronics and Emerging Technologies for Penn’s Executive Master’s in Technology Management weekend program, a blend of technology and business that is targeted to high technology managers. Since they have been in industry for at least five years and have backgrounds spanning all the engineering disciplines, EMTM courses are very different from those taught in other graduate programs. The “Emerging Technologies” course developed by Prof. Van der Spiegel is a lecture series introducing students to advancements that are expected to significantly impact industry. It is the only course in the program that EMTM students take every semester.

Professor Van der Spiegel’s commitment to and impact on engineering education has extended to campus life. As House Master of Ware College House from 1992-1998, he organized extracurricular activities that realized his goal of integrating engineering education into campus life in a manner that enriched both engineering and non-engineering students.

Prof. Van der Spiegel has been an active volunteer for the IEEE Solid-State Circuits Council/Society for more than 20 years and has served as Chapters Chair since the Society was formed ten years ago. During his tenure, the number of chapters has grown from one to more than 60. Chapters provide continuing professional education through guest seminars and short courses for members in their local areas. Professor Van der Spiegel has also served as Technical Program Chair of the International Solid-State Circuits Conference (ISSCC 2007), the world’s foremost conference on semiconductors, and is a Distinguished Lecturer of the Society.

> **“More than half of the 43 senior projects mentored by Prof. Van der Spiegel in the past decade won departmental design awards.”**
>
> ***Kenneth R. Laker***

Lanzerotti Applauded for Editorship of LEOS Newsletter

Mary Lanzerotti was presented with the IEEE/LEOS 2007 Distinguished Service Award for dedicated service as Editor of the LEOS Newsletter from 2001 through 2006 by Alan Willner, LEOS President. In a ceremony during the Society's Awards Banquet on 23 October in Lake Buena Vista, Florida, she received a plaque and an honorarium for work "resulting in outstanding changes to the publication." The LEOS Distinguished Service Award recognizes outstanding contributions by a Society member to the benefit of the group. For more information about LEOS see www.i-leo.org.

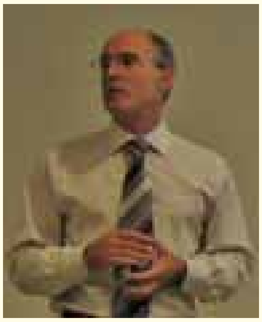
SSCS Distinguished Lecturers Visit Athens and Varna

A. N. Skodras, Hellenic Open University, School of Science & Technology
Patras, Greece (skodras@ieee.org)

A very successful and warm event was hosted by the IEEE SSCS Greece Chapter on 18 September, 2007 at the Central Library of the National Technical University of Athens. The idea, simple and effective, was to arrange for a combined visit of four Distinguished Lecturers (instead of one at a time) who would speak in a half-day special event. This idea, which was conceived by the SSCS Education Committee Chair, Dr C.K. Ken Yang, was named the "IEEE-SSCS DL Region 8 Tour" because the same distinguished lecturers would also visit neighboring Bulgaria during the same trip.

The invited speakers and their presentations were:

Prof. Takayasu Sakurai	University of Tokyo, Japan	•"Moore's Law Plus: What are Needed other than Scaling in Interconnects?" solving issues of IC's by 3D-stacking and large area integrated circuits based on organic transistors
Prof. Mircea R. Stan	University of Virginia	•"Power-aware and Temperature-aware Circuit Design" power-aware and temperature-aware circuit design techniques
Prof. Ian Galton	University of California, San Diego,	•Performance enhancement techniques for fractional-N PLLs
Prof. John R. Long	Delft University of Technology, the Netherlands	•"Wireless IC Building Blocks in CMOS/BiCMOS" wireless IC building blocks in CMOS/BiCMOS


Ian Galton


T. Sakurai


M. Stan


John Long

In view of the fact that national elections had forced many people to be out of the city, the caliber and diversity of the attendance was gratifying. For those who could not participate in person, the program was streamed to provide access online. Remote attendees could pose questions via email or skype to the Chapter Chair, Prof. A. Skodras. The event was reported in the third issue of the "THE CIRCUIT" www.upatras.gr/ieee/thecircuit.htm), a newsletter published quarterly in Greek and sent to all CAS/SSC members in Greece. The contributions of Prof. N. Hadjiargyriou and Prof. N. Koziris of the IEEE Greece Section were instrumental in organizing the tour.

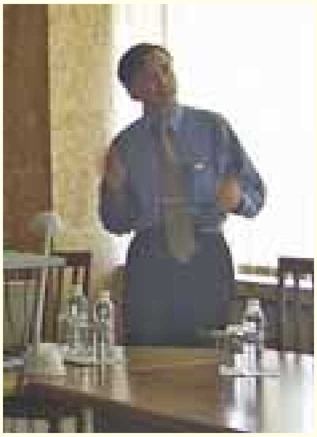
On the day before the program, the group visited the HTCI (Hellenic Technology Clusters Initiative) www.htci.gr), a new and dynamic effort that supports the creation of Innovative Technological Clusters aiming to make the companies that comprise them competitive in international markets. The first cluster focuses on the semiconductor, microelectronics, and embedded systems sector. Based in Maroussi (Athens) at the Microelectronics Innovation Centre, it constitutes a reference point for over twenty rapidly developing high technology companies, with more than 650 executives—mainly research and development engineers—nationwide.


At the Hellenic Technology Clusters Initiative (HTCI), from left: T. Chaniotakis, I. Tsiatouchas, V. Makios, I. Galton, J. Long, and M. Stan.

After the program, from left: M. Stan, A. Skodras (Chair, SSCS-Greece), T. Sakurai, I. Galton, and J. Long.

Jordan Kolev, SSCS Chapter Chair, Organizes DL Program at the Technical University of Varna


From left, J. Long, J. Kolev, T. Sakurai, I. Galton, M. Stan.


Takayasu Sakurai


Mircea Stan


In the foreground, M. Stan, J. Long, I. Galton.

Betty Prince Talks in Brazil

SSCS DL Betty Prince chatted with Carlo Requiao da Cunha, a faculty member at the Federal University of Santa Catarina in Florianopolis, after presenting a three-hour tutorial on "Embedded Non-Volatile Memories" at the Congresso Chip in Rio Conference on 5 September in Rio de Janiero. She also presented the conference plenary address on “Nanotechnology and Embedded Memories." The meeting, which is sponsored annually by the Brazilian Microelectronics Society, was held in conjunction with the 22nd Symposium on Microelectronics Technology and Devices (SBMICRO 2007) and the 20th Symposium on Integrated Circuits and Systems (SBCCI 2007) in 2007. These conferences comprise the most advanced forum for integrated circuits and systems in Brazil.

Congratulations New Senior Members

20 Elected in August and September

Bertan Bakkaloglu	Phoenix Section	Ravishanker Krishnamoorthy	Singapore Section
David Blaauw	Southeastern Michigan Section	Kent Lundberg	Boston Section
O Buhler	Denver Section	Adrian Maxim	Central Texas Section
David Chiang	Oregon Section	Paul Murtagh	Buenaventura Section
Carl Debono	Malta Section	Kevin On	Xian Section
Michael Fischer	Central Texas Section	John Rogers	Central Texas Section
Kyung Han	Santa Clara Valley Section	Robert Schuelke	Twin Cities Section
Teo Tee Hui	Singapore Section	Akio Ushida	Shikoku Section
Chung Chih Hung	Santa Clara Valley Section	Fu-Cheng Wang	Orange County Section
Wern Ming Koe	Dallas Section	Yuan Xie	Central Pennsylvania Section

Call for Fellow Nominations

Nominations are being accepted until March 1, 2008 for the 2009 class of IEEE Fellows.

IEEE Fellows are an elite group from around the globe. The IEEE looks to the Fellows for guidance and leadership as the world of electrical and electronic technology continues to evolve. The accomplishments that are being honored should have contributed importantly to the advancement or application of engineering, science and technology, bringing significant value to society.

Revisions to the IEEE Fellow nomination process have taken place over the past few years, mainly in an effort to generate more Fellow nominations from industry. Fellow nominees are now classified as Research Engineer/Scientist, Application Engineer/Practitioner, Technical Leader, or Educator.

Candidates for Fellow must hold Senior Member grade at the time the nomination is submitted and shall have been an IEEE member in good standing (in any grade) for a period of five years or more preceding January 1 of the year of election.

Any person, including a non-member, is eligible to be an IEEE Fellow nominator with a few exceptions. The Steps, responsibilities and forms are online at www.ieee.org/web/membership/fellows/fellow_steps.html

Nominations, references and endorsements may be submitted electronically.

TOOLS:
How to Write Readable Reports and Winning Proposals

Part 5: Persuasive External Proposals

Peter and Cheryl Reimold, www.allaboutcomunication.com

Writing a formal proposal for an external customer can be a daunting task that sends people scrambling for help. In particular, standard formats and canned sections seem to offer safety.

Unfortunately, these safe approaches are almost guaranteed not to work because they violate the core requirement of a persuasive proposal: a precise fit between benefits offered and perceived needs of the customer. Since each customer's situation is special, no all-purpose strategy can be effective. Instead, you need an individual approach.

Two Keys to a Winning Proposal

What are the things that really work with proposal readers? Here are the two that come up most often:

- An executive summary that states the benefits of your solution strongly and ties them clearly to the customer's needs
- A proposal body that backs up the claims of the executive summary crisply and without techno-babble

Your first step is to study the customer's needs as expressed in the request for proposal, if there is one. (Otherwise, do your own thorough research on the customer's situation.) People usually spend too little time on this stage of proposal preparation; instead, they waste it on writing up a lot of irrelevant detail in hyper-technical language.

Next, identify the solutions you can offer for the customer's needs and describe them in a trial executive summary. Then use that summary as your guide in developing the rest of the proposal.

Typically, components include transmittal letter, executive summary, background and overview, technical, objectives, work plan, related experience, key personnel, facilities and equipment, schedule, cost or budget, and conclusion. However, the actual titles and order must carefully follow any guidelines laid out in the request for proposal.

Four Temptations to Resist

What makes writers spend a great deal of time, only to produce unfocused, overdetailed proposals? We have observed four common reasons:

1. Getting overwhelmed by the demands of format. People fear proposals must be very formal and technically impressive. In truth, they just need to be persuasive—with no more technical detail than appropriate for the readers. In particular, remember that the front sections and conclusion are read by everybody on the evaluation team, so keep them brief and nontechnical. Reserve intricacies for the sections specifically labeled as technical.

2. Writing detail sections before formulating your main message in the summary. Beginning with the executive summary offers tremendous benefits, especially if the writing is a team effort. It focuses all details on key selling points. From the outset your document will be leaner and more relevant, and you'll have less cutting and editing to do.

3. Falling into features thinking. Especially if you have not managed to fit your benefits to the customer's needs, you may be tempted to switch to a features-based approach to unload all your selling points. Go back to the beginning: Identify the key needs and work out the winning strategy to fill them.

4. Giving in to plain laziness. Pulling standard components off the shelf and slapping them together for a proposal, after changing a few names and other incidentals, seems so much faster and easier. It is—but what good does it do? You might as well not write a proposal at all; that would be even easier and faster, and would get the same result! As we said, proposals inherently must be tailored to the special needs of the customer. Those needs aren't sitting around on your shelf.

Cheryl and Peter Reimold have been teaching communication skills to engineers, scientists, and businesspeople for 20 years. Their firm, PERC Communications (+1 914 725 1024, perccom@aol.com), offers businesses consulting and writing services, as well as customized inhouse courses on writing, presentation skills, and on-the-job communication skills. Visit their Web site at http://www.allaboutcommunication.com.

This article is gratefully reprinted with permission from the authors as well as with permission from the IEEE Professional Communication Society Newsletter Editor. This article is reprinted from the January/February 2003 issue, Volume 47, Number 1, page 8 of the IEEE PCS Newsletter.

ISSCC 2008 to Focus on System Integration for Life and Style

SSCS Flagship Conference to Meet on February 3-7 in San Francisco

Bill Bowhill, Intel Corporation, ISSCC Program Vice Chair, bill.bowhill@intel.com

As semiconductor technology continues its advance into the nanometer domain, the range of electronic systems is broadening from enormous processing and storage in computing to micropower and wireless mobile functions.

Design and system integration must master all levels of today's technology jigsaw puzzle to enable the new and exciting systems which alter our lives and lifestyles in endless ways:

Ultra-low-power-sensor and wireless techniques that deliver new tools for advances in medical and life sciences; entertainment and computing functions that merge on the desktop; mobile phones that host a whole range of functions such as on-line information, finance, security and audio/video entertainment.

The integration of these advances into sophisticated systems allows more processing to fit into tinier packages and brings power consumption down to the point that everything can be battery powered in a hand-held device. However, the huge opportunities of nanometre technology also present daunting challenges: Designers must manage both vast complexity in the digital domain and the realization of high-performance analog, RF and interface functions with complex device behavior and low-voltage supplies.

ISSCC 2008 will feature presentations that demonstrate ways in which the integration of novel circuit and systems can deliver functions that enrich the users' life and style.

Plenary Session

- *Hyung Kyu Lim* from the Samsung Advanced Institute of Technology will discuss "The 2nd Wave of the Digital Consumer Revolution: Challenges and Opportunities." The rapid advancement of wireless communication and mobile Internet combined with advances in user interfaces and input device technologies are changing the way people interact. Examples include online social networking, nomadic lifestyles that burst the boundaries between work and personal life, and remote medical services such as on-the-spot diagnosis and emergency paging.

- New human interface technologies are changing the way people interact with each other and with the virtual computing network. *Bill Buxton* from Microsoft Research will discuss surface computing using interactive display technologies. The talk is entitled "Surface and Tangible Computing, and the 'Small' Matter of People and Design." The rapid evolution of electronic technologies, integration techniques, and fabrication processes has spurred the development of a wide range of new interactive products. The presentation will examine the evolution of large surface-type computing devices and small graspable computational objects and demonstrate that these two extremes of the computational spectrum can meet in a seamless integrated experience.

- Advanced CMOS technologies and ultra-lower power design are enabling integration of significant computational power into small form factors. *Mike Muller* from ARM will discuss "Embedded Processing: At the Heart of Life and Style". As the largest supplier of processor IP to SoC developers, ARM has a unique perspective on the problems of performance, cost, and power for mobile products in nanometer CMOS -- a technology that allows great improvements and more functions for each chip. Nevertheless, power is an increasing problem: While power consumption in the active state increases with the number and speed of the gates, standby power gets worse due to leakier transistors. This presentation will explore how IC system developers may address this problem by the betterment of circuit cells, power optimization, and processor architecture, and by better synergy between hardware and software.

- The final plenary talk discusses the future of computing. "Why Can't A Computer Be More Like A Brain? Or What To Do With All Those Transistors?" will be presented by *Jeff Hawkins* from Numenta. The age of intelligent machines may be on the horizon. If so, there will be many opportunities to rethink how integrated circuits may play a leading role. The brain's physical structure, like that of the modern microprocessor, constrains how information is stored. To build machines which approach human-transaction throughput rates, data will need to be organized in hierarchical memory structures. Hierarchical Temporal Memory (HTM) is a new theory based on the behavior of the human neocortex that provides a framework for building models that can be executed on conventional computers to dramatically advance artificial intelligence hosted in high-performance computer platforms.

Regular Paper Sessions

The world's semiconductor industry and research institutions continue on a fast path of innovation and improved device performance. Following the Plenary Session, 237 technical papers will be presented in 31 sessions over 2 $^1/_2$ days. They highlight the latest advancement in circuit design and technology. Novel designs to be presented include:

- 6 data converters in 65nm and the first in 45nm. A low-voltage ADC for a sensor application operates down to 200mV supply.
- High-performance processors demonstrating improvements in both single- and multi-threaded performance.
- The highest level of processor integration ever reported (2 billion transistors).
- Micro-architecture and circuit innovations reduce power consumption of an x86 processor by 5x.
- A single-chip eye tracker provides extremely high-frame-rate and fast processing for tracking eye movements in real time.
- A 45nm 3.5G baseband and multimedia-application-processor SoC extends the features and services of next-generation mobile phones.
- Memories: Fastest embedded DRAM macro in bulk CMOS; First GDDR5 DRAM (with quadruple data-rate) developed; First high-volume functional 153Mb SRAM chip in 45nm high-κ metal-gate technology; First-reported NAND-Flash memory with three-dimensional silicon integration in 45nm lithography.
- 60GHz integrated frequency-tripler with quadrature outputs in 90nm CMOS.
- An op-amp with a 0.33μV offset independent of temperature using a single room-temperature calibration.
- A wireless sensor-node SoC for smart bandaids is used for vital-sign monitoring in body-area network applications.
- The smallest Nuclear-Magnetic-Resonance (NMR) system (2500cm^3) is used for detection of bio-molecules.
- The first imager (1.1x1.5 mm^2) implanted into a human eye, partially restoring vision to a blind patient.
- The first fully-integrated 14-band MB-OFDM UWB transceiver.
- The first dual-band MIMO CMOS radio SoC for 802.11n wireless LAN.
- A 40Gb/s CMOS serial-link Receiver with adaptive equalization and CDR.

Educational Events: Tutorials

The Conference will also include many educational events: Ten independent tutorials will be presented (Sunday, February 3rd) by experts from each of the ISSCC 2008 Technical Program Subcommittees: Analog; Data Converters; High-Performance Digital; Imagers, MEMS, Medical and Displays; Low-Power Digital; Memory; RF Technology Directions; Wireless; and Wireline:

- T1: Fundamentals of Class-D Amplifier Operation & Design
- T2: Pipelined A/D Converters: The Basics
- T3: CMOS Temperature Sensors
- T4: SoC Power-Reduction Techniques
- T5: Digital Phase-Locked Loops
- T6: Leakage-Reduction Techniques
- T7: NAND Memories for SSD
- T8: Silicon mm-Wave Circuits
- T9: CMOS+ Bio: The Silicon that Moves and Feels Small Living Things
- T10: Basics of High-Speed Chip-to-Chip and Backplane Signaling

Short Course: "Embedded Power Management for IC Designers"

This year's short course (Thursday, February 7th) will explain the fundamental power management issues faced by IC designers and explore state-of-the-art circuit- and system-level techniques for power management. The four 90-minute presentations, intended for both entry-level and experienced engineers will be:

SC1: Navigating the Path to a Successful IC Switching Regulator Design
SC2: Circuit Techniques for Switching Regulators
SC3: Power Reduction and Management Techniques for Digital Circuits
SC4: Power/Energy for Autonomous and Ultra-Portable Devices

While new generations of consumer electronic products consume less power than their predecessors, the requirements for power delivery keep changing in the direction of lower voltage and higher current. At the same time, market pressures dictate that every new generation of a product provides increased functionality at reduced cost: and emerging applications such as RF ID tags and sensor networks require elimination of conventional power sources altogether.

These trends have caused power management to be a critical issue in modern IC design. The switching regulators predominantly used for DC power conversion in battery-operated devices introduce switching noise as the current they supply is increased, whereas analog and mixed-signal circuits that use the power become increasingly sensitive to such noise as their supply voltages are decreased. Increasingly, multiple voltage domains, each with different load scenarios, must be supported. Moreover, cost minimization often requires that as much of the power management circuitry as possible to be implemented in a highly scaled CMOS technology optimized for digital circuitry. Thus, techniques to convert and use power efficiently are essential for success.

Advanced-Circuit-Design Forums

7 Advanced Circuit Design Forums will be held during the conference. They provide an informal all-day interaction in which circuit experts exchange information on their current research. The Forum topics this year are as follows

F1: Embedded Memory Design for Nanoscale VLSI Systems
F2: Wide-Dynamic-Range Imaging
F3: Architectures and Circuit Techniques for Nanoscale RF CMOS
F4: Power Systems from the Gigawatt to the Microwatt – Generation, Distribution, Storage and Efficient Use of Energy
F5: Future of High-Speed Transceivers

F6: Transistor Variability in Nanometer-Scale Technologies
F7: Digitally Assisted Analog and RF Circuits

The evening program provides seven Special Evening Topic Sessions (SETs), in which experts provide insight and background on a subject of current importance and two panel discussions in which experts debate a selected topic and field audience questions in a semiformal atmosphere. The SET sessions cover a diverse range of topics this year including: Environmental impacts and opportunities of semiconductors; the challenges associated with designing sensors used in life-critical applications; and the highlights of IEDM 2007.

The two panels will debate the role of private equity firms in the IC industry; the limits of multi-core integration for general-purpose processors and whether it is better to integrate many simple cores or fewer complex cores.

The full program is as follows:

Special Topic Sessions
SE1: Green Electronics: Environmental Impacts, Power, E-Waste
SE2: MEMS for Frequency Synthesis and Wireless RF Communications (or Life without Quartz Crystal)
SE3: From Silicon to Aether and Back
SE4: Unusual Data-Converter Techniques
SE5: Trusting Our Lives to Sensors
SE6: Highlights of IEDM 2007
SE7: Trends and Challenges in Optical Communications Front-End

Panels:
E1: Private Equity: Fight them or Invite them
E2: Can Multicore Integration Justify the Increased Cost of Process Scaling?

More information about ISSCC 2008 may be found at: www.isscc.org/isscc/.

Invitation from the ISSCC 2008 Technical Program Chair

I would like to invite you to attend the 55th ISSCC, which will be held in San Francisco on February 3-7, 2008. The conference theme is “System Integration for Life and Style” in recognition that integration of novel circuits and systems can deliver functions that enrich the users’ life style.

There will be 237 papers distributed over 31 technical sessions covering advances in analog and digital circuits; data converters; imagers, medical and displays; MEMS; memories; RF building blocks; technology directions, and wireless and wireline communications.

Beside the regular paper sessions, the ISSCC will offer a wide variety of high-quality educational programs, adding to the already significant value of the ISSCC. This year, there are ten Tutorials, seven Advanced Circuit Design Forums, and one Short Course. This year's short course deals with the popular topic of “Embedded Power Management for IC Designers.”

There are also four plenary presentations.

- “The 2nd Wave of Digital Consumer Revolution: Challenges and Opportunities,”
  Hyung Kyu Lim (Samsung Advanced Institute of Technology)
- “Surface and Tangible Computing, and the ‘Small’ Matter of People and Design,”
  Bill Buxton (Microsoft Research)
- “Embedded Processing: At the Heart of Life and Style,”
  Mike Muller (ARM)
- “Can’t A Computer Be More Like A Brain? Or What To Do With All Those Transistors?,”
  Jeff Hawkins (Numenta)

In addition, Evening Sessions will include: Two panels that will bring together experts and visionaries who share their views. Moreover, seven special-topic sessions will provide an opportunity to learn about an emerging topic in a relaxed setting.

As you can see, the upcoming ISSCC continues its tradition of presenting the best in solid-state circuits and providing an opportunity to learn about the latest developments through its rich choice of educational activities. In addition, the ISSCC is a great avenue for networking, meeting old colleagues and making new friends. I am sure you'll enjoy ISSCC and I hope to be able to welcome you in San Francisco.

Yoshiaki Hagihara
ISSCC 2008 Technical Program Chair
yoshi@isscc.net

VLSI-TSA and VLSI-DAT to Convene on 21-25 April in Hsinchu, Taiwan

15th International Symposium on VLSI Technology, Systems, and Applications & 4th VLSI Design, Automation and Test

Clara Wu, Symposia Secretariat, clara@itri.org.tw

The 2008 International Symposium on VLSI Technology, Systems, and Applications (VLSI-TSA) and the 2008 International Symposium on VLSI Design, Automation and Test (VLSI-DAT) will be held from April 21 to 25, 2008 at the Ambassador Hotel in Hsinchu, Taiwan. Sponsored by the Industrial Technology Research Institute (ITRI) and divided into separate annual symposia since 2005, VLSI TSA-DAT lasts for two and a half days in the same week, with a one day overlap.

The aim of the joint conference is to bring together scientists and engineers actively engaged in research, development, and manufacturing on VLSI technology, systems, and applications and on VLSI design, automation and test to discuss current progress in this field.

In 2008, each symposium will feature three keynote speakers:

VLSI Technology, Systems, and Applications

Dr. Reinhard Ploss	Trends in Electronics and Semiconductors for Automotive Applications Infineon, Germany
Dr. Clark T. C Nguyen	Integrated Micromechanical Radio Front-Ends UC Berkeley, USA
Dr. Kinam Kim	Future Memory Technology Challenges and Opportunities Samsung, Korea

VLSI Design, Automation, and Test

Dr. Willy Sansen	Efficient Analog Signal processing in nm CMOS Technologies K.U Leuven, Belgium
Dr. Randal E. Bryant	Reasoning about Data: Bits, Bit Vectors, or Words Carnegie Mellon University, USA
Dr. Janusz Rajski	Logic Diagnosis, Yield Learning and Quality of Test Mentor Graphics, USA


Dr. Reinhard Ploss


Dr. Clark T. C Nguyen


Dr. Kinam Kim


Dr. Willy Sansen


Dr. Randal E. Bryant


Dr. Janusz Rajski

VLSI-TSA will also include fifty juried papers; three tutorials; two special sessions on Post-CMOS and High Voltage Device & Process; a short course on "DRAM and new Channel Material vs. New Devices Structure," and invited talks on FEOL, NVM, BEOL, CMOS integration, Characterization & Modeling, 3D & packaging, CMOS devices and DRAM.

Please register at vlsitsa.itri.org.tw or http://vlsidat.itri.org.tw. Should you have questions, please contact conference registrar, Ms. Yvonne Chen at +886-3-5913003 or email to HRD@itri.org.tw for assistance.

Mm-wave CMOS Applications: A Report from a CSICS Panel

Anne O'Neill SSCS Executive Director, a.oneill@ieee.org

How long will GaAs and SiGe continue as the mainstream technology for hi frequency applications? The Compound Semi-Conductor IC Symposium (CSICS) experts are one group very interested to hear the prognosis for future applications and the feasibility of 60 GHz WLAN/WPAN in CMOS. And the questions at the panel discussion during the November 29th Program in Portland Oregon, showed their attention.

Millimeter wave IC products are not around the corner but here. Gabriel Rebeiz from UCSD reminded the audience that an automotive radar chip described by Ian Gresham at the Microwave Symposium in June 2006 is now in production. General Motors is counting on M/A-COM shipments of 1M units per year (rate of 100K units per month) to occur at the end of 2008. The primary problems still on their way to a better solution are a commodity package and appropriate low-cost high-volume testing. Currently QFN packages designed for 5GHZ operation are being used simply because they are available in quantity although they are much too big and introduce too much inductance. So packaging and testing are two business challenges for this BiCMOS application.

Although these mm wave products are Si-Ge and operate at 24 GHZ, the future of 60 GHz CMOS production is closer. Joy Laskar reported that Georgia Tech has demonstrated a 60 GHz transceiver and beam-former that is not a MIMIC combining some portion of III-V on a separate substrate, but a true IC. It is a scaled phased array on a single chip that includes an LNA, mixer chain. It is RF-in and bit-out and hot pluggable into existing back-ends.

Key to driving advances will be the communication standards that are almost agreed upon. Nishikawa of NTT listed ECMA technical committees still in discussion and 802.15.3c which is in voting now. Mahbod Eyvazkhani of Nokia got the audience to laugh by talking about consumer interest to transfer movies to their cell phones. But all the panelists admitted that high definition video and high bit rate data transfer will provide the high volume demand that will make investing in this technology worthwhile.

However Nishikawa of NTT showed a chart indicating that unit costs will drop below $10 a chip only when the volume is greater that a million chips a month. He doubted that new LAN standards alone would be enough to make this product type a going business line. Jonghae Kim of IBM SRDC simply said that a lot more data on production runs, process variation and yield will be needed before such answers are known. Initial costs for CMOS will cost considerably more than pHEMT solutions.

Ali Niknijad of UC-Berkeley ticked off other applications that would benefit from 60 GHZ CMOS technology for data transfer, HD set-top boxes, high density DVDs. And HD displays. "Just moving memory around will do it," he said about applications driving the technology. After posting about 15 specifications, Niknijad distilled the transceiver to the sweet spot of 10 dBm Pout and less that 10 dB for a noise factor. This is achievable he assured the audience. Flash will be the first memory to handle the 60 GHz transmission he asserted. And 802.11 applications will probably move UWB aside.

A challenge for the circuit designer of 60 GHz IC applications, is solving issues about the antenna. Currently on-chip antenna design can take up a lot of valuable real estate when integrated on a CMOS chip with other logic. Some panelists advised to shrink the design and not use transmision-line, making the design more RFIC like, not MMIC like. Niknijad pointed audience attention to a patented bond wire antenna in use, that works at 60 GHz.

Joy Laskar from Georgia Tech where a lot of research has been done on packaging, pointed out that it is preferable to have a single RF input and to use a different architecture chain that C-Band. Switch beam will use less real estate than beam forming but those switch designs are a topic for another session.

Then panel closed with one last audience question that contrasted optimal designs with the business reality. Why not W band that has less path loss and greater bandwidth than 60 Hz? Answer: There are no standards being written for W band.

SSCS-Germany Cosponsors SAMOS 2007

Conference Founder Stamatis Vassiliadis Memorialized

Embedded Computer Systems: Architectures, Modeling, and Simulation

Holger Blume, Program Chairman IC-SAMOS 2007, Chairman IEEE SSCS Germany Chapter, blume@eecs.rwth-aachen.de

Prof. Stamatis Vassiliadis

Prof. Stamatis Vassiliadis (IEEE Fellow, ACM Fellow, Member of the Dutch Academy of Sciences, and Professor at Delft University of Technology), who passed away on 7 April, 2007 was memorialized at the 2007 SAMOS VII conference. This year's Embedded Computer Systems: Architectures, Modeling and Simulation symposium took place on the Greek island of Samos, from 16-19 July.

Born in Manolates, Samos, Stamatis founded the SAMOS conference and workshop series in 2000 and was the head and the heart of these events until his death. The series will not be the same without him. In a short presentation about Stamatis's life, SAMOS board member John Glossner recognized him as an outstanding computer scientist and a good friend to all of us due to his vivid and hearty manner.

In order to create a permanent commemoration of this inspiring scientist and to preserve his special spirit, the SAMOS organizing committee established the "Stamatis Vassiliadis Best Paper Awards." The IC-SAMOS Award and the SAMOS Workshop Award were given for the first time to:

• "Systematic Data Structure Exploration of Multimedia and Network Applications realized Embedded Systems" IC-SAMOS Award	Lazaros Papadopoulos Christos Baloukas Nikolaos Zompakis Dimitrios Soudris (Democritus University Thrace, Xanthi, Greece)
• "The Next Generation Challenge for Software Defined Radio" Workshop Award	Mark Woh Sangwon Seo Hyunseok Lee Yuan Lin, Scott Mahlke Trevor Mudge (University of Michigan Ann Arbor, USA) Chaitali Chakrabarti , (Arizona State University, USA); Krisztian Flautner (ARM Ltd. UK)

This year's program focused on SAMOS' traditional areas of interest: embedded systems and embedded architectures. Session topics included processor architectures, design space exploration, multiprocessor architectures, VLSI architectures, systems and applications and reconfigurable architectures. Special sessions were devoted to SoC architectures for software defined radio and embedded sensor systems and sensor networks.

Highlights were invited talks by Willie Anderson (VP Engineering for Qualcomm CDMATechnologies) on "Software Is The Answer but What Is The Question?" and by John Glossner (CTO and EVP for Sandbridge Technologies) on "The Sandblaster SB3011 Processor." Both presentations inspired lively discussions among conference participants.

SAMOS '2007 symposium board and program chairs (from left): John Glossner (Sandbridge Technologies, USA), Jarmo Takala (Tampere University of Technology, Finland), Mladen Berekovic (IMEC, Belgium), Holger Blume (RWTH Aachen University, Germany), Andy Pimentel (Univ. of Amsterdam, The Netherlands), and Georgij Gaydadijev (TU Delft, The Netherlands); missing from this photograph: Shuvra Bhattacharyya (Univ. of Maryland, USA).

The two co-located SAMOS events -- the International SAMOS Conference (IC-SAMOS), sponsored and co-organized by the Germany Chapter of the IEEE Solid-State Circuits Society and the IEEE Circuits and Systems Society, and the SAMOS workshop -- attracted an increasing number of paper submissions compared to 2006 (207 from 30 countries, a 40% increase). Due to their high quality, the selection process was very competitive, entailing four reviews per paper. The overall acceptance rate was less than 30 % for the conference and less than 40 % for the workshop. Traditionally, the symposium features presentations in the morning, while in-depth, formal discussions on research results and future directions take place in an informal setting after lunch. The best papers of the conference are published in special issues of the Journal of VLSI Signal processing and the Journal of Systems Architecture. Proceedings of the SAMOS workshop have been published in the Springer LNCS series.

SAMOS VIII will take place in 2008 from July 21 - 24. For more information visit: samos.et.tudelft.nl/samos_viii/

See you in Samos next year!

Sakurai and Razavi Visit SSCS-Seoul in July and August

SSCS DL Takayasu Sakurai of Tokyo University spoke on "Organic Integrated Circuit Design for Ubiquitous Electronics" at Ewha Womans University on 6 July, 2007. According to Assistant Professor Sung Min Park, "Almost fifty percent of the faculty members of the EE Department of Ewha Womans University specialize in semiconductors, IC design, SoC design, and the like. So Prof. Sakurai's talk was very much related to our interests."

Precis: The other extreme of the silicon VLSI's which stay as small as a centimeter square, a new domain of electronics called large-area integrated circuit as large as meters is waiting, which may open up a new continent of applications in the era of ubiquitous electronics. One of the implementations of large-area electronics is based on organic transistors. This talk provides perspectives on organic circuit design taking E-skin, sheet-type scanner, Braille display and wireless transmission sheet as examples.


Dr. Takayasu Sakurai (front row, fourth from left) addressed 35 students at Ewha Womans University in Seoul, Korea on 6 July, 2007. At his right is Prof. Sung Min Park; at his left are Prof. Shin-Il Lim (in back), Prof. Kwang-sup Yoon, and Prof. Nak-Myeong Kim and Prof. Hyesook Lim (in back). Professors Park, H. Lim and N. Kim are Ewha University faculty.

Prof. Behzad Razavi presented a lecture entitled "60-GHz Transceivers in CMOS : Why and How ?" on 14 August at Korea University, which houses a center for 60GHz wireless transceivers.

Precis: The 7-GHz unlicensed band around 60 GHz offers the possibility of wireless communication at data rates reaching several gigabits per second. Moreover, the short wavelength allows integration of the antenna on-chip and opens prospects for beam forming and MIMO signaling.

With multiple antennas and transceivers operating on one chip, and with the enormous analog and digital signal processing required for high-rate communications, the use of CMOS technology becomes attractive and perhaps essential.

This talk presents the challenges in circuit and architecture design for 60-GHz CMOS transceivers and describes our recent work on receiver design for this frequency band. Specifically, a heterodyne receiver is presented that achieves a noise figure of 6.9-8.3 dB with a power dissipation of 80 mW in 90-nm CMOS technology.


Dr. Behzad Razavi addressed an audience of 80 at Korea University in Seoul on 14 August, 2007. From Left (first row): Prof. Jae-Sung Rieh, Prof. Chulwoo Kim, Prof. Yogendera Kumar, Prof. B. Razavi, and Prof. Andy Chung.

18th VLSI Design/CAD Symposium Cosponsored by IEEE Taipei and Tainan Sections

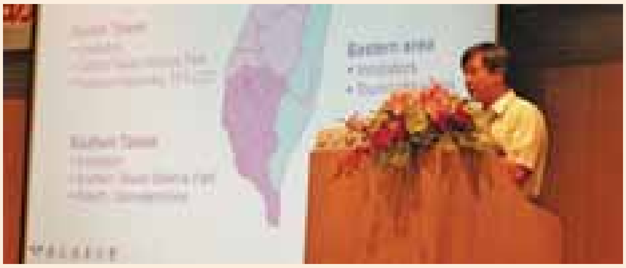
Annual Meeting of IEEE SSCS and CAS in August

Chua-Chin Wang, Chapter Chair SSCS-Tainan, ccwang@ee.sysu.edu.tw

The 18th VLSI/CAD Symposium was held on 8-10 August, 2007 in Hualien, Taiwan. Home to semiconductor foundries such as TSMC and UMC, Taiwan is renowned as an IC design power house. The VLSI Design/CAD Symposium, which plays an important role in stimulating local research, is aimed at providing an open forum for professors, industrial engineers and, most important of all, graduate students to exchange cutting-edge RD knowledge and ideas in the fields of SOC/ASIC design and EDA research


General Chair Prof. Chua-Chin Wang of National Sun Yat-Sen University greeting attendees at the 2007 (18th) VLSI Design/CAD Symposium on 8 August, 2007.

Prof. Chung-Yu Wu, President of National Chiao Tung University, gave a keynote speech entitled "What Happens Next? When Engineering Falls in Love with Biology, Medical Science, and Life Science," describing the cutting-edge chip design developed by his research team.



A second keynote speech, "Sustainable Development and Hi-Tech Industries," by Prof. Jyuo-Min Shyu, Dean of the College of EE and CS, National Tsing Hwa University, ignited a discussion about the need for a long term development plan for Taiwan and the worldwide IC industry.

In a talk on "Design for Reliability and Robustness - Coping with Increasing Variability and Reliability Concerns," Prof. Kwang-Ting Tim Cheng of UC Santa Barbara pointed out the rising cost of DFT and DFM in the next decade.

Prof. Shey-Shi Lu of National Taiwan University described the latest SoC solutions for nodes used in a wireless sensor network – - the next biomedical and electronic interdiscipline research topic -- in "A SoC for Biomedical Wireless Sensor Network."

Other highpoints of the symposium were

- a panel discussion on the national SOC project of Taiwan entitled "NSoC : Naïve or Novel Soc?" hosted by Prof. Chau-Chin Su;
- three "Live Demo" sessions, where SOC systems were physically presented on chips or boards by speakers from brand-name Korean IC design companies including RDC, Sunplus, Faraday, and Andes, and medalists of national IC/IP design contests. The entire ballroom was packed during the all the sessions;
- fifteen oral sessions with 90 papers, and three poster sessions with 88.

SSCS Chapter Chairs Shen-luan Liu (Tapei) and C. – C. Wang (Tainan) hosted the annual joint meeting of SSCS members. Prof. C. K. Wang, SSCS Region 10 Representative (seated in front at left) spoke about SSCS local and worldwide activities.

"Among the social activities organized for the conference, my favorite was the magic show (left) and the gourmet seafood at the banquet. All the attendees were so impressed, they kept saying that the symposium should do this more often."
C.C. Wang

Details about the symposium program and organization team can be found in www.ee.nsysu.edu.tw/vlsi2007/.

Murmann and Razavi Visit SSCS-Taipei

SSCS Extra Chapter Subsidy Underwrites Short Course on A/D Converter Design

By IEEE SSCS Taipei Chapter

In light of the importance of digitally-assisted approaches to analog design, SSCS-Taipei invited Prof. Boris Murmann of the Department of Electrical Engineering, Stanford University to present a short course on the topic of deep-submicron ADC. Entitled "Challenges and Solutions for A/D Converter Design in Deep Submicron CMOS" and funded by an extra chapter subsidy from the Society, it took place in Hsinchu and Taipei on 5-6 September, respectively, and attracted over one hundred attendees, in almost equal proportions from industry and academia.

Two weeks later, SSCS Distinguished Lecturer, Prof. Behzad Razavi of UCLA presented an invited talk on millimeter-wave circuit design at National Taiwan University (NTU), Taipei. Hosted by the Director of the Graduate Institute of Electronics Engineering, Prof. Shey-Shi Lu, Dr. Razavi's one-hour lecture, entitled "A Millimeter-Wave Circuit Technique," attracted an audience of approximately 200 on 19 September.

Murmann Describes Design Methodology for Devices Not Obeying Square Law

Deep submicron CMOS technologies have brought many benefits to digital designs, but have also introduced harsh challenges for analog designers: The simple square-law model can no longer predict deep submicron transistor behaviors. Thus, a paradigm shift has occurred to take advantage of the cheap and powerful digital capability to compensate for non-ideal analog circuits in deep submicron processes.

Focusing on amplifier design with deep submicron devices, Prof. Murmann introduced his course with a systematic circuit design approach for devices that do not obey square law. He described the design methodology in detail and showed several case studies. In the second part of his lecture, he dove into ADC design, introducing several figure-of-merit definitions for evaluating ADC performance and discussing the fundamental limits. Then he presented digitally-assisted ADC design, including illustrations of several examples bringing a mix of theoretical and practical design knowledge to the lecture.

Razavi Introduces Inductive Peaking Technique

For millimeter-wave/RF circuits, deep submicron CMOS technologies have enabled higher operating frequency. However, some limitations still pose great challenges for circuit designers. In his presentation, Prof. Razavi introduced an inductive peaking technique that allows operation near the self resonance frequency of inductors. Using the proposed technique, fundamental oscillators operating at 130 GHz and frequency dividers achieving a maximum frequency of 125 GHz have been demonstrated. The prototypes have been fabricated in TSMC's 90-nm CMOS technology.

Prof. Razavi is an award-winning researcher, teacher, and author. He joined UCLA in 1996, where he has pursued research on high-speed analog circuits, RF and wireless design, phase-locking phenomena, and data converter design. He was recognized as one of the top 10 authors in the 50-year history of ISSCC. Prof. Razavi has authored five textbooks on analog and RF design and edited two on phase-locked systems.

Prof. Boris Murmann presented a short course on ADC Converter Design to an audience of 75 at National Chaio-Tung University in Hsinchu, Taiwan on 5 September.

Thirty-five attended Prof. Murmann's ADC Converter Design course on 6 September at National Taiwan University, Taipei.

Behzad Razavi addressed an audience of 200 on 19 September at National Taiwan University (NTU) on "A Millimeter-Wave Circuit Technique."

230 Papers Represent International Community at ASICON 2007 in Guilin, China

7th International ASIC Conference Organized by SSCS-Shanghai and Fudan University

Ting-Ao Tang, Chair, SSCS-Shanghai, tatang@fudan.edu.cn

ASICON is one of the most important international conferences about Integrated Circuits design held in China. Sponsored by IEEE, the Institution of Engineering & Technology (IET) and the Chinese Institute of Electronics (CIE) and held seven times since 1994, the conference provides a forum for researchers, students, and engineers working in the fields of SOC/VLSI circuits design, EDA/CAD technologies and related areas to discuss and exchange state-of- the- art information.

SSCS-Shanghai and Fudan University jointly organized and prepared the program for the 7th International ASIC Conference, which took place on 26-29 October, 2007.

Fudan University Professor Ting-Ao Tang, Chair of SSCS-Shanghai and General Chair of ASICON 2007, welcoming attendees to the Conference.

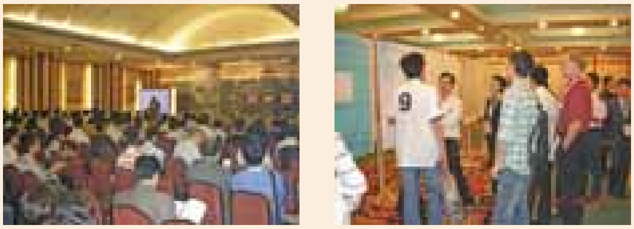
On its opening day, the conference offered seven tutorials:

- "Design of Integrated Radio Transceiver Front-ends in Submicron and Deep Submicron CMOS Technologies," Prof. John Long, TU Delft, The Netherlands;
- "A/D Converters for Wireless Communication in Nanometer CMOS," Prof. Yun Chiu, University of Illinois at Urbana-Champaign, USA;
- "SOC Design Flow Case Tutorial: Design a Video Processing Pipeline," Dr. Wei Ruan, Shengqi Yang and Tiehan Lu, Intel, USA;
- "Inductance Extraction and Compact Modeling of Inductively Coupled Interconnects in the Presence of Process Variations," Prof. Sheldon Tan, UC Riverside and Prof. Jeffrey Fan, Florida International University, USA;
- "Recent Advances and Trends in Semiconductors," Dr. Linming Jin, Brocade Communications Systems Inc., USA;
- "ESD and Latch-up: Computer Aided Design (CAD) Tools And Methodologies For Today And Future VLSI Designs," Dr. Steven Voldman IBM, USA;
- "Software Defined Cognitive Radios," Prof. A.H., Tewfik, Prof. Ramesh Harjani , Prof. Gerald E. Sobelman, University of Minnesota.

Four keynote speakers gave invited speeches on three successive mornings:

- Dr. Kevin Zhang (Intel), "Circuit Design in Nano-Scale CMOS Era";
- Dr. Steven Voldman (IBM) "ESD advanced technology";
- Prof. Takeshi Ikenaga (Waseda University, Japan), "Video Compression LSI: Past, Present, and Future Trends";
- Dr. Steve Leibson (Technology Evangelist Tensilica, Inc., USA), "Challenges for Consumer Electronics in the 21st Century."

Of 464 papers submitted from 22 countries, 403 came from universities (86%) and 63 from industries and institutes (14%). 230 papers were accepted for oral presentation in four parallel sessions.



Attendees at a presentation and discussing poster papers at ASICON, 2007.

At the closing banquet, the four winners of the ASICON 2007 Excellent Student Paper awards were announced:

- M. AbdEsalam Hassan (Osaka University of Japan), "A SystemC Simulation Modeling Approach for \Allocating Task Precedence Graphs to Multiprocessors";
- Lang Mai (Fudan University), "A novel CML-based synchronization algorithm for IR-UWB communication";
- Xin Li (Tsinghua University of China), "Thermal-aware Incremental floorplanning for 3D ICs"
- Guohua Chen (Chinese Academy of Sciences), "Design of a Low Power Digital Core for Passive UHF RFID Sensors."

This year was the first time that ASICON was held in Guilin, one of the most beautiful cities for tourists in China. Attendees enjoyed the mountains and rivers as well as the opportunity to share research results at the Conference. The 8th ASICON will be held in Shanghai in October, 2009.

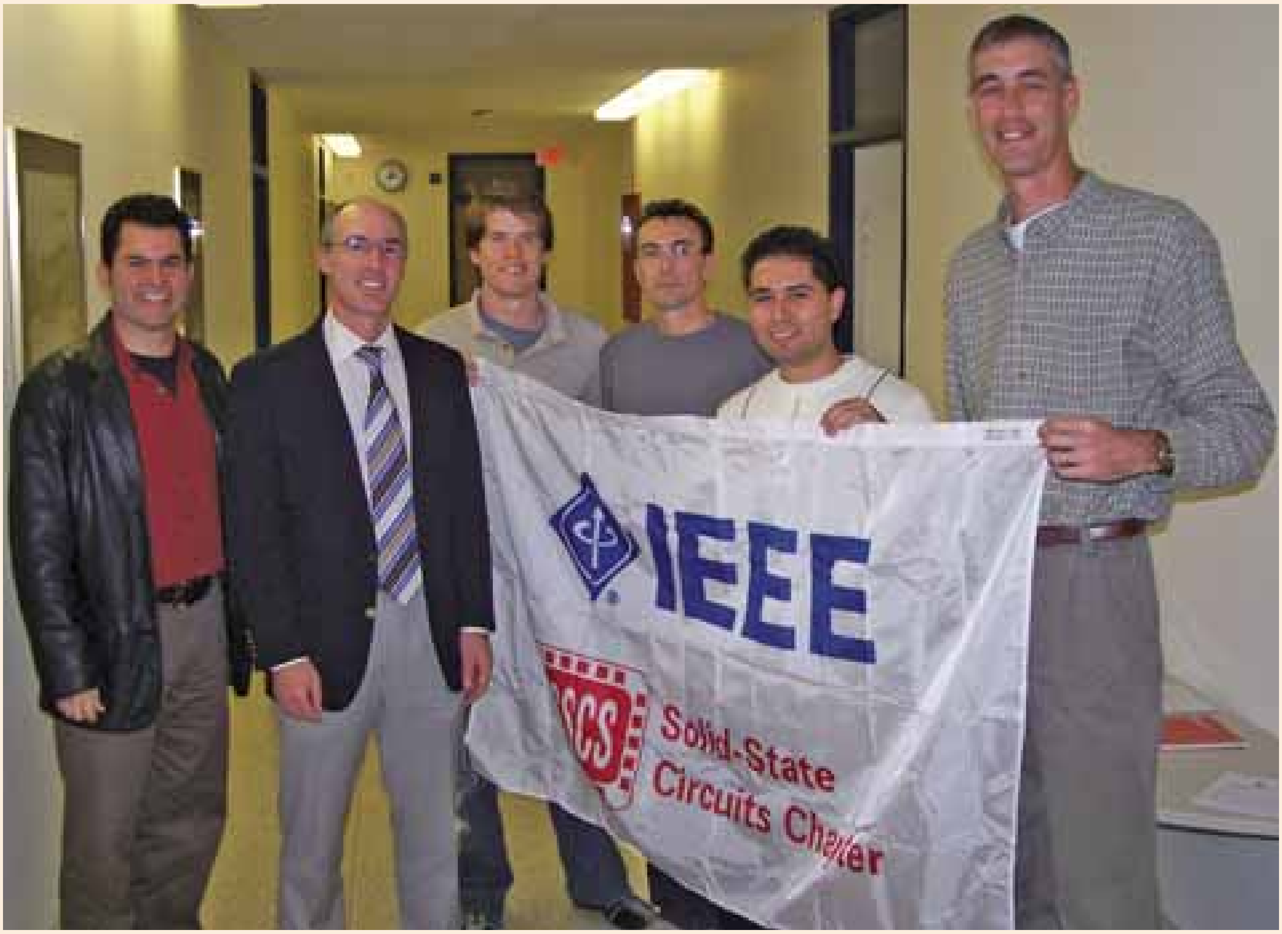
Ian Galton Speaks on "Performance Enhancement Techniques for Fractional-N PLLs" at SSCS-CASS/Atlanta

Prof. Gabriel A. Rincón-Mora, Chairman, Atlanta SSCS-CASS Chapter, Georgia Institute of Technology, rincon-mora@ece.gatech.edu

Forty-eight people, including two members from industry and three Georgia Tech professors attended Ian Galton's lecture on PLLs at SSCS-Atlanta on 7 November, 2007. According to chapter member Oscar Palomino, "PLL technology is a very popular topic at Georgia Tech, which offers graduate courses and features various research teams developing novel designs on the subject."

Abstract: This talk provides a tutorial-level explanation of fractional-N PLLs for frequency synthesis followed by a description of recently-developed techniques that can be used to enhance their performance. The tutorial portion of the talk briefly reviews integer-N PLLs and then explains the additional ideas and issues associated with the extension to fractional-N PLLs. Topics include a self-contained explanation of the relevant aspects of _¤__ modulation, and non-ideal effects of particular concern in fractional-N PLLs such as charge pump nonlinearities and data-dependent divider delays. Then, a charge pump linearization technique and an adaptive phase noise cancellation technique are presented, including implementation details and experimental results associated with a 2.4 GHz ISM-band fractional-N PLL CMOS integrated circuit.

Dr. Gabriel Rincón-Mora presents a certificate of appreciation to Dr. Ian Galton on behalf of the Atlanta SSCS-CAS chapter, 7 November, 2007.



From left to right: Dr. Gabriel Rincón-Mora (Chair, SSCS-CAS), Dr. Ian Galton (Distinguished Lecturer), Luke Milner and Huseyin Dinc (Ph.D. EE candidates), Oscar Palomino (M.S.E.E candidate), and Patrick O'Farrell (Secretary, Atlanta SSCS-CAS Chapter & Design Engineer, National Semiconductor).

Academia and Industry Interact in Ireland

SSCS DLs Pelgrom, Galton, and Castello Speak at Chapter Events

Peter M. Kennedy, FIEEE MRIA Vice-President for Research Policy & Support
North Wing, Main Quad University College Cork, Ireland, vpresearch@ucc.ie

As Ireland pushes a national research and technology transfer agenda, the SSCS Ireland Chapter has been actively promoting interaction between academia and the circuit design industry by organizing guest lectures, conference previews, and workshops.

Highlights of the year for SSCS Ireland include Distinguished Lectures by *Marcel Pelgrom*, who spoke about "Nanometer CMOS: An Analog Challenge" in Dublin in March; *Ian Galton*, who gave presentations on "Performance Enhancement Techniques for Fractional-N PLLs" and "Mismatch-Shaping DACs for Delta-Sigma Data Converters" in Cork in September; and *Rinaldo Castello*, who spoke about "Reconfigurable RF front-ends for wireless transceivers" in Cork and at the IEEJ Analog VLSI workshop in Limerick in November.

The presentations were attended by graduate students and staff from leading universities and research institutes, as well as mixed-signal and RF designers from a range of companies, including Analog Devices, ChipSensors, Cypress, Freescale, Silicon & Software Systems (S3), and Xilinx.

The Distinguished Lecturer programme is highly appreciated by SSCS members in Ireland, 30% of whom attended at least one of the lectures. A typical comment is that of Cormac O'Sullivan, S3, who remarked, "It's great that we can have such a high calibre of speaker here in Cork" thanks to SSCS.

Further details about the SSCS Ireland Chapter can be found at: sscs.ucc.ie.

SSCS Ireland Chapter Chair Prof. Peter Kennedy, University College Cork (left), with Distinguished Lecturer Ian Galton, UCSD (center), and Roger Whatmore, Director, Tyndall National Institute.

Prof Katsutoshi Saeki of the Institute of Electrical Engineers of Japan (IEEJ) making a presentation to Prof. Rinaldo Castello of the University of Pavia, Italy as a token of appreciation for his invited lecture at the IEEJ Analog VLSI Design Workshop in Limerick on 9 November 2007.

THE LATEST IN SOLID STATE CIRCUITS FROM WILEY AND WILEY-IEEE PRESS

VLSI Circuit Design Methodology Demystified

A Practical Approach for Building up Concepts

Liming Xiu

9780470127421 • November 2007 • Paper • 224pp • $69.95
Wiley-IEEE Press

This book was written to arm engineers qualified and knowledgeable in the area of VLSI circuits with the essential knowledge they need to get into this exciting field and to help those already in it achieve a higher level of proficiency. Few people truly understand how a large chip is developed, but an understanding of the whole process is necessary to appreciate the importance of each part of it. It teaches readers how to become better engineers through a practical approach of diagnosing and attacking real-world problems.

Wireless LAN Radios

System Definition to Transistor Design

Arya Behzad

9780471709640 • December 2007 • Cloth • 240pp $79.95
Wiley-IEEE Press

Wireless LAN Radios presents a sophisticated overview of the subject, covering the necessary theory while emphasizing the practical aspects of this promising technology. Coverage includes 802.11 flavors and system requirements, receiver and transmitter radio architectures, analog impairments and issues, and key radio building blocks. This title also presents a detailed explanation of analog, digital, and mixed-mode calibration techniques for improving system performance and chip yield, while the impact of radio architecture on die size, system cost, and power consumption is also thoroughly evaluated.

Modeling and Design Techniques for Radio-Frequency Power Amplifiers

Arvind Raghavan, Nuttapong Srirattana, Joy Laskar

9780471717461 • December 2007 • Cloth • 224pp • $79.95
Wiley-IEEE Press

Richly complemented with hundreds of figures and equations, *Modeling and Design Techniques for Radio-Frequency Power Amplifiers* introduces and explores the most important topics related to RF power amplifier design under one concise cover. The description of state-of-the-art techniques makes this book a valuable and handy reference for practicing engineers and researchers, while the breadth of coverage makes it an ideal text for graduate- and advanced undergraduate-level courses in the area of RF power amplifier design and modeling.

Nonvolatile Memory Technologies with Emphasis on Flash

A Comprehensive Guide to Understanding and Using Flash Memory Devices

Joseph E. Brewer, Manzur Gill

9780471770022 • December 2007 • Cloth • 768pp • $135.00
Wiley-IEEE Press

Nonvolatile Memory Technologies with Emphasis on Flash seamlessly gathers together information on the complex group of technologies that make up nonvolatile memory into one well-organized book. While providing a detailed view of state-of-the-art mainline technologies that are currently being produced in high volume, it also explores less-exposed and alternate technologies that may emerge in the future. Written as a general reference, this book serves as both an ideal supplemental text for undergraduate and graduate courses on nonvolatile memory and as an invaluable resource for engineers, technical managers, and other sophisticated practitioners.

Adaptive Inverse Control

A Signal Processing Approach, Reissue Edition

Bernard Widrow, Eugene Walach

9780470226094 • October 2007 • Cloth • 508pp • $125.00
Wiley-IEEE Press

Written by two pioneers in the field, this book presents methods of adaptive signal processing that are borrowed from the field of digital signal processing to solve problems in dynamic systems control. This unique approach allows engineers in both fields to share tools and techniques. Clearly and intuitively written, *Adaptive Inverse Control* illuminates theory with an emphasis on practical applications and commonsense understanding.

Discrete-Signal Analysis and Design

William E. Sabin

9780470187777 • December 2007 • Cloth • 192pp • $125.00 • Wiley

This book provides an introduction to discrete-time and discrete-frequency signal processing, which is rapidly becoming an important, modern way to design and analyze electronics projects of all kinds. It presents discrete-signal processing concepts from the perspective of an experienced electronics or radio engineer, which is especially meaningful for practicing engineers, technicians, and students. The approach is almost entirely mathematical, but at a level that is suitable for undergraduate curriculums and also for independent, at-home study using a personal computer. The accompanying CD-ROM includes Mathcad® v.14 Academic Edition, providing users with a sophisticated and world-famous tool for a wide range of applied mathematics capabilities beyond the book itself.

Electromagnetic Theory

Julius Adams Stratton

9780470131534 • January 2007 • Cloth • 640 pp • $95.00
Wiley-IEEE Press

First published in 1941, Julius Stratton's classic *Electromagnetic Theory* has been a mainstay for generations of students, researchers, and scientists. This classic reissue of the original features a foreward by Dr. Donald G. Dudley that details the book's contribution to the field, and an introductory biography by Dr. Paul E. Gray, former MIT President and colleague of Dr. Stratton. Areas discussed include Hansen vector wave functions, the outstanding treatment of phase and group velocity, and the Stratton-Chu formulation for integration of the vector Helmholtz equations.

FPGA Prototyping by VHDL Examples

Xilinx Spartan™-3 Version

Pong P. Chu

9780470185315 • January 2008 • Cloth • 468pp • $89.95 • Wiley

This book uses a "learning by doing" approach to introduce the HDL (hardware description languages) and FPGA development process to designers through a series of hands-on experiments. A wide range of examples is included, from a simple gate-level circuit to an embedded system with an eight-bit soft-core microcontroller and customized I/O peripherals. All examples can be synthesized and physically tested on an actual FPGA prototyping board.

WILEY
Publishers Since 1807

IEEE

ORDERING INFORMATION

1 (877) 762-2974 in North America + 44 (0) 1243 843294 in Rest of World

Log on to www.wiley.com/ieee

Enter Promotion Code SSCJ8 to receive 20% off featured titles at checkout.

Eight Technical Meetings in Fort Collins during 2007

SSCS DLs Fischette, Allstot and Nguyen Speak

Alvin Loke, Denver Chapter Chair, alvin.loke@ieee.org

The Denver SSCS Chapter hosted a total of eight seminars in 2007, three of which were sponsored by the SSCS Distinguished Lecturer Series. Topics ranged from cutting-edge microprocessors to techniques for designing high-speed serial links to forefront technologies such as next-generation lithography.

The year started with *Robin Porter* from Venture Operations describing ingredients for establishing a successful start-up. By comparing two companies competing in the thin server appliance space (Cobalt and Whistle), she emphasized the importance of business model strategy and supply chain management in contributing to boom vs. bust.

Given the high concentration of local companies involved in serial link design, it was no surprise that our next talk by *Troy Beukema* from IBM Research (Yorktown, NY) was a big hit. Mr. Beukema provided a broad overview of the systems, circuits, and modeling challenges that lie ahead to overcome successful links beyond 10Gb/s.

Three new SSCS Distinguished Lecturers visited our chapter: *Dennis Fischette*, from Advanced Micro Devices (Sunnyvale, CA), delivered a practical overview of monolithic phase-locked loop design. Next, *Prof. David Allstot* from the University of Washington did a phenomenal job explaining bandwidth extension fundamentals using inductors and transformers. Shunt and series peaking never looked easier! Finally, *Prof. Clark Nguyen* from the University of California rounded up the year with a fascinating seminar on MEMS for RF front-ends.

Dr. Shawn Searles from Advanced Micro Devices (Austin, TX) gave an extended encore of his ISSCC 2007 paper on AMD's Barcelona native quad-core processor. In addition, *Profs. Gu-Yeon Wei* and *David Brooks* came from Harvard University to explain how they are tackling device variability using joint architecture and circuit techniques such as local voltage regulation for dynamic voltage-frequency scaling for multiple cores and alternative memory structures.

Local adjunct professor *Dr. Hugh Grinolds* from Colorado State University (Fort Collins, CO) presented a nice overview of extreme ultraviolet (EUV) lithography as the next viable replacement for 193nm immersion ArF. He introduced key optical principles and discussed the present state of development from both equipment and process perspectives.

The 2008 elections for chapter officers were recently held and we welcome two new members to the team: Steve Martin from Avago Technologies and Visvesh Sathe from AMD.

Please visit ewh.ieee.org/r5/denver/sscs/ for more information, including past presentation slides, about our chapter events. Starting in 2007, all seminars have been videotaped onto DVDs, thanks to Program Chair Bruce Doyle doubling his duties as videographer!

After SSCS DL David Allstot explained bandwidth extension fundamentals in Fort Collins, from left: Bob Barnes (Vice Chair & Treasurer), Ron Kennedy, Bruce Doyle (Program Chair), Mike Gilsdorf, Prof. David Allstot, Don McGrath (former Chair), Alvin Loke, and Tin Tin Wee (Secretary & Webmaster).

SSCS Far East Chapters Meet in Jeju, Korea on 13 November, 2007

Coinciding with the 3rd annual A-SSCC, the 2nd SSCS Region 10 chapter meeting was chaired by Jan Van der Spiegel (SSCS Chapters Committee Chair) and attended by AdCom President-Elect Willy Sansen, SSCS Region 10 Representative and Chapter Committee member C.K. Wang and the officers of eight Chapters (Beijing, Kansai, Seoul, Shanghai, Singapore, Tainan, Taipei and Tokyo). The participants, who shared best practices with each other and the AdCom, were (from left): Prof. Hanjun Jiang (Beijing), Prof. Suki Kim (Seoul), Prog. Zhihua Wang (Beijing), Dr. Kabuo Hideyuki (Kansai), Prof. Sung-min Park (Seoul), Prof. Tohru Furuyama (Tokyo), Prof. Andy Chung (Seoul), Prof. Willy Sansen, Prof. Jan Van der Spiegel, Prof. Shen-luan Liu (Taipei), Prof. Akira Matsuzawa (Tokyo), Prof. Chua-Chin Wang (Tainan), Prof. C. K. Wang (Taipei), Prof. Ting-Ao Tang (Shanghai), Prof. Kwang Sub Yoon (Seoul) and Prof. Yong Ping Xu (Singapore).

Letters to the Editor

Dear Editor,

With regard to Thomas Lee's "Tales of the Continuum: A Subsampled History of Analog Circuits" in the Fall 2007 issue, I'd like to make a comment.

This article would have been improved had it included some reference to Karl D. Swartzel, Jr.'s op amp. Swartzel was the Bell Labs designer of the original amplifier used in the M-9 analog computational system (US patent 2401779). A Google link search on this May 1, 1941 patent filing shows a string of 77 references, some indication that it was indeed an influential work. It is truly unfortunate that this key development so often gets overlooked.

The author's Reference 9 includes a narrative of the early Bell Labs projects, and places the earliest op amp developments and Swartzel's work in some perspective.

Walt Jung
IEEE Member

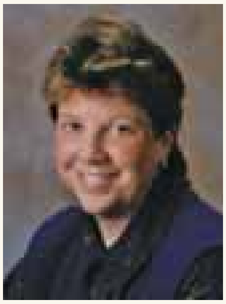
Corrections

On p. 58 of the Fall ’07 issue, the middle name of Dr. R. Jacob Baker was misspelled as Jakob.

In the same issue, “A History of The Continuously Innovative Analog Integrated Circuit,” section iv, paragraph 1, line 4 should have read “Max Hauser” not “Mark Hauser” and “Bob Brodersen,” not “Bob Broderson.”

In the same article, section iv, paragraph 2, line 8 should have read “In 1987 they were able” not “In 1985.” *Stephen Lewis, UC-Davis, lewis@ece.ucdavis.edu*

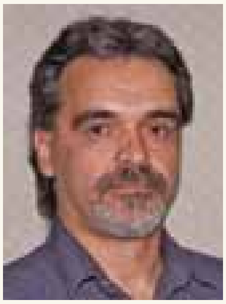
Fiez, Kuroda, Nauta, Sevenhans and Soyuer Elected to AdCom


Terri Fiez


Tadahiro Kuroda


Bram Nauta


Jan Sevenhans


Mehmet Soyuer

Terri Fiez, Tadahiro Kuroda, Bram Nauta, Jan Sevenhans and Mehmet Soyuer were elected to SSCS AdCom and will serve three year terms governing the Society, beginning 1 January 2008. Coming from industry and academia, from Asia, Europe, and North America, these five join ten other elected AdCom members whose terms overlap.

Terri S. Fiez received the B.S. and M.S. in Electrical Engineering in 1984 and 1985, respectively, from the University of Idaho, Moscow. In 1990, she received the Ph.D. degree in Electrical and Computer Engineering from Oregon State University, Corvallis. From 1985 to 1987 and in 1988 she worked at Hewlett-Packard Corp. in Boise and Corvallis, respectively.

In 1990, Dr. Fiez joined Washington State University as an assistant professor and became an associate professor in 1996. In the fall of 1999, she joined the Department of Electrical and Computer Engineering at Oregon State University as Professor and department head and became the Director of the School of Electrical Engineering and Computer Science in 2003. She has served on the committees of the IEEE International Solid-State Circuits Conference, IEEE Custom Integrated Circuits Conference, and ISCAS, and was a guest editor of the Journal of Solid-State Circuits. Dr. Fiez was awarded the NSF Young Investigator Award, the Solid-State Circuits Society Predoctoral Fellowship, and the 2006 IEEE Education Activities Board Innovative Education Award. Her research interests are the design of high performance analog signal processing building blocks, simulation and modeling of substrate coupling effects in mixed-signal ICs, and innovative engineering education approaches. This will be Dr. Fiez second term as an elected member of the Solid-State Circuits Society (SSCS) Administrative Committee (AdCom). She is an IEEE Fellow.

Tadahiro Kuroda received the Ph.D. degree in electrical engineering from the University of Tokyo in 1999. In 1982, he joined Toshiba Corporation, where he designed CMOS SRAMs, gate arrays and standard cells. From 1988 to 1990 he was a Visiting Scholar at the University of California, Berkeley, where he conducted research in the field of VLSI CAD. In 1990, he returned to Toshiba for research and development of BiCMOS ASICs, ECL gate arrays, high-speed and low-power CMOS LSIs for multimedia and mobile applications. He developed a Variable Threshold-voltage CMOS (VTCMOS) technology for controlling VTH through substrate bias and a Variable Supply-voltage scheme for controlling VDD by an embedded DC-DC converter, and employed them in a microprocessor core and an MPEG-4 chip in 1997. In 2000, he moved to Keio University, Yokohama, Japan, where he has been a professor since 2002. This year he is Visiting MacKay Professor at the University of California, Berkeley. His research interests include ubiquitous electronics, sensor networks, wireless and wireline communications and ultra-low-power CMOS circuits. He has published more than 200 technical publications including 50 invited papers, 18 books/chapters, and filed more than 100 patents.

Dr. Kuroda served as the General Chairman for the Symposium on VLSI Circuits and as Vice Chairman for ASP-DAC. He has chaired sub-committees for A-SSCC, ICCAD and SSDM, and served on conference program committees for the Symposium on VLSI Circuits, CICC, DAC, ASP-DAC, ISLPED, and others. He is an IEEE Fellow and an IEEE SSCS Distinguished Lecturer.

Bram Nauta was born in Hengelo, The Netherlands in 1964. In 1987 he received the M. Sc. degree cum laude in electrical engineering from the University of Twente, Enschede, The Netherlands. In 1991 he received the Ph.D. degree from the same university on the subject of analog CMOS filters for very high frequencies.

In 1991 he joined the Mixed-Signal Circuits and Systems Department of Philips Research, Eindhoven the Netherlands, where he worked on high speed AD converters and analog key modules. In 1998 he returned to the University of Twente as full professor heading the IC Design group, which is part of the CTIT Research Institute. His current research interest is high-speed analog CMOS circuits. He is also a part-time consultant in industry.

Dr. Nauta served as Associate Editor of IEEE Transactions on Circuits and Systems -II; Analog and Digital Signal Processing (1997-1999), as Guest Editor (1998) and Associate Editor (2001-2006) for the IEEE Journal of Solid-State Circuits. He is member of the technical program committees of ISSCC, ESSCIRC, and Symposium on VLSI circuits. He is co-recipient of the ISSCC 2002 "Van Vessem Outstanding Paper Award".

Nauta is the Editor in Chief of the IEEE Journal of Solid-State Circuits and recently elevated IEEE Fellow.

Jan Sevenhans, who is an IEEE Fellow recognized for "contributions to solid-state telecom transceiver integration," joined the Communication High Voltage business unit of AMI Semiconductor in Belgium in 2005 and previously was a distinguished Member of the Technical Academy of Alcatel Bell in Antwerp, Belgium. He served as Program chair of ISSCC 2006 and has been European Chair of the International Solid-State Circuit Conference (ISSCC). In 2002 he chaired the workshop "Analog telecom access circuits and concepts" at ISSCC.

Born in 1955, Dr. Sevenhans received a Masters degree in 1979 and a Ph.D. in 1984 from the KU Leuven in Belgium; his doctoral dissertation focused on CCD imagers for facsimile applications. He joined Alcatel Bell in 1987, working on analog and RF circuit design for telecom applications in GSM, ADSL, ISDN, and POTs, and on CMOS and bipolar silicon technology. He has filed many patents and published numerous articles in IEEE conference proceedings and journals. Since the late eighties he has been involved in many European research projects such as GSM in Jessi, Medea, Medea+, RACE, IST, and ESPRIT and Girafe - Gigahertz Radio front Ends, in addition to Medea A203, SODERA, and SPACE. Over the past ten years, he has served as reviewer and/or evaluator of several European projects, and as Region 8 representative for the SSCS AdCom.

Mehmet Soyuer received the B.S. and M.S. degrees in electrical engineering from the Middle East Technical University, Ankara, Turkey in 1976 and 1978. He received the Ph.D. degree in electrical engineering from the University of California at Berkeley in 1988, subsequently joining IBM at the Thomas J. Watson Research Center, Yorktown Heights, NY as a Research Staff Member. His work has involved high-frequency mixed-signal integrated circuit designs, in particular monolithic phase-locked-loop designs for clock and data recovery, clock multiplication, and frequency synthesis using silicon and SiGe technologies.

At IBM Thomas J. Watson Research Center, Dr. Soyuer managed the Mixed-Signal Communications Integrated-Circuit Design group from 1997 to 2000. He was the Senior Manager of the Communication Circuits and Systems Department from 2000 to 2006. In 2006, he was promoted to the position of Department Group Manager, Communication Technologies, at Thomas J. Watson Research Center.

Dr. Soyuer has authored numerous papers in the areas of analog, mixed-signal, RF, microwave, and nonlinear electronic circuit design, and he is an inventor and co-inventor of eight U.S. patents. Since 1997, he has been a technical program committee member of the International Solid-State Circuits Conference (ISSCC). He was an Associate Editor of the IEEE Journal of Solid-State Circuits from 1998 through 2000, and was one of the Guest Editors for the December 2003 Special ISSCC Issue. Dr. Soyuer chaired the Analog, MEMS and Mixed-Signal Electronics Committee of the International Symposium on Low Power Electronics and Design (ISLPED) in 2001. He was also a technical program committee member of the Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF) in 2004 and 2006. This will be Dr. Soyuer's second term as an elected member of the Solid-State Circuits Society (SSCS) Administrative Committee (AdCom). Dr. Soyuer is a senior member of IEEE and a Distinguished Lecturer of IEEE-SSCS.

Look for the responsibilities of AdCom members in the accompanying announcement for next years election, "Call for Nominations for AdCom." Thanks to these global technical experts for being willing to serve!

Call for Nominees for SSCS Administrative Committee Election

Each year SSCS elects five members to govern the Society on the body called the Administrative Committee (AdCom). These AdCom members serve three year terms. The Bylaws of the Society guarantee a choice for members in the election by requiring that the nominating committee prepare a slate of a minimum of 8 candidates for the 5 positions. The nominating committee begins its work in the beginning of the year in order to announce its candidates in the summer News issue. Members interested to run or to nominate others should send their recommendations to the Chair of the Nominating committee, Richard C. Jaeger, jaeger@eng.auburn.edu. The election is in the fall and student members are not eligible to run or vote. The five nominees receiving the highest number of votes of the Society membership will be elected. There is also a petition process for interested parties who are not endorsed by the Nominating Committee.

Scope

Elected AdCom members are expected to attend the two administrative meetings each year. Some Committee work is carried on by email throughout the year. The AdCom oversees the operations of chapters, publications and conferences including the Journal of Solid-State Circuits, the International Solid-State Circuits Conference, the Custom Integrated Circuits Conference, the VLSI Circuits Symposium, and the Asia Solid-State Circuits Conference. In addition, the Society cosponsors or technically cosponsors a number of other conferences including the European Solid-State Circuits Conference.

The AdCom has responsibility for overseeing these and for other potential future technical activities within the Society's field of interest.

Terms of Office

- The term of office is three years beginning 1 January 2009.
- AdCom members may be reelected to a second consecutive term.
- Members who miss two consecutive AdCom meetings shall be dropped from membership in the absence of extenuating circumstances.

Nominees by Petition

Those interested to use the petition process must begin no later than July 15, immediately after the Nominating Committee's slate has been announced in the summer issue. Contact the SSCS Executive Director, a.oneill@ieee.org. Once eligibility of the petition candidate is verified, any society voting member who wishes to sign such petition may do so electronically through ton-line software under the administration of the IEEE Corporate Office. The number of signatures required for a petition candidate is 2% of SSCS voting members at the time the petition process begins. This is expected to be approximately 140 signatures. Once a member is posted on the site, he or she will remain up to receive endorsement signatures, until a predetermined date in late August or early September when the election begins.

2008 IEEE
Compound Semiconductor IC Symposium

INTEGRATED CIRCUITS IN GaAs, InP, SiGe, GaN and OTHER COMPOUND SEMICONDUCTORS

October 12 – 15, 2008
Monterey, CA, USA

Sponsored by the IEEE Electron Devices Society
Technically co-sponsored by the Solid State Circuits Society
and the Microwave Theory & Techniques Society

FIRST CALL FOR PAPERS

2008 CSIC Symposium

Over the last 30 years, CSICS has become the preeminent international forum on developments in integrated circuits using compound semiconductors such as GaAs, InP, GaN, SiGe and other materials. Coverage embraces all aspects of the technology, from materials issues and device fabrication, through IC design and testing, high volume manufacturing, and system applications. The IEEE Compound Semiconductor IC Symposium (CSICS) provides the ideal forum to present your latest results in high-speed digital, analog, microwave/millimeter wave, mixed mode, and optoelectronic integrated circuits. First-time papers concerned with the utilization and application of InP, GaAs, SiGe, GaN and other compound semiconductors in military and commercial products are invited. Specific technical areas of interest include:

- Innovative RFIC Device & Circuit Concepts
- Millimeter-wave/High-Speed CMOS IC
- Circuit Design & Fabrication
- Manufacturing Technology & Cost Issues
- CAD/CAM/CAT Tools & Techniques
- IC Testing & Methodology
- Packaging Technology
- Reliability
- Advanced Device Applications
- System Applications (e.g., wireless, vehicular, RADAR, military)
- Optoelectronic and OEIC applications

Symposium Highlights

High quality technical papers will be selected from worldwide submissions for oral presentation and publication in the Symposium Digest. Invited papers and panel sessions on topics of current importance to the Compound Semiconductor IC community will complete the program. Extended versions of selected papers from the Symposium will be published in a special issue of the *IEEE Journal of Solid State Circuits.*

Co-Location with BCTM in 2008

We are pleased to announce that CSICS will co-locate for 2008 with the IEEE Bipolar / BiCMOS Circuits and Technology Meeting (BCTM) in Monterey. Joint functions including an afternoon session, social functions and the exhibition will permit cross-fertilization of ideas between these two technical meetings.

Compound Semiconductor Primer Course

The Symposium will again offer the popular primer course, "Basics of GaAs, InP and SiGe RFICs," which is an introductory-level class intended for those wishing to obtain a broad overview of RFIC technology. The Sunday evening course will cover materials and processes, device operation, and both analog/microwave and digital ICs. The Course will be tailored to provide the specific background needed for participants to understand and appreciate the papers presented in the Symposium Technical Program.

Short Course

Two short courses will be held on Sunday, October 12, 2008. The courses are currently under development and will cover current topics in the industry. Organizer: Dave Halchin, RFMD, E-mail: dhalchin@rfmd.com, ph: +1-336-931-8123.

Deadline for Electronic Receipt of Abstracts is Close of Business, May 12, 2008

Authors must submit an Abstract (not more than 4 pages including figures and other supporting material) of results not previously published or not already accepted by another conference. Papers will be selected on the basis of the abstract.

The abstract must concisely and clearly state:

- **a) The purpose of the work**
- **b) What specific new results have been obtained**
- **c) How it advances the state-of-art or the industry**
- **d) References to prior state-of-art**
- **e) Sub-committee preference:**
  - **▪ Digital OEIC,**
  - **▪ Analog RF/Microwave,**
  - **▪ Technology/Manufacturing**
  - **▪ CMOS Technology and ICs**

The abstract must include: the title, name(s) of the authors(s), organization(s) represented, correspondence authors' postal and electronic addresses, and telephone and FAX numbers. Please indicate your preference for subcommittee review. The program committee will honor the authors' preference where possible, but reserves the right to place the paper in other review categories.

Company and governmental clearances must be obtained prior to submission of the abstract.

The accepted abstracts may be used for publicity purposes. Portions of these abstracts may be quoted in magazine articles publicizing the Symposium. **Please note on the abstract if this is not acceptable.**

Authors must submit the Abstract electronically using the www.csics.org web page. Please note that the **only** accepted file format is **PDF**. Authors will be informed regarding the results of their submissions by June 24, 2008. Authors of accepted papers will be required to submit an **MS-Word version** of a 4-page camera-ready extended abstract to IEEE by July 21, 2008 for publication in the Symposium Technical Digest.

Further questions on abstract submission may be addressed to the Symposium Technical Program Chair:

Marko Sokolich
TEL: 1-310-317-5148
Email: msokolich@hrl.com

All Symposium information, including abstract submission instructions and a link to our abstract submission address is available on our website at:

http://www.csics.org/

CEDA Celebrates Second Anniversary

President's Message

The IEEE Council on Electronic Design Automation (CEDA) has made great progress in the two years since its creation. In June 2005, CEDA was formed to create a focal point and pull together EDA activities in the IEEE. The CEDA Board of Governors, officers, and volunteers have done a lot to create the CEDA that you now recognize. Since its formation, CEDA has increased sponsorship of conferences, added publications, and started technical activities. If you are interested in volunteering a few hours a month, please e-mail me (aldunlop@adelphia.net) or any of the council officers, and we can plan a useful, rewarding activity for you.

At its inception, CEDA took the leadership in cosponsoring the Design Automation Conference (DAC), the IEEE/ACM International Conference on Computer-Aided Design (ICCAD), and the Design, Automation and Test in Europe Conference (DATE). These are significant conferences in the EDA space. We have since grown to sponsor 12 conferences and workshops focusing on specific topics or regions, and the roster is increasing. A list of the specific meetings that CEDA sponsors is available at CEDA's Web site, www.ieee-ceda.org.

In publications, the council copublishes IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (T-CAD) with the IEEE Circuits and Systems Society. We started the CEDA Currents Newsletter in 2006 to cover news and noteworthy events. Recently, CEDA launched the electronic version of IEEE Design & Test, working in cooperation with the IEEE Computer Society and the Test Technology Technical Council (TTTC).

CEDA established an awards committee in 2005, which became part of the IEEE Fellow selection process in 2006. This year, CEDA became a cosponsor of the Phil Kauffman award with the EDA Consortium.

The CEDA Technical Activities Committee supports several activities, including student competitions in physical design, logic synthesis, and circuit design; and a Distinguished Speaker Series featuring the best papers from DAC, ICCAD, T-CAD, and other forums. (Videos of the Distinguished Speaker Series are available on our Web site.) CEDA also cosponsors the Computer-Aided Network Design (CANDE) Technical Committee (www.cande.net) and the Design Automation Technical Committee (http://tab.computer.org/datc) with the IEEE Circuits and Systems Society and the IEEE Computer Society, respectively.

This is only the beginning. There are many other activities on the horizon and many more possibilities. At the core, they are driven by the interests and zeal of our volunteers. For instance, we are in the process of creating an infrastructure for research and have seeded a small effort in this area. We are looking for volunteers for this project, and of course, any other project you may have preference for. So, look us up on the Web or in person, and drop us a note if you are interested in learning further.

Al Dunlop, CEDA President

TTTC Joins CEDA's Launch of IEEE D&T Electronic Edition

Working in cooperation with the IEEE Computer Society Press, CEDA recently launched the IEEE D&T Electronic Edition. We are happy to report that the Test Technology Technical Council (TTTC) has joined this effort.

The D&T Electronic Edition is an exact, cover-to-cover copy of the printed magazine including all illustrations, graphics, conference calls and other advertising. This compact, easy-to-navigate format will be delivered every two months for an annual subscription cost of $19.95 (half the best member price for subscription to the regular D&T print issue). To receive this excellent rate, you will not need to be a member of the IEEE or any society. Simply sign up for the electronic edition through CEDA.

Here is what our friends are saying about IEEE D&T Electronic Edition:

D&T and TTTC have enjoyed a long and close relationship at multiple levels, from editors and authors to special sections, embedded newsletters, and electronic broadcasts; to membership and readership of D&T. In a changing publishing environment, easy access to publishing and distribution channels enables us to provide worthwhile exclusive benefits to a broader community. The importance of peer-reviewed, carefully produced, and high-quality technical content is even more acutely felt by the busy professional. We are proud to see D&T take the lead in providing low-cost access to such content.

—Yervant Zorian, D&T EIC Emeritus and TTTC Senior Past Chair

The D&T Electronic Edition joins a growing list of attractive membership benefits for test technology professionals. As the lead representative of an expanding worldwide test community, TTTC is pleased to actively support and participate in this initiative, as this will provide clear benefits for existing and future members of TTTC.

—Andre Ivanov, TTTC Chair

D&T Electronic Edition is a bold new experiment in providing low-cost access to high-quality peerreviewed technical material for the EDA professional. With this launch, D&T joins IEEE Transactions on Computer-Aided Design as a complementary publication targeted toward the busy professional. We hope you like the new magazine and join us in the expanding EDA community at CEDA.

—Al Dunlop, CEDA President

For more information and to sign on, please visit CEDA's Web site at www.ieee-ceda.org.

New Codesign Contest at MEMCODE

Forrest Brewer, University of California, Santa Barbara and James C. Hoe, Carnegie Mellon University

New to the 5th ACM/IEEE International Council on Formal Methods and Models for Codesign --MEMOCODE, held 30 May through 1 June 2007 in Nice, France and cosponsored by CEDA -- is the hardware-software codesign contest. Its goal is to identify issues specific to codesign practice and to foster greater interest in the design aspects of MEMOCODE. The contest also serves to showcase advances in codesign tools and methodologies.

To make the contest feasible, we decided to keep the term relatively short and to provide a working code base for at least one inexpensive, easily available platform. We ultimately opted for a problem that could be done well in a week, and we allowed the contestants a month's lead time to solve it.

We did not wish to limit the competition to a particular execution platform because we thought that many design groups would be more familiar with their preferred platforms. Instead, we left the choice of platform to the contestants and provided a grading metric that attempts to equalize the differences. We did, however, select the Xilinx XUP2VP prototyping board as the reference platform. The XUP2VP board provides a large variety of interfaces, is well supported, and is inexpensive. The onboard Virtex-II Pro XC2VP30 FPGA has a substantial programmable-logic fabric, a fair amount of on-chip memory, and two PowerPC 405 embedded processors. For the XUP2VP environment, we provided reference starter design materials, including a software-only reference solution and a reference hardware-software interface library comprising ready-to-use C functions and Verilog modules.

The design problem chosen for 2007 was the Blocked Matrix-Matrix Multiplication. The basic algorithm, though fundamentally simple to understand, lends itself to a large space of high-leverage optimizations in managing data movement, storage, and bandwidth. We designed the problem to require hardware involvement in the design as well as a software component. We focused on performance as the primary metric of merit. The metric used is the speedup achieved by the contestants' design, relative to the official software-only reference design on their platform of choice. We further asked the contestants to describe the design in sufficient detail so that a panel of judges could make decisions about the elegance of the approach as well as the efficacy of a particular design. We felt that it was important for the judging panel to be able to reward a unique or novel solution, even if its overall performance was less competitive.

Two teams, from MIT and Virginia Tech respectively, successfully submitted final designs, which were presented and discussed at the MEMOCODE conference on 31 May 2007. The audience selected the MIT team as the winner, and the Virginia Tech team as a co-winner of the cash award to each team.

Although the contest did not have the number of entrants we had hoped for, the two final entries were of very high quality and offered real technical contributions to share with the conference audience. We believe the codesign contest adds an important new dimension to MEMOCODE and should remain a valuable component in the future. The call for participation for next year's contest is available at memocode07.ece.cmu.edu/contest.html.

Recipients of National Medal of Technology Announced in June

On 12 June 2007, President George W. Bush announced the recipients of the nation's highest honor for technology, the 2005 National Medal of Technology. This prestigious award honors leading innovators in the US. The award is given to individuals, teams, and companies or divisions for their outstanding contributions to the nation's economic, environmental, and social well-being through the development and commercialization of technology products, processes, and concepts; technological innovation; and development of the nation's technological manpower. The 2005 award recipients included

- Semiconductor Research Corporation;
- Alfred Y. Cho of Lucent Technologies, Murray Hills, N.J.;
- Dean L. Sicking, University of Nebraska-Lincoln;
- a team from Wyeth Pharmaceuticals, Madison, N.J.;
- Genzyme Corp., Cambridge, Mass.;
- Xerox, Stamford, Conn.

The US Department of Commerce administers the award, which was established by an act of Congress in 1980. For more information about the National Medal of Technology, visit www.technology.gov/medal.

The Most-Downloaded Articles in 2006

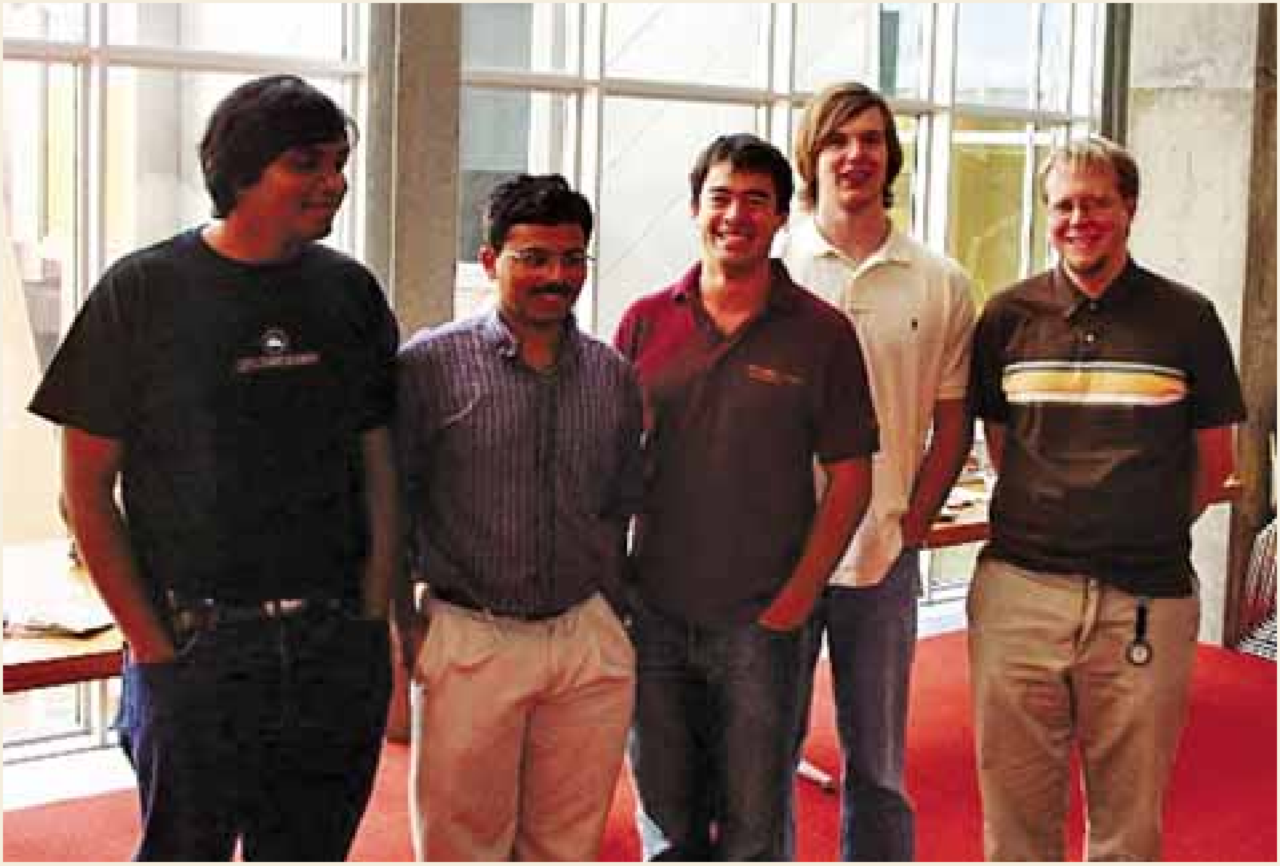
The most-downloaded articles in 2006 from IEEE Design & Test and IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems were:

- "Embedded Systems and the Kitchen Sink" Jan.–Feb. 2006 452
- "Dynamic Power Management in Wireless Sensor Networks" Mar.–Apr. 2005 423
- "Physical Design for 3D System on Package" Nov.–Dec. 2005 381
- "Design, Synthesis, and Test of Networks on Chips" Sep.–Oct. 2005 340

CANDE Holds Successful Workshop on Queen Mary

The Computer-Aided Network Design (CANDE) Technical Committee—a venerable group of EDA stalwarts, thought leaders, and decision-makers— held its annual workshop on 6-8 September 2007 aboard the Queen Mary in Long Beach, California.

The program included sessions on multicore and many-core chips, statistical design, and nano- and biodesign, with keynote talks by Bill Joyner of Semiconductor Research Corp. (SRC) on "CAD and the Queen Mary: Tied Up at the Dock?" and by Drew Endy of MIT on "Technologies for Engineering Biology." More information on CANDE is available at www.cande.net.



At the 5th ACM/IEEE International Council on Formal Methods and Models for Codesign (MEMOCODE) in May, a team from MIT won the first hardware-software codesign contest.

MEMOCODE and DAC Colocated in 2008

The 6th IEEE/ACM Conference on Formal Methods and Models for Codesign (MEMOCODE) will be collocated with the 45th Design Automation on 5-7 June 2008 in Anaheim, California. Every year, MEMOCODE features a design contest to demonstrate the value of system-level design tools and methods in real-life designs, in a competitive environment. For more information, go to www.memocode-conference.com.

Upcoming GRC and FCRP Funding Opportunities

The Global Research Collaboration (GRC), an arm of SRC, conducts mission-driven research on behalf of its members' companies, responding to broad industry needs in semiconductors. The first step in this process involves submitting calls for white papers in response to identified industry needs in various areas, grouped under the following thrusts: computer-aided design and test (CADTS), device sciences, integrated circuits and systems, interconnects and packaging, nanomanufacturing, and cross-disciplinary thrusts. For more information and to see any current calls for white papers, go to //grc.src.org.

The Focus Center Research Program (FCRP) is managed by the directors of five FCRP research centers in charge of research addressing long-term industry needs. For more information, see www.src.org/member/about/funding.asp.

Upcoming CEDA Events

Design, Automation and Test in
Europe Conference (DATE)
10-14 March 2008
Munich, Germany
http://www.date-conference.com

2nd ACM/IEEE International Symposium on Networks-on-Chip (NoCS)
7-11 April 2008
Newcastle University, UK
http://www.nocsymposium.org

For more information regarding sponsorship of conferences and meetings, contact Richard Smith, dsmith@topher.net.

CEDA Currents is a publication of the IEEE Council on Electronic Design Automation. Please send contributions to Kartikeya Mayaram (karti@eecs.oregonstate.edu) Preeti Ranjan Panda (panda@cse.iitd.ac.in) or Anand Raghunathan (anand@nec-labs.com).

KEEP YOUR PROFESSIONAL EDGE WITH INNOVATIVE COURSES FROM IEEE

Staying technically current in today's ever-changing workplace is a career must if you want to maintain your professional edge. IEEE offers an innovative new product called Expert Now, as well as a growing service, the Education Partners Program, to help meet your continuing professional development needs.

65 IEEE "Expert Now" Online Modules Bring Top Tutorials to your Desktop

Expert Now is a collection of over 65 one-hour long, interactive online courses on topics such as aerospace, circuits & devices, communications, computing, laser & optics, microwave theory & techniques, power, reliability, signal processing and software. Presented by experts in the field, each course brings to your desktop the best tutorial content IEEE has to offer through their technical meetings that take place worldwide. Continuing Education Units (CEUs) can be earned upon successful completion of the assessment. To review the course catalog visit ieeexplore.ieee.org/modules.modulebrowse.jsp.

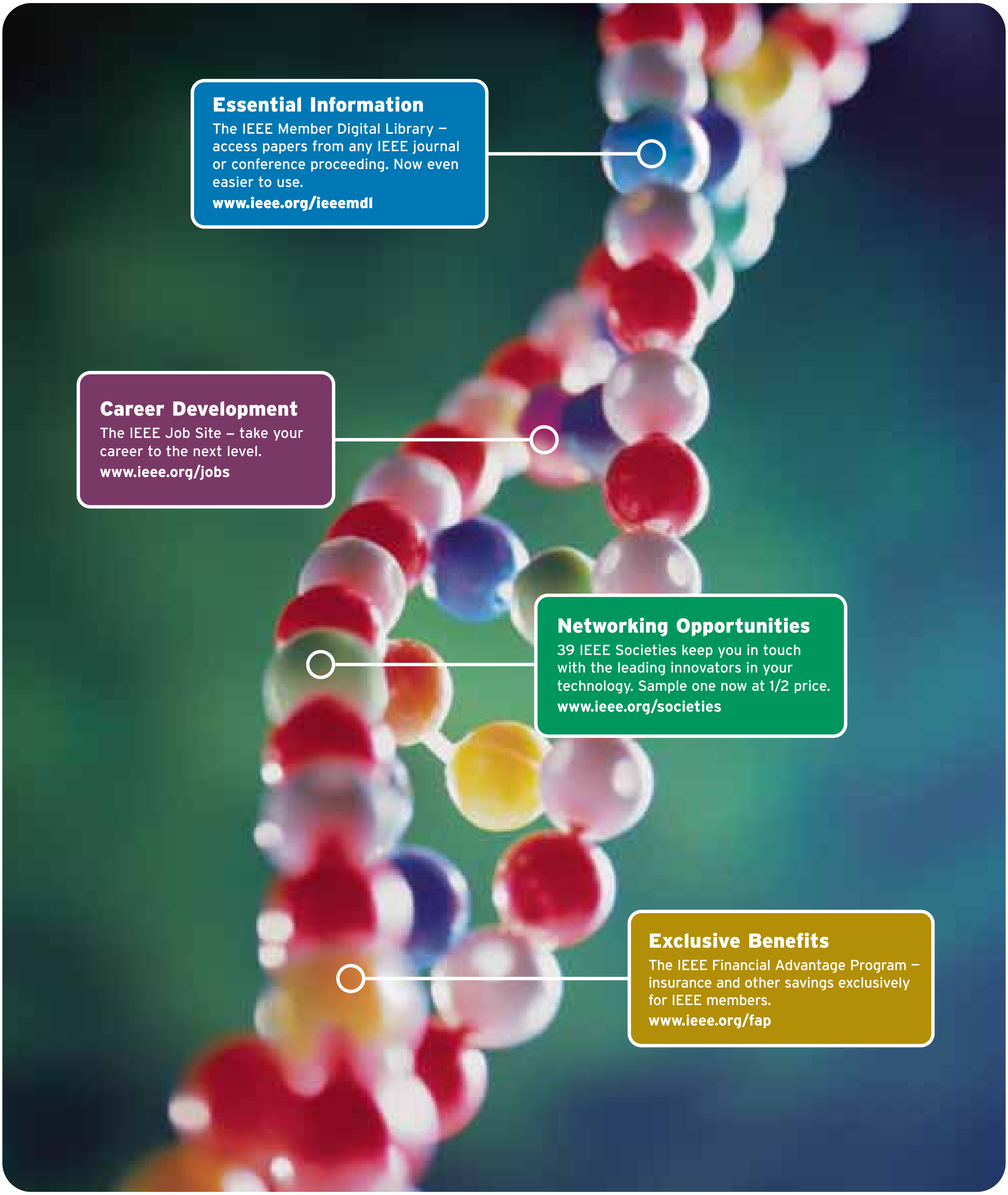
More than 6,000 Courses from Academic and Private Institutions Boost Professional Development

For those looking for a more robust educational experience such as a longer online course or a more traditional classroom setting, the IEEE Education Partners Program can prove helpful in your search for continuing professional development opportunities. Exclusive for IEEE members, it provides access to more than 6,000 on-line courses, certification programs, and graduate degree programs at up to a 10% discount from academic and private providers that IEEE has peer reviewed to accept into the program. To review the current list of partners participating in the program visit www.ieee.org/web/education/partners/eduPartners.html

IEEE Continuing Education Units (CEUs) Convert into Professional Development Hours (PDHs)

Another way to browse for a course or educational events taking place in your area is through the courses registered with IEEE to offer CEUs. To review what's available in your area visit www.ieee.org/ web/education/ceus/index.html. IEEE is an Authorized provider of CEUs through the International Association for Continuing Education and Training, as well as an authorized provider of CEUs for the Florida State Board. IEEE CEUs are also accepted by the New York State Board and can easily be converted into PDHs. One CEU is equal to 10 contact hours of instruction in a continuing education activity. IEEE CEUs readily translate into Professional Development Hours (PDHs) (1 CEU = 10 PDHs).

For more general information on IEEE's Continuing Education products and services, visit www.ieee.org/web/education/home/index.html. Specific inquiries can be directed to Celeste Torres via email, c.torres@ieee.org or by phone +1 732 981 3425.



Solid-State Circuits Society Newsletter Advertising Sales Offices

445 Hoes Lane, Piscataway NJ 08854
www.ieee.org/ieeemedia

Impact this hard-to-reach audience in their own Society publication. For further information on product and recruitment advertising, call your local sales office.

MANAGEMENT
James A. Vick
Staff Director, Advertising
Phone: 212-419-7767
Fax: 212-419-7589
jv.ieeemedia@ieee.org

Susan E. Schneiderman
Business Development Manager
Phone: 732-562-3946
Fax: 732-981-1855
ss.ieeemedia@ieee.org

Marion Delaney
Advertising Sales Director
Phone: 415-863-4717
Fax: 415-863-4717
md.ieeemedia@ieee.org

PRODUCT ADVERTISING
Midatlantic
Lisa Rinaldo
Phone: 732-772-0160
Fax: 732-772-0161
lr.ieeemedia@ieee.org
NY, NJ, PA, DE, MD, DC, KY, WV

New England/Connecticut
Stan Greenfield
Phone: 203-938-2418
Fax: 203-938-3211
sag.ieeemedia@ieee.org
CT

New England/Eastern Canada
Jody Estabrook
Phone: 978-244-0192
Fax: 978-244-0103
je.ieeemedia@ieee.org
ME, VT, NH, MA, RI
Canada: Quebec, Nova Scotia, Newfoundland, Prince Edward Island, New Brunswick

Southeast
Bill Holland
Phone: 770-436-6549
Fax: 770-435-0243
bh.ieeemedia@ieee.org
VA, NC, SC, GA, FL, AL, MS, TN

Midwest/Central Canada
Dave Jones
Phone: 708-442-5633
Fax: 708-442-7620
dj.ieeemedia@ieee.org
IL, IA, KS, MN, MO, NE, ND, SD, WI
Canada: Manitoba, Saskatchewan, Alberta

Midwest/Ontario, Canada
Will Hamilton
Phone: 269-381-2156
Fax: 269-381-2556
wh.ieeemedia@ieee.org
IN, MI. Canada: Ontario

Ohio
Joe DiNardo
Phone: 440-248-2456
Fax: 440-248-2594
jd.ieeemedia@ieee.org
OH

Southwest
Steve Loerch
Phone: 847-498-4520
Fax: 847-498-5911
sl.ieeemedia@ieee.org
AR, LA, TX, OK

So. California/Mountain States
Marshall Rubin
Phone: 818-888-2407
Fax: 818-888-4907
mr.ieeemedia@ieee.org
HI, AZ, NM, CO, UT, NV, CA 93400 & below

Northern California/Western Canada
Peter D. Scott
Phone: 415-421-7950
Fax: 415-398-4156
ps.ieeemedia@ieee.org
AK, ID, MT, WY, OR, WA, CA 93401 & above
Canada: British Columbia

Europe/Africa/Middle East
Heleen Vodegel
Phone: +44-1875-825-700
Fax: +44-1875-825-701
hv.ieeemedia@ieee.org
Europe, Africa, Middle East

Asia/Far East/Pacific Rim
Susan Schneiderman
Phone: 732-562-3946
Fax: 732-981-1855
ss.ieeemedia@ieee.org
Asia, Far East, Pacific Rim, Australia, New Zealand

RECRUITMENT ADVERTISING
Midatlantic
Lisa Rinaldo
Phone: 732-772-0160
Fax: 732-772-0161
lr.ieeemedia@ieee.org
NY, NJ, CT, PA, DE, MD, DC, KY, WV

New England/Eastern Canada
John Restchack
Phone: 212-419-7578
Fax: 212-419-7589
j.restchack@ieee.org
ME, VT, NH, MA, RI
Canada: Quebec, Nova Scotia, Prince Edward Island, Newfoundland, New Brunswick

Southeast
Thomas Flynn
Phone: 770-645-2944
Fax: 770-993-4423
ft.ieeemedia@ieee.org
VA, NC, SC, GA, FL, AL, MS, TN

Midwest/Texas/Central Canada
Darcy Giovingo
Phone: 847-498-4520
Fax: 847-498-5911
dg.ieeemedia@ieee.org;
AR, IL, IN, IA, KS, LA, MI, MN, MO, NE, ND, SD, OH,
OK, TX, WI. Canada: Ontario, Manitoba, Saskatchewan, Alberta

West Coast/Southwest/Mountain States
Tim Matteson
Phone: 310-836-4064
Fax: 310-836-4067
tm.ieeemedia@ieee.org
AZ, CO, HI, NV, NM, UT, CA, AK, ID, MT, WY, OR, WA. Canada: British Columbia

Europe/Africa/Middle East
Heleen Vodegel
Phone: +44-1875-825-700
Fax: +44-1875-825-701
hv.ieeemedia@ieee.org
Europe, Africa, Middle East

Three Advanced Engineering Courses

JACK BASKIN SCHOOL of ENGINEERING
UNIVERSITY OF CALIFORNIA, SANTA CRUZ

MEAD Microelectronics Inc.

Course Location

Courses will be held **March 24-28, 2008** at the
University of California Santa Cruz
Jack Baskin Engineering Building
Santa Cruz, CA 95064

The courses are jointly organized with the John Baskin School of Engineering of the University of California, Santa Cruz.

For additional information contact:

MEAD Microelectronics, Inc.
7100 NW Grandview Drive
Corvallis, Oregon, 97330
Telephone: (541) 758-0828
Fax: (541) 752-1405
Email: valence@mead.ch (technical questions) or
usmead@cmug.com (administrative questions)

For programs, fee and registration information, please visit our web site: www.mead.ch

Deadline for early registration is February 15, 2008

The schedules given here are based on information available a the time of printing. MEAD Microelectronics reserves the right to make modifications in the program if necessary.

1. Low-Power, Low-Voltage Analog IC Design

Monday, March 24

E. Vittoz	• MOS Transistor Modeling for Low-Voltage and Low-Current Circuit Design • Limits to Low-Voltage, Low-Power Analog Design • Basic Low-Voltage, Low-Power Circuit Techniques

Tuesday, March 25

W. Sansen	• Stability of Operational Amplifiers • Systematic Design of Low-Power Operational Amplifiers • Important Opamp Configurations • Fully-Differential Operational Amplifiers

Wednesday, March 26

W. Sansen	• Low-Power/Low-Voltage Design in Submicron CMOS • Rail-to-Rail Input and Output Amplifiers • Low-Power Design for Inductive and Capacitive Input Sources • Bandgap and Current Reference Circuits

Thursday, March 27

W. Sansen	• Distortion in Elementary Transistor Circuits • Low-Power Continuous-Time Filters
M. Pelgrom	• Matching of MOS Transistors in Deep Submicron Technology

Friday, March 28

M. Pelgrom	• Layout Considerations in Mixed-Signal Circuit Design
K. Pedrotti	• Circuits for Energy Scavenging in Low Power Applications

2. Power Management

Monday, March 24

R. Redl	• DC-DC Converters, Topologies & Control Techniques • Converter Modeling and Feedback Loop Design • Microprocessor Power Supplies

Tuesday, March 25

P. Brokaw	• Bandgap References • Alternative Bandgaps and Applications
D. Maksimovic	• Fundamentals of Switched-Mode Power Supplies for Portable Applications

Wednesday, March 26

D. Maksimovic	• Control Techniques and Their Integrated Circuit Implementation for Switched-Mode Converters in Portable Applications • Adaptive Power Management Techniques for Portable Applications
T. Szepesi	• Battery Charging Techniques & Circuits for Notebook Computers & Cellular Phones

Thursday, March 27

R. Blauschild	• Transistor-Level Off-Line DC-DC Controller Design
V. Ivanov	• Power CMOS and BCD Linear Amplifier Design • Circuit Techniques for Integrated Switching Regulators

Friday, March 28

J.Steensgaard	• Switched-Capacitor Power Supplies

3. Practical Approach to Delta-Sigma Design

Monday, March 24

G. Temes	• Introduction to Delta-Sigma ADCs and DACs
R. Schreier	• Second and Higher Order Single-Loop Modulators • Bandpass and Quadrature Delta-Sigma Modulation

Tuesday, March 25

J.Steensgaard	• Architectural and Topological Alternatives in Delta-Sigma Modulators • Design of Decimation and Interpolation Filters

Wednesday, March 26

G. Temes	• Delta-Sigma DACs - Theory & Design
I. Galton	• Mismatch-Shaping Multi-Bit D-S Modulators

Thursday, March 27

R. Schreier	• High-Level Design and Simulation • Design Examples
W. Sansen	• Low-Voltage Delta-Sigma Converters • Nanometer Delta-Sigma Design

Friday, March 28

R. Adams	• Theory vs. Reality: the Things That REALLY Affect Final Converter Performance • Unusual Applications of the Noise-Shaping Principle
R. Schreier	• CT Delta-Sigma Design

SSCS EVENTS CALENDAR

Also posted on www.sscs.org/meetings

SSCS SPONSORED MEETINGS

2008 ISSCC International Solid-State Circuits Conference
www.isscc.org
3– 7 February 2008
San Francisco, CA, USA
Contact: Courtesy Associates,
ISSCC@courtesyassoc.com

2008 Symposium on VLSI Circuits
www.vlsisymposium.org
19–22 June 2008
Honolulu, Hawaii
Paper deadline: Passed.
Contact: Phyllis Mahoney,
phyllism@widekehr.com

2008 Custom Integrated Circuits Conference
http://www.ieee-cicc.org/
21–24 September 2008
San Jose, CA, USA
Contact: Ms. Melissa Widerkehr, Conference Manager
19803 Laurel Valley Place
Montgomery Village, MD 20886
Phone: 301-527-0900 x 101
Fax: 301-527-0994
cicc@his.com

SSCS PROVIDES TECHNICAL CO-SPONSORSHIP

2008 International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA)
vlsidat.itri.org.tw
21 - 23 Apr 2008
Hsinchu, Taiwan
Contact: Ms. Stacey C.P. Hsieh
stacey@itri.org.tw

2008 Design Automation Conference
www.dac.com
9–13 June 2008
Anaheim, CA, USA
Paper deadline: Passed.
Contact: Kevin Lepine, Conference Manager
kevin@dac.com

2008 Radio Frequency Integrated Circuits Symposium
www.rfic2008.org
15–19 June 2008
Atlanta, GA
Paper deadline: Passed.
Contact: Mr. Stephen Lloyd
lloydsl@ieee.org

2008 IEEE Symposium on VLSI Technology
www.vlsisymposium.org
19–22 June 2008
Honolulu, Hawaii
Paper deadline: Passed.
Contact: Phyllis Mahoney, *vlsi@vlsisymposium.org*
or Business Center for Academic Societies, Japan,
vlsisymp@bcasj.or.jp

Hot Chips
www.hotchips.org
3-8 Aug 2008
Palo Alto, CA, USA
Paper deadline: 24 March 2008
Contact: John Sell, *info2007@hotchips.org*

ISLPED International Symposium on Low Power Electronics and Design
www.islped.org/
Aug 2008
Contact: Diana Marculescu
dianam@ece.cmu.edu

ESSCIRC/ESSDERC 2008 - 38th European Solid State Circuits/Device Research Conferences
www.esscirc2007.org
15 Sep - 19 Sep 2008
Edinburgh, Scotland
Paper deadline: 5 April 2008
Contact:Bill Redman-White, ESSCIRC Chair
bill.redman-white@nxp.com

2008 IEEE Integrated Circuit Ultra-Wide Band ICUWB
www.icuwb2007.org
10-12 Sep 2008
Hannover, Germany
Paper deadline: 10 February 2008
Contact: Michael Y.W. Chia
chiamichael@i2r.a-star.edu.sg

2008 IEEE Bipolar/BiCMOS Circuits and Technology Meeting - BCTM
www.ieee-bctm.orgA
14-16 Oct 2008
Monerey, CA
Paper deadline: 17 March 2008
Contact: Ms. Janice Jopke
ccs@mn.rr.com

2008 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)
www.csics.org
12 Oct - 15 Oct 2008
Monterey CA
Paper due date: 12 May 2008
Contact: William Peatman
wpeatman@anadigics.com

2008 International Conference on Computer Aided Design (ICCAD)
9-13 November 2008
Place: TBD
Contact: Kathy MacLennan, Conference Manager
MP Associates, Inc.
5405 Spine Rd., Ste. 102
Boulder, CO 80301
Tel: (303) 530-4562
kathy@mpassociates.com

SSCS IEEE SOLID-STATE CIRCUITS SOCIETY NEWS is published quarterly by the Solid-State Circuits Society of The Institute of Electrical and Electronics Engineers, Inc. Headquarters: 3 Park Avenue, 17th Floor, New York, NY 10016-5997. $1 per member per year (included in society fee) for each member of the Solid-State Circuits Society. This newsletter is printed in the U.S.A. Application to mail Periodicals postage rates is pending at New York, NY and at additional mailing offices.

Postmaster: Send address changes to SSCS IEEE Solid-State Circuits Society News, IEEE, 445 Hoes Lane, Piscataway, NJ 08854. ©2008 IEEE. Permission to copy without fee all or part of any material without a copyright notice is granted provided that the copies are not made or distributed for direct commercial advantage and the title of publication and its date appear on each copy. To copy material with a copyright notice requires specific permission. Please direct all inquiries or requests to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. Tel: +1 732 562 3966.

To maintain all your IEEE and SSCS subscriptions, email address corrections to *address-change@ieee.org*
To make sure you receive an email alert, keep your email address current at *sscs.org/e-news*

445 Hoes Lane
Piscataway, NJ 08854