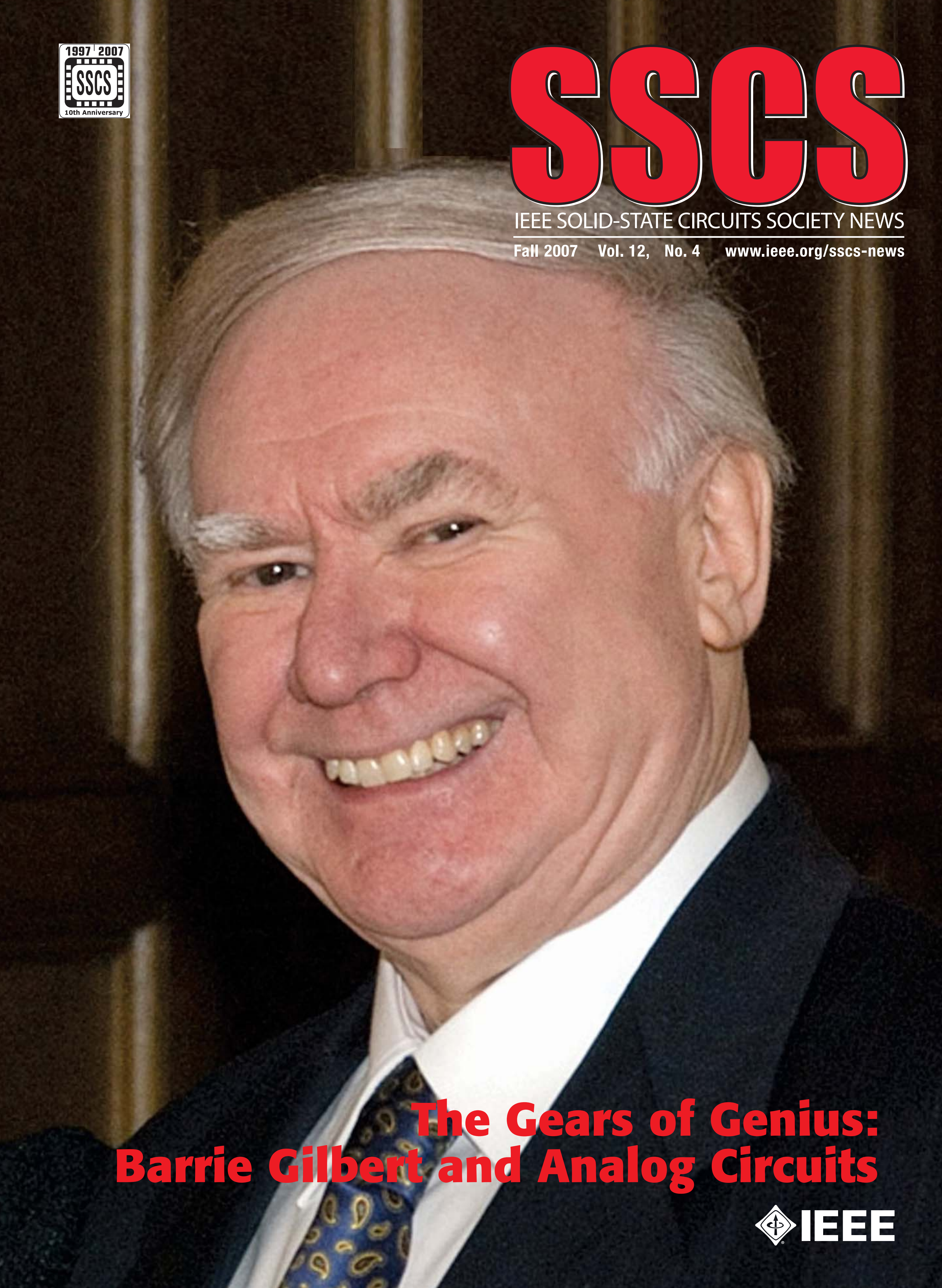

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IEEE SOLID-STATE CIRCUITS SOCIETY NEWS

Fall 2007 Vol. 12, No. 4 www.ieee.org/sscs-news

The Gears of Genius: Barrie Gilbert and Analog Circuits

IEEE

Editor's Column

Welcome to the Fall, 2007 issue of the Solid-State Circuits Society Newsletter! We appreciate all of your feedback on our first four issues featuring The Technical Impact of Moore's Law, The Impact of Dennard's Scaling Theory, The Origins of the Integrated Circuit, and The 40th Anniversary of Amdahl's Law. Thank you for your support of our efforts!

This issue is the fourth of 2007, and completes the inaugural year of our quarterly series. The SSCS News is published annually (one issue each in Winter, Spring, Summer, and Fall). The goal of every issue is to be a self-contained resource, with background articles (that is, the 'original sources') and new pieces by experts who describe the current state of affairs in technology and the impact of the classic papers and/or patents.

This issue contains one Research Highlights article:

(1) "The Silicon that Moves and Feels Small Living Things," by Donhee Ham and Robert M. Westervelt of Harvard University in Cambridge, MA.

The theme of this issue is "The Gears of Genius: Barrie Gilbert and Analog Circuits." Three feature articles discuss this theme:

(1) "The Gears of Genius," by Barrie Gilbert;

(2) "Tales of the Continuum: A Subsampled History of Analog Circuits," by Thomas Lee of Stanford University;

(3) "A History of the Continuously Innovative Analog Integrated Circuit," by Ian Young of Intel Corporation.

We reprint this original article in this issue (the fifth most cited article of all time in JSSC):

(1) Barrie Gilbert, "The Gilbert Cell, the Linear Mixer with Gain, in CMOS or Bipolar," IEEE JSSC, 1968

Thank you for taking the time to read the SSCS News. We appreciate all of your comments and feedback! Please send comments to myl@us.ibm.com.

Letters to the Editor

To the Editor,

I came across the website of IEEE SSCS News while browsing on the Internet, about a month ago. In my first encounter with your Newsletter, I was thrilled to discover in the last issue Amdahl's classic article reprinted 40 years after its original publication! Indeed, Amdahl's law has brought a completely new approach to analyzing parallel computer performance and has been recognized as one of the great achievements in our profession since the invention of electronic digital computing.

In my view, however, the most valuable contribution of the July 2007 issue is Gene Amdahl's new paper, which gives an overview of his professional career, going back to his achievements and describing for the first time some more details of his talk and the heated discussions that followed at the 1967 Spring Joint Computer Conference in Atlantic City. This article which will probably become as popular as

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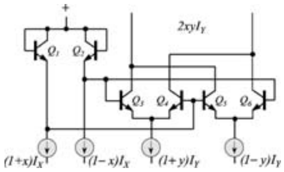

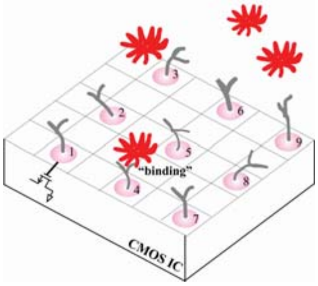

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NEWS

The Silicon that Moves and Feels Small Living Things

Donhee Ham and Robert M. Westervelt, Harvard University, Cambridge, MA 02138, donhee@seas.harvard.edu

Silicon microelectronic chips that make today's computers possible are emerging as powerful new tools for rapid and sensitive analysis of small biological objects, including cells, proteins, DNA, and viruses. The interface between electronic systems & biological systems is aimed at revolutionary advances in the life sciences and human healthcare, e.g., early cancer detection.

The present article is an attempt to share some exciting developments in this burgeoning area with this newsletter's readership. A large amount of high quality research is being done in the field. Therefore, the selected topics and references are far from being exhaustive, but we think they are examples which comprise an effective exposure to the field.

How does one go about interfacing solid-state circuits with squishy biological objects? The theoretical underpinning is that biological entities possess inherent electric properties (DNA carries intrinsic charges; cells are dielectric; nerve cells fire electrical pulses; etc.) and also that biological species can be attached to certain molecules or artificial particles of pronounced electric or magnetic characters. It is these electric or magnetic properties with which silicon circuitries can be structurally and functionally configured to interact. To gain one concrete picture for this broad and very widely applicable statement, let us begin our brief journey into this field with one of the most fascinating silicon-biology interfaces, *electronic DNA microarrays*.

Electronic DNA microarrays

DNA contains and issues the language of life. It gives cells instructions for living, and tells living organisms about their hereditary traits. This language is coded into the DNA's famous double helix structure: Fig 1(a). Each helical strand exhibits a sequence of four chemical bases, adenine (A), guanine (G), cytosine (C), & thymine (T), e.g., CAAGTG. The two twisted strands are bound together by pairing base A always with base T, and G always with C. Due to this pairing rule, within any section of DNA, once the sequence of one strand is identified, that of the other strand is easily inferred: e.g., the complementary sequence of CAAGTG is GTTCAC. DNA sequences are the language of life. Reading them, therefore, is of prime importance.

Electronic DNA microarrays are CMOS integrated circuits (ICs) that can rapidly decipher unknown DNA sequences [1-6]. A double-stranded DNA molecule can unzip into two complementary strands. A single-stranded DNA molecule thus obtained can bind back to its complementary sequence (either the old mate or a new one), forming again a double-stranded DNA molecule. This binding of two complementary strands, or *hybridization*, underlies the genetic sequencing operation of the electronic DNA chip.

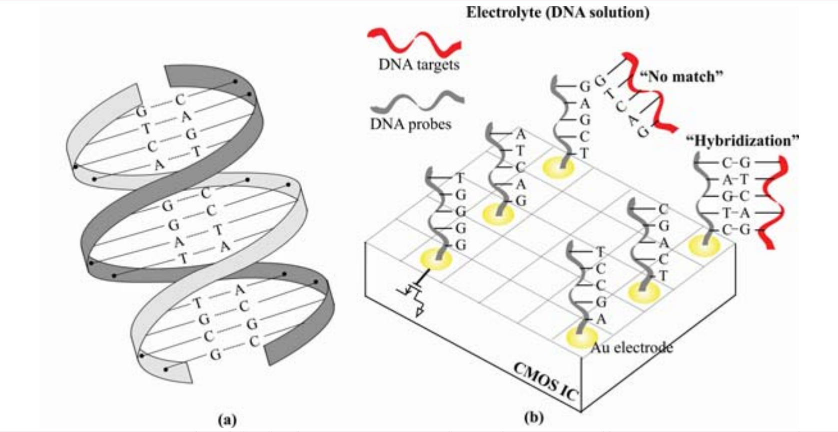

Fig. 1: (a) DNA's double-helix structure. (b) Schematic illustration of an electronic DNA microarray.

The electronic DNA microarray is constructed by immobilizing single-stranded DNA molecules of different identified sequences onto different grid points on a CMOS IC [Fig. 1(b)]. The grid points are often defined by post-fabricated gold electrodes that are electrically connected to the underlying CMOS IC. Different grid points represent distinct DNA sequences. These single-stranded DNA molecules of known sequences making up the array are called *DNA probes*. Now consider single-stranded DNA molecules of an unknown sequence, or *DNA targets*. When a solution of DNA targets is introduced onto the DNA array, the target strands wander around to eventually hybridize to their complementary probe strands at a specific grid point [Fig. 1(b)]. Locating the hybridization position reveals the target sequence, for we already know the probe sequence at that position, which must be complementary to the target sequence. The CMOS IC underneath is used for electronic detection of the hybridization point.

One well-established electronic detection technique is to label DNA targets with reporter molecules of a distinctive electronic signature and to search for them. Redox enzymes are an example of such electronic labels. If a voltage is suddenly applied between an electrode where hybridization occurred and the electrolyte (DNA target solution), redox labels attached to target molecules will give up electrons to the electrode, thereby increasing the current through the electrode. The same voltage step in an electrode with no hybridization would cause no such current increase as redox labels are absent at that electrode. By applying the voltage step and monitoring current change fast across the whole array using the underlying IC, hybridization positions are rapidly detected, leading to target sequence identification. Redox-label-based CMOS DNA chip examples are found in [1-3].

While the label-based detection

offers excellent sensitivity, significant efforts are being placed to develop label-free electronic DNA microarrays [4,5] because elimination of labeling steps would simplify the sample preparation. In [4], for example, the capacitance of an electrode immersed in the electrolyte is monitored to sense hybridization. No labeling is needed, as target strands added to an electrode during hybridization naturally lead to a dielectric constant change, or, capacitance change.

Field effect transistors (FETs), the basic commodity of CMOS ICs, can be also used *directly* for label-free electronic detection of DNA hybridization [7-9]. Underlying this sensing modality is the exploitation of the impact of DNA's intrinsic negative charges upon the FET behavior. Imagine that underneath the DNA array there is a corresponding FET array integrated in the CMOS IC. The gate dielectric of each FET is linked to DNA probe strands of the same sequence in a corresponding site in the DNA array. When a target strand hybridizes to its complementary probe strand anchored to a specific FET gate, the target's intrinsic charge alters the channel conductance and capacitance of the FET. Therefore, by monitoring the channel of each FET in the array, one can attain label-free electronic readout of target sequences. While field effect sensors per se are widely used [9], there is a lot of room for development in their use in DNA microarrays. Post-processing to expose gate dielectrics to electrolyte may pose a challenge. The smallest possible FET width must be used to maximize the impact of the DNA's charge on channel properties.

Hybridization is at the heart of many other DNA sequencing techniques. What makes electronic DNA microarrays unique is their massively parallel operation. Distinct probe sequences numbering as many as hundreds of thousands can be simultaneously available across an array. The CMOS IC monitors each site of the array fast across at a gigahertz speed, and hence, its operation may be regarded as parallel to human eyes. This parallelism allows for rapid collection of vast amounts of genetic information (far faster than non-microarray techniques), accelerating the speed at which we probe the secrets of living organisms. The parallelism is a direct outcome of using CMOS microfabrication techniques to build large microarrays, and is enhanced by the use of integrated electronics.

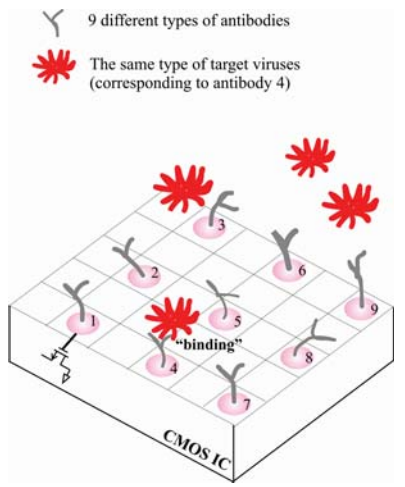

Fig. 2: Schematic illustration of a CMOS biosensor microarray to detect viruses.

In the original invention, which is still the commercially dominant form of the DNA microarray, hybridization is sensed by optical means [10]: fluorescent dyes labeling target strands light up upon illumination, reporting hybridization points. This optical machine boasts sensitivity superior to, and parallelism similar to, its much smaller electronic cousin. Although considerable work is needed to develop a high-performance electronic DNA chip as an alternative to the optical type, decisive advantages of using ICs (small size, low cost, programmability, real-time, label-free options) are the cogent reason for the ever-growing efforts in the development of electronic DNA chips.

Other electronic biosensor microarrays

Generalizing the concepts of the electronic DNA chip, one can readily consider CMOS biosensors that can detect other biological objects such as viruses and disease marker proteins [11]. Just like a DNA strand sticks specifically to its complementary strand, a virus or a protein binds specifically to its unique biochemical mate, an antibody. This highly specific binding is analogous to the way different keys fit into different locks. Fig. 2 illustrates a scenario where nine different types of viruses can be detected by using an array of nine specifically corresponding types of antibodies. When the array is exposed to a target solution containing type-4 viruses, for instance, the viruses will specifically bind to antibodies in array point 4. This binding can be detected using the CMOS IC below in much the same ways DNA hybridization is detected. By reading the location of the binding, the presence and type of viruses are determined. The multiplexed array platform can be especially useful for the diagnostics of complex diseases like cancer, where samples should be screened for multiple disease markers.

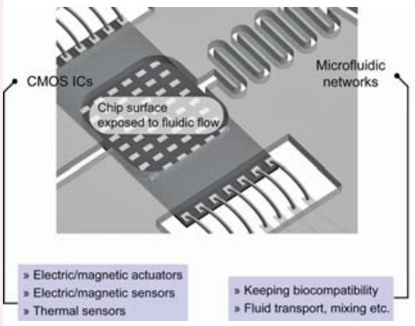

Fig. 3: Conceptual illustration of a CMOS/microfluidic hybrid system.

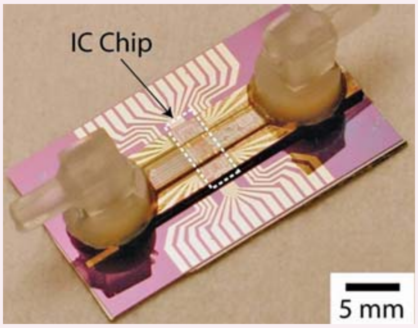

Fig. 4: Our first IC/microfluidic hybrid prototype.

One relevant design goal of electronic microarrays to sense viruses and disease marker proteins should be to maximize the ultimate sensitivity, because such capabilities would enable early disease detection when the pathogens are still sparse, which is of central importance in medical diagnostics. As transistors continue to become smaller with the scaling of CMOS technology, such ultra sensitive biosensors will become very feasible especially in the form of field effect sensors.

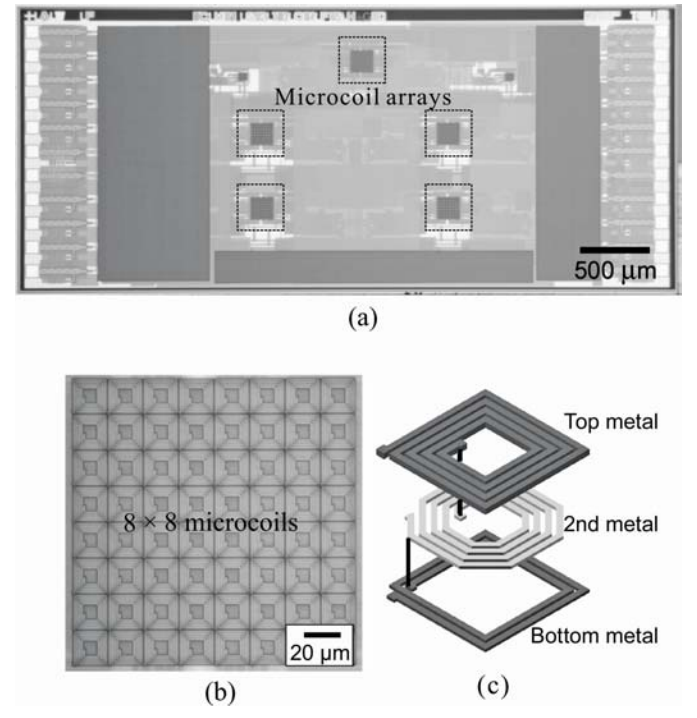

Fig. 5: (a) CMOS microcoil array IC. (b) Microcoil array close-up. (c) Schematic depiction of a single microcoil.

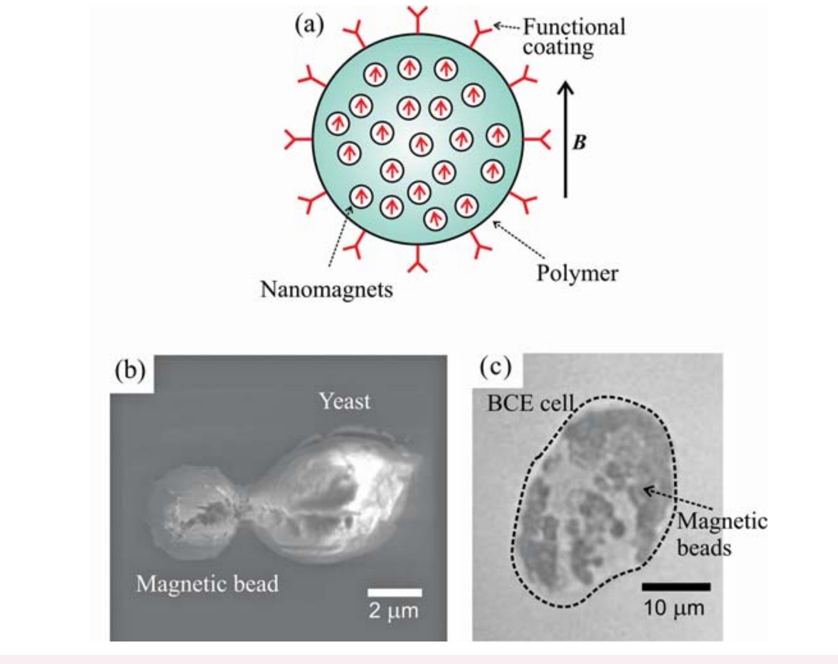

Fig. 6: (a) Illustration of a magnetic bead. (b) Yeast cell attached to a magnetic bead. (c) BCE cell that has engulfed multiple magnetic beads.

CMOS/microfluidic hybrid system

We have seen how solid-state circuits can be electrically interfaced with biological systems for their analysis. To make all this possible, however, biological systems ought to be introduced and maintained on top of a CMOS IC in a wet, biocompatible environment. Preserving a sample drop on the chip using a glass cover is one way, and it works out well for a variety of experiments as seen in many papers. Placing a microfluidic system on top of the CMOS IC, however, represents a superb approach. It allows valve-controlled precision for the introduction & removal of samples, consistent sustenance of biocompatibility, sophisticated flow control for sample mixing, reaction, & separation, and robust system packaging.

Together our two groups systematically developed such a hybrid system combining a microfluidic system on top of a CMOS IC [12-15]. Fig. 3 is a conceptual illustration of the hybrid system. Fig. 4 shows our first hybrid prototype used for magnetic actuation of cells [12] as discussed shortly. We refer interested readers to [16] for our recipes in fabricating microfluidic systems on CMOS ICs.

So far we have focused on using CMOS ICs for electronically "feeling" bio objects. We will now venture into new territory, exploring how to "move" biological cells, in the course of which we will introduce magnetic labels to attach to bio objects. We will later return to the business of sensing, but this time using the magnetic labels in conjunction with magnetic resonance.

Magnetic manipulation of biological cells

The ability to simultaneously control the motions of multiple individual cells along different paths with tight spatial control is desired for complex cell sorting operations. Such ability may also enable new types of investigations in systems biology, e.g., one can assemble an artificial microscale tissue by bringing together cells one by one into a desired geometry.

Various means are used to actuate cells, but simultaneous & independent addressing of individual cells with tight position control is not easy. For example, optical tweezers boast high-precision, 3D control of single cells, but are not suitable for handling multiple cells simultaneously. For another example, one can pull many cells attached to magnetic beads along the same direction using a magnetic tweezer (elongated electromagnet with a sharp tip), but control resolution is low and parallel manipulation of individual cells along different paths is difficult.

To attain the capability to simultaneously move multiple individual cells along different paths with tight position control, together our groups developed integrated *microcoil array* circuits within the CMOS/microfluidic hybrid structure

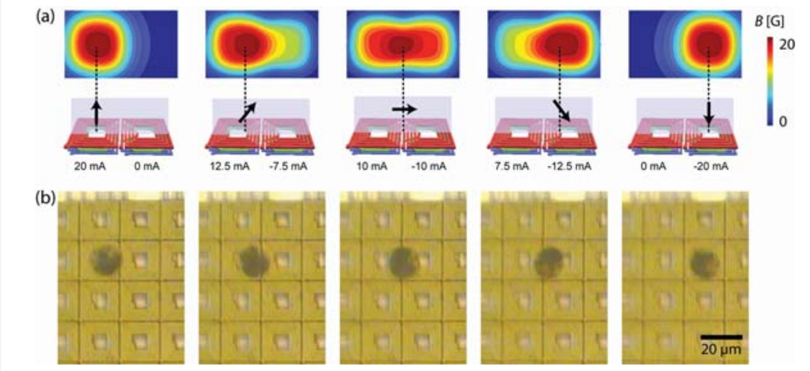

Fig. 7: 2-coil manipulation example: (a) Calculated field patterns for different current distributions. (b) Corresponding experiment using a single BCE cell. Reprinted from [15] with permission of the Royal Society of Chemistry.

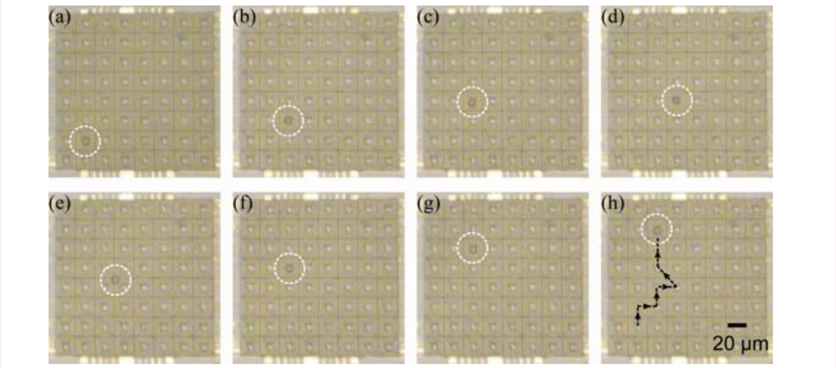

Fig. 8: Manipulation of a single magnetic bead. The alphabetical subfigure indices (a) through (h) represent images at different times, in chronological order.

[12-15]. The CMOS IC consists of a microcoil array and its control electronics: Fig. 5 shows an example IC we built. When the current distribution in the microcoil array is given, the array produces a certain spatial pattern of microscopic magnetic fields. In a given field pattern, magnetic dipoles (e.g., magnetic beads we will discuss shortly) move towards local field magnitude peak positions and get trapped there. Now by changing the current magnitude and direction in each microcoil independently, the field pattern is reconfigured and magnitude peak positions are moved independently. Magnetic-bead-bound cells suspended inside the microfluidic system on top of the IC then can be transported along different paths simultaneously. The spatial manipulation resolution is set by the dimension of the microcoil, which can be made comparable to or smaller than most cells. The parallel operation of multiple microcoils is what enables independent addressing of individual cells. The programmability of the CMOS IC makes the manipulation versatile and efficient. The detailed design of microcoil array ICs can be found in [14,16].

A brief discussion of magnetic beads would be useful. A magnetic bead is a polymer microsphere containing nanomagnets [Fig. 6(a)]. When subject to a magnetic field, the nanomagnets line up and the bead develops a net magnetic moment. It is this magnetic moment that interacts with magnetic fields in our manipulation. The bead surface can be modified with antibodies for specific bindings to target objects, e.g., yeast [Fig. 6(b)]. Fig. 6(c) shows a bovine capillary endothelial (BCE) cell that has engulfed multiple beads (~ 250 nm).

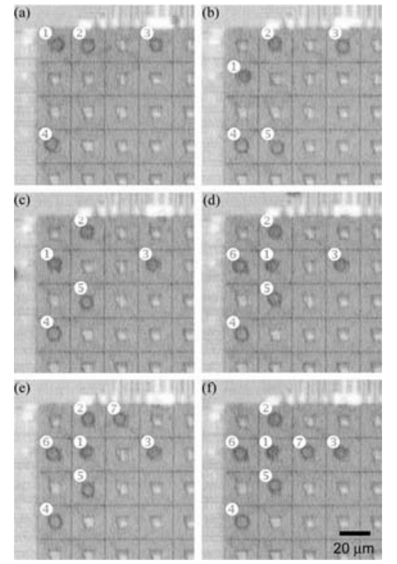

Fig. 9: Manipulation of multiple magnetic beads.

Figs. 7 ~ 10 show our magnetic manipulation experiments using the microcoil array IC [14, 15]. Fig. 7 elucidates the principle of magnetic manipulation with two microcoils. As current distribution changes, the calculated field peak moves from one coil to the other [Fig. 7(a)]. Fig. 7(b) is a matching experiment using a BCE cell. The cell rolls during the transport as the field direction also changes [Fig. 7(a)].

Fig. 8 shows the manipulation of a single magnetic bead (8.5 µm). By moving a field magnitude peak along a prescribed path, the bead was transported with an average speed of 11 µm/s subject to an average force of 40 pN.

Fig. 9 shows simultaneous independent manipulation of multiple beads to arrange them in a cross shape. One current source is shared sequentially in time among all coils to minimize power consumption [14]. This is possible

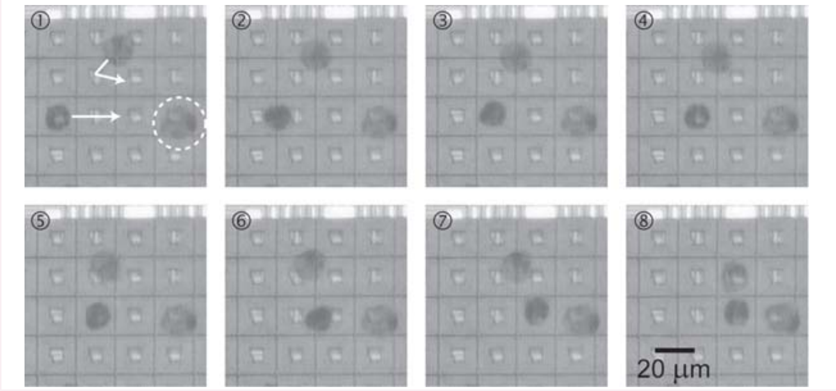

Fig. 10: Manipulation of multiple BCE cells.

because electronics are much faster than the motion of objects in fluid.

Fig. 10 shows manipulation of three BCE cells. The cell in the circle is held still; the rest cells are independently moved.

Electric manipulation of biological cells

In the same way that the spatially patterned magnetic fields move magnetic dipoles, spatially non-uniform electric fields produced by a microelectrode array can move dielectric objects (e.g., cells). Roberto Guerrieri's group at U. Bologna first implemented this *dielectrophoresis* in CMOS ICs [17]. We (the Westervelt group) also developed CMOS IC arrays in conjunction with a robust microfluidic system on top [18]. Depending on specific needs, a proper choice can be made between the electric and magnetic method. Each approach has advantages and disadvantages: while the magnetic method is more biocompatible as magnetic fields are transparent to cells, it requires more sample preparation steps (bead attachment).

Magnetic resonance based biosensors

Nanoscale magnetic beads (~ 30 nm) can be utilized for biosensing in a very fascinating way. Consider putting magnetic nanoparticles whose surfaces are modified with specific DNA strands into a bio-sample. If complementary strands exist in the sample, hybridizations occur and the magnetic nanoparticles self-assemble into clusters [Fig. 11(a)], as found by Ralph Weissleder's group at the Massachusetts General Hospital [19]. Similarly, magnetic nanoparticles coated with antibodies can self-assemble into clusters in the presence of specific target proteins [Fig. 11(b)]. This self-assembly can be detected using nuclear magnetic resonance (NMR) [19].

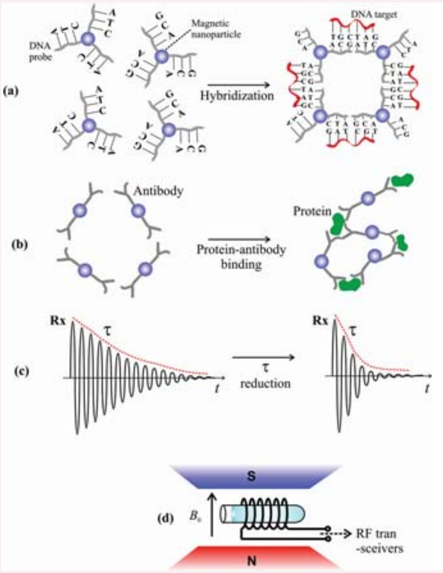

Fig. 11: Magnetic relaxation switch.

In a standard NMR experiment [Fig. 11(d)], nuclei spins within a sample (e.g., proton spins of hydrogen atoms within water) excited by a pulsed RF signal sent through the coil will initially precess about a common axis and at a common frequency, both of which are defined by the static magnetic field B_0. Spin-spin interactions, however, will interfere with this uniform precession, causing variations in precession frequencies among different spins. On a macroscopic average, the resultant loss of phase coherence manifests as an exponential relaxation (damping) in the precession of the net magnetic moment. During this precession and relaxation, the coil picks up a damped sinusoidal signal. The relaxation's characteristic time called T_2 is a measure of how fast coherence is lost.

The clusters (bigger magnets) that are formed from magnetic nanoparticles in the presence of target objects produce pronounced local magnetic fields that introduce spatial and temporal modulations on top of the static field B_0. This modulation introduces more precession frequency variations on top of those caused by the basic spin-spin interactions, accelerating the rate at which the system loses phase coherence. Therefore, the resultant reduction in the relaxation time T_2 [Fig. 11(c)] indicates the presence of target objects. This technique by Weissleder, which he aptly calls *magnetic relaxation switch*, is a new electronic biosensing modality [19,20].

Currently we (the Ham group with the Weissleder group) are miniaturizing the magnetic resonance biosensor [21,22]. Full NMR RF transceivers incorporating pulse-sequence techniques are integrated on CMOS ICs, along with an array of NMR microcoils. Again we encounter a microarray, whose effective operation is enabled by CMOS ICs. We believe that the sensitivity of our parallel NMR measurements of small divided samples on the microcoil array will dwarf that of the standard NMR measurement of one larger sample in statistically a very fascinating manner. Such high sensitivity would facilitate early disease detection.

CMOS biotechnology

With several implemented examples and feasible implementation ideas, we have illustrated how a CMOS IC can be utilized to electronically actuate and analyze micro and nanoscale biological objects in a sample placed on top. Here CMOS ICs play active roles in front-end sensing and actuation in direct contact with the biological world.

One powerful feature of the CMOS-bio interface uniquely derived from the use of CMOS technology is parallelism seen through various microarrays, combined with programmability. This enables rapid, sensitive, and selective detection and versatile actuation. Possibilities for label-free detection are an additional merit. As transistors become smaller with technology scaling, they will become more suitable for highly sensitive direct detection as field effect sensors. Sensitive front-end analog ICs will be an integral part of the CMOS-bio interface.

This field, which we call CMOS biotechnology, brings together various disciplines of engineering and science. There are many exciting developments, and we looked at only a small fraction of them, omitting fascinating subjects like neuron-CMOS interfaces [23-26] to study brain dynamics or to aid vision processes. Though limited, we hope this review has conveyed a meaningful perspective of this new fertile ground of research.

Contributors: Yong Liu and Hakho Lee enabled the magnetic manipulator work. Liu and Nan Sun in our group work with Lee, now at MGH with Weissleder, on the CMOS MR biosensor.

Acknowledgements: We thank William Andress of Harvard, Larry DeVito of ADI, NSF, and NIH for suggestions and supports.

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He received his B.S. degree in physics from Seoul National University, Korea, graduating with Presidential Honor at the top of the class in the Natural Science College in 1996, and his Ph.D. degree in electrical engineering from the California Institute of Technology, Pasadena, CA, in 2002, winning the Charles Wilts Doctoral Thesis Prize, best thesis award in electrical engineering. His doctoral work examined the statistical physics of electrical circuits. His work experiences include the Caltech-MIT Laser Interferometer Gravitational Wave Observatory (LIGO), 1997/1998, and the IBM T. J. Watson Research Center, 2000. He has been on IEEE conference technical program committees, including the International Solid-State Circuits Conference, and has held industry & government technical advisory positions on subjects including ultrafast solid-state electronics and science and technology at the nanoscale.

Donhee Ham was a fellow of the Korea Foundation for Advanced Studies and a recipient of the IBM Doctoral Research Fellowship. He is also the recipient of the IBM Faculty Partnership Award. He shared Harvard's Hoopes prize in 2003 with Mr. William Andress. He is a co-editor of CMOS Biotechnology (Springer, 2007).

Robert M. Westervelt received the Ph.D. degree in physics from UC Berkeley in 1977. Following a postdoctoral appointment at Berkeley, he moved to Harvard University, where he is currently the Mallinckrodt Professor of Applied Physics and Physics.

His group investigates the quantum behavior of electrons inside nanoscale semiconductor structures and develops tools for the manipulation of biological systems. Current research topics include: imaging electron flow through nanoscale devices at low temperatures using scanning probe microscopy, making artificial molecules composed of few-electron quantum dots for quantum information processing, and the development of hybrid integrated circuits/microfluidic chips to trap, move, assemble, and sort biological cells and small particles in fluids. He is Director of the NSF-funded Nanoscale Science and Engineering Center at Harvard University, which includes participants from the Massachusetts Institute of Technology, UC Santa Barbara, and the Museum of Science in Boston. Previously, Prof. Westervelt was Director of the Materials Research Science and Engineering Center, and Co-Director of the Joint Services Electronics Program at Harvard.

The Gears of Genius

Barrie Gilbert, IEEE Life Fellow, ADI Fellow

THE MIRACLE

The *Square and Compass* is a tiny pub – well, actually, the *only* pub – in the sleepy village of Worth Matravers, nestled high on the chalk cliffs along the Dorset coast, looking out over the English channel toward France. *The Coastal Hikers*' Guide says of this pub: "Fantastic place; geese running around; roaring log fires; best scenery in the world; the friendliest people; completely unspoiled; a gem". Whenever I make a trip back there, the salty ocean spray, borne up on summer zephyrs, feels just as it did on my face during an earlier time, when electronics and I were both very young.

One evening in 1940, this pub - called "The Sine and Cosine" by the TRE boys - was packed to capacity. Its rustic tranquility had been shattered by an influx of high-spirited workers from a secret research lab (TRE) nearby. They had good reason to be in a celebratory mood. Earlier in the day, Philip Dee, one of the engineers at this top-secret development site, and on war-time loan from the Cavendish Labs of Cambridge University, received an ordinary-looking package from Birmingham University. Its contents would have made an alert espionage agent crave for possession, had he known it contained two precious samples of a unique and radically different sort of microwave oscillator tube: an invention destined to sharpen the eyesight of the older Chain Home UHF radar stations scattered all around this coast during WW2, and radically shift the dynamics of this grim war [1].

Dee was filled with a mixture of awe, elation and anticipation tinged with concern as he carefully extricated one of these strange, awkward devices, sprouting metal pipes for cooling and vacuum pull-down, a rigid coaxial line for its output, and connections for DC power. What he held was quite unlike any other tube. For one thing, it didn't have a visible glass envelope, so the inner structure couldn't be seen; and it needed a powerful magnet, as well as hundreds of volts at several amps, to do its special thing. In essence, it was little more than an elaboration of the diode, the earliest and the simplest of all electron tubes; but that magnet introduced a thrilling twist!

The boffins up north had waxed ecstatic about its miraculous properties; fitting, since Britain needed a miracle. France had already fallen, and the bombing raids all across England were intense. Dee may have wondered "How can yet another type of valve change the outcome of this endless conflict?" He could not have foreseen, nor even could Robert Watson-Watt, credited as the 'father' of radar (he was later knighted for this work; his first, pre-magnetron system dreams on in the British Museum, Figure 1) how such a naively simple device could not only win a war, but that it would guide his seafaring through the darkest storm; that it would become a key to forecasting the weather and mapping the earth's terrain and resources; that it would one day cook our dinner in minutes rather than hours.

Figure 1: Sir Robert Watson-Watt's baby, dreaming contentedly in the British Science Museum of great days.

It was even less foreseeable that its cousins, the klystron family, harnessing swarms of electrons in a game of electromagnetic give-and-take called *bunching*, would one day be used by the score to accelerate particles almost to light speed in colliders, revealing layer upon layer of the complexity of matter as they hurtle, blind and thoughtless, head-to-head; and in an instant annihilate each other, leaving just assorted fragments; much as do people in war. It was beyond imagination's reach that another ingenious device, the traveling-wave tube, would be used to deliver movies produced and directed by lonely robots roving Mars; or conveniently supplying us with colorful coffee-table close-ups of Saturn's rings and Jupiter's moons; capturing visions of the awesome ever-humbling immensity of space through Hubble's eyes; or mailing the occasional postcard of some small, ignoble potato-objects boiling aimlessly in our star's asteroid belt, harboring inclinations to wipe out life on Earth, while a small radar silently measures our space-craft's closing distance, as we test our propositions to land on them, prod and poke them, and report back on the stuff they're made of.

These amazing electron tubes *profoundly changed the face of civilization*, fully as much as would a later remarkable electronic innovation. No, this was not the *accidental* discovery of minority-carrier conduction. In my own design experience, the debut of discrete commercial transistors (BJTs) only *modified* the paradigms of design and manufacture; just as, later, gluing together four or five components into an awkward, one-off, and rudimentary hybrid proved little and changed nothing. Rather, it would be a *truly revolutionary* invention: Jean Hoerni's planar process [2].

But for now, in 1940, the only vision that mattered was that of a new hawk-eyed radar; and this primitive new device (Figure 2a) held that promise. The basic form of its internal structure can be seen more clearly in a dismantled RAF magnetron from a later time (Figure 2b). We can imagine the excitement felt by Dee as he attached the heavy magnet to the steel flanges, with its focusing poles carefully aligned to the upper and lower ends of the rod-like cathode, thus creating an intense magnetic flux along its

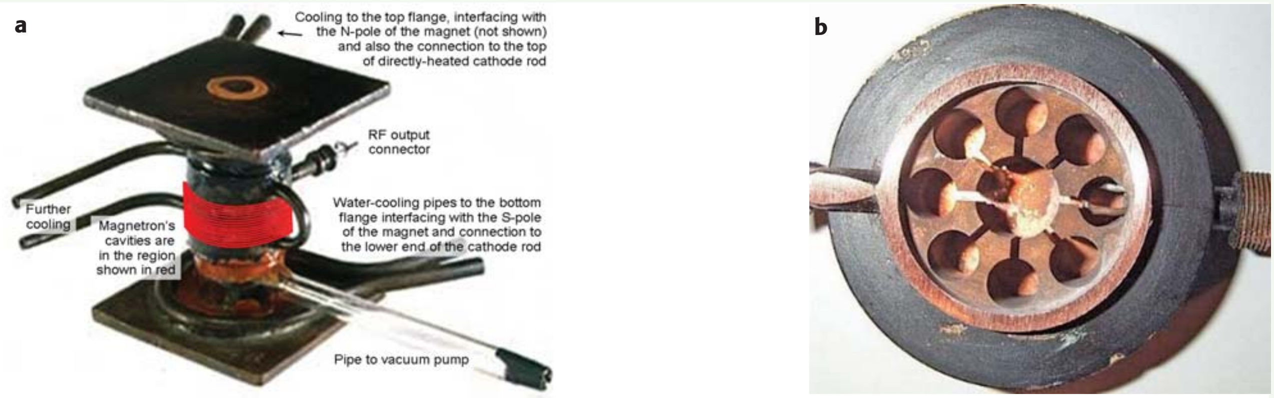

Figure 2: The cavity magnetron of Randall and Boot (now also in the British Science Museum) minus its magnet. (b) A production magnetron disassembled to reveal the resonator cavities in the anode block.

radial axis of symmetry. When pumped down to Birmingham's specified vacuum, he started the flow of cooling water, then applied the low voltage to heat the cathode, and made sure the anode was well-grounded. Finally, with trepidation, he applied the supply-voltage to the cathode; at first, perhaps only a hundred volts.

As Dee inched up the supply voltage it seemed nothing remarkable was happening, except the cooling water was becoming very hot. Then, at a critical voltage, he saw the magnetron burst into oscillation. Or rather, he noticed that the RF test load, a bank of five or six 100-W house lamps, began to glow. By the end of the day, using the full accelerating voltage recommended by its inventors, Randall and Boot, the microwave output was lighting up the laboratory like the sun, while the cooling water retreated to a much less threatening temperature. The cavity magnetron *really worked*!

The anode, a thick annulus of solid copper in which six cylindrical cavities had been milled, accelerated electrons radially outward from the cathode as in any ordinary diode. In the absence of a magnetic field these electrons would have hurtled directly to the anode, where they could only turn their energy (momentum) into useless heat (Figure 3a). But a magnetron is no ordinary diode: its magnet forces the electrons to follow a *strongly curved* path; and by adjusting the magnetic and electric fields, they can be made to arrive at the anode's inner wall traveling in an almost *circular* path, now carrying their high energy in a powerful, swirling electron tornado (Figure 3b).

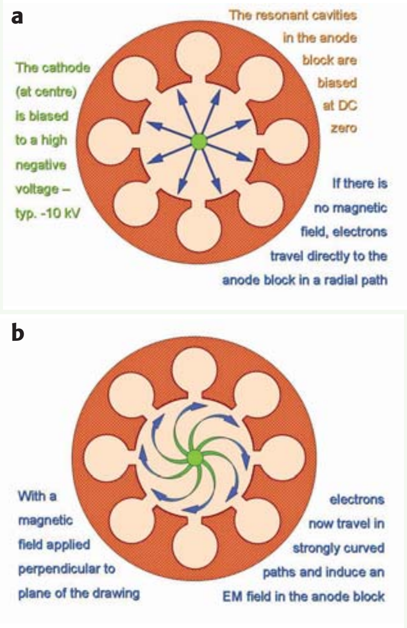

Figure 3: Electron flow in an 8-Cavity magnetron (a) without, and (b) with magnetic field applied.

Randall's theory predicted the cavities needed a diameter of ~1.2 cm to produce a 9.5-cm oscillation (f ≈ 3.2GHz). They act like *microwave whistles*: arriving electrons give up some of their energy as they *blow across* their open gaps, resulting in strong EM-fields in these high-Q resonators that interact with the constantly-refreshed supply of high-energy electrons, further reinforcing the RF power. This extraordinary behavior must have astonished Dee, as rather ordinary DC volts and amps were being converted *directly to pure microwave power*, and gushing out of its coupler like water off a roof during a tropical downpour. Great ingenuity had been poured into previous wondrous tubes, but nothing before the cavity magnetron had provided such power at these high frequencies – orders of magnitude greater than any previous source – and with unprecedented efficiency.

By pulsing the cathode supply at a moderate rate, very narrow pulses of enormous peak power could be generated. Soon, radars would be using magnetrons operating at 16 kV and an I_{PK} of 8 A, thus accepting 128 kW peak DC power, of which more than 50 kW was directly converted to RF. These extremely-short microwave pulses would resolve far smaller targets than possible with more primitive UHF radars. At a stroke the magnetron transformed radar in a way comparable to converting a pair of opera glasses into a space telescope. It was this prospect of super-accurate radar that had created such high hopes at TRE that summer evening in 1940, and provided an excuse for all the rowdy celebrations over at the pub.

A FEARFUL PROXIMITY

That same evening, barely far enough away to be insulated from the jubilance over at the *Square and Compass*, Frederick Arthur Gilbert, a serious and sensitive man, and an accomplished classical pianist, was diligently practicing a Beethoven sonata. A toddler, his third birthday just days before, squeezed alongside him on the black piano bench. He was doing his bit to contribute to the unfolding invention, exploring the cackling potential of the top octaves: *What If*? this key? *How About*? this black one? All the while his father's playing was weaving a complex tapestry of enigmatic infinite loops in this boy's head, creating a painful confusion: *What is music*?

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Two days later the piano, so recently joyful, was in mourning. The latest round of bombs that were intended to destroy the older UHF radar station at Ventnor, on the Isle of Wight, or perhaps put an end to the magnetron work at TRE, missed their target. Instead, they hit our home town. I was the top-octave augmenter: the last of his four children. By all the normal rules of nature, my mid-forties mother should have been excused from further childbearing. *Surprise*! On June 5, 1937, two days after the death of Sir James Barrie, the author of *Peter Pan*, I showed up.

So my father named me Barrie, celebrating the creator of this imaginary character, wishing the same for me: that I might never need to grow up, and be forced to develop my life in what was at the time threatening to become the foreign occupation of England. He didn't live to witness that dark prospect vanquished, or to play real duets with me, sharing our mutual joy of music-making like the chromatic soul-mates we doubtless would have been, perhaps striving to guide his new son to make a mark on the world stage as a concert performer. *What If?*

Largely because of radar, and the developments at TRE, a few miles from me, the War would eventually be won by the Allied forces. But in those dark years, I was fatherless and my mother was obliged to raise me and my siblings with zero income. Among our few assets was the piano. Not being musical, she soon sold it, to pay for necessities. So at a stroke I lost both my teacher and the beloved instrument that had once sung for my chubby fingers, as I added joyfully to the fluid sonorities miraculously emerging from my father's hands. My sole inheritance was a stack of sheet music. Some were his own hand-written compositions, but most were the works of the great composers, liberally annotated in the garish purple of the day's 'indelible' ink: *'Legato here'; 'Careful - sudden key-change'; 'Marked fff, but don't wake Barrie.'*

A month after my father's death, Aug. 12, 1940, a secret event took place that was nonetheless so relevant to my life that it might as well have been advertised in the *Swanage* Times or the *Bournemouth Daily Echo*. One of those primitive magnetrons bounced a tentative pulse off the walls of the Norman church at St. Aldhelm's Head, on the Dorset coast. Satisfied with this general test, and perhaps as a way to do some calibration, Dee's team turned the keen vision of their contraption toward a passing cyclist and later, a small aircraft miles out to sea. It was the first time a magnetron had been used in a radar system; and the first time an aircraft had been tracked by radar. While this constructive work was being pursued, three of the early-warning stations in Kent were again under attack; and a fourth, the one at Ventnor, was briefly put out of action later in the afternoon. More bombings of these stations were expected.

Inexplicably, Field Marshall Goering believed that these towers were of no great significance, and he redirected the bombing raids to inland targets, such as Coventry cathedral. The *Enigma* code had recently been cracked (with the help of the *first programmable digital computer,* 'Colussus,' designed by Tommy Flowers, whom I've had the pleasure of meeting) so Winston Churchill knew about this particular air-raid, but he couldn't tip his hand and reveal this knowledge. Many have said that if more attacks *had* been ordered, and those radar defenses were destroyed, the Battle of Britain would have been lost within one month. Instead, by July of 1941, the miraculous magnetron was doing its thing in Navy radar stations, and shortly thereafter, in RAF aircraft. Earlier, in great secrecy, samples had been shown to a group at MIT, and the US soon began to make their own magnetrons. By the time they showed up to aid Europe, their military craft were also equipped with radar.

A DEARTH OF MENTORS

In his autobiography [3] the anthropologist Oliver Sacks tells of a favorite uncle who encouraged his curiosity about the world around him during his childhood in the 1930's. This fellow, who owned a company that made light bulbs ("We once used osmium for filaments," he said), spent a lot of time with his young nephew, reveling in the magical properties of basic chemicals, especially crystals and metals. His admiration for one particular metal led Sacks to name this influential mentor Uncle Tungsten. At a recent MIT event ($H^2.O$), where Sacks happened to be the keynote speaker, we talked about early-life influences, and the enjoyment of our experiments in physics and chemistry. The closeness of our learning trajectories was remarkable, but the similarities ended there. Sacks was fortunate in having a highly attentive and supportive extended family of intellectuals and professionals, all of significant means. I had only my overburdened mother, freshly widowed by the insanity of war, and she was constantly broke. As the youngest of her four children, I wore ill-fitting hand-me-downs and repeatedly re-darned socks (a lost art in the consumerist West).

So when asked "*Who was your most influential mentor?*" I'm embarrassed (since many seem well-prepared – even eager – to amplify this theme) in having to reply that I can't recall there being anyone of that sort. I was a lone wolf-cub, befriended only by a hyperactive urge to experiment with everything. Without a father or an Uncle Tungsten, my childhood inspiration came largely from mile-long treks to the nearest library, where I found such deeply inspiring works as Robert Millikan's account of his painstaking experiments for determining the mass-to-charge ratio of the electron, and

"*Principles and Practices of Radar,*" by Penrose and Boulding.

Even before I could read, and for many years after my father died, I browsed the enigmatic pages of his stack of music, my only link to him, trying to make sense of their strange yet familiar symbols. Neither my mother nor my older siblings could help. So I became a loner, guided by my imagination, in the company of enigma, perplexity and hypotheticals. I began to formulate probing questions. *What If?* we had not lived so dangerously close to these radar stations, and TRE? *What If?* my father had lived? I felt sure my life should be devoted to music, in some performing capacity, and at an early age, I resolved to earn enough to purchase my own piano. I eventually did, at 18, paying by installments, and taught myself to play. Ironically, this playful instrument was made in Germany. I still have it, but I've since augmented my arsenal with two grand pianos (decked out as *Disklaviers*), and a farm of synthesizers, computers and perversely expensive audio equipment.

The magnetron was powerless to avert the appalling loss of life that occurred in London later in 1940, particularly during the incendiary bombings of the night of December 29. Not many years later, it was to be my good fortune to be inspired by the war's inventions. It was through *radar*, as much as anything else, that I got tangled up in electronics. *Radar became my inspiring mentor*. The linkage between its brilliant developments, during my childhood, and the numerous neat notions of my own during adult life are readily discernable. Thus, my explanation of how a magnetron works will seem familiar when I later describe a semiconductor device, invented at Tektronix in 1969, to which it bears an uncanny resemblance.

Such strong connections between creative events throughout one's life are surely commonplace; they are an aspect of what may be called the *continuity-of-concepts* principle – the fact that most of us have but a few seminal ideas, forged at an early age, from which we wring every ounce of utility. Sadly, few of today's young circuit designers, having acquired most of their knowledge from studies during school and university years, will have had the opportunity to be exposed to such a rich and varied set of formative experiences as were enjoyed by people of my age. The rare exceptions are the *practical experimenters*, tinkerers, who nowadays build robots with microprocessors for brains, using analog ICs for augmenting the acuity of their sensors and the precision of power-control for their actuators.

TRANSFORMING LOSS TO ADVANTAGE

But I've also learned, from conversations with people having a similar childhood, that inventive aptitudes often arise from the *transformative power of loss* – the shock of, say, no longer having the companionship of a parent during the critical formative years, for whatever reason; and is even aided by the *severely limited resources* associated with poverty. Hiro Moriyasu, a co-worker of mine at Tektronix, was a prolific inventor. This friend died in July, 2005. His obituary states that in 1974 "[*he created*] *one of the first personal computers, the Tektronix 4051, which caused IBM to take an earlier model off the market.*" As a boy, Moriyasu-san lived in Kure City, Hiroshima Prefecture, until the shameful day the US dropped the world's first atomic bomb, surely mankind's most hideous perversion of technology. It appears he hid in a farm truck during this terrible assault on the nearby community, and witnessed the incredible devastation first-hand. Because of this tragedy, he was raised by monks as an orphan. Luckily for Tektronix, he eventually became a first-class engineer.

Yet, it's not so very surprising that creativity may arise in adult life when the infant mind is faced with the *perplexing meaningless* of great loss. Forced to accept enigma as a normal and constant aspect of life, and limited by a *paucity of means*, the child develops *pragmatism* and *flexibility*. Lacking help in making sense of non-linguistic *symbolic representations*, he acquires intellectual resourcefulness and independence of spirit. Without the safe ingredients of a normal childhood, the young mind does not simply make *adjustments*, to restore *a neutral* outlook: it may over-compensate. It somehow manages to extract *strength from loss*, and gains the confidence to go it alone, fiercely vowing to be independent and copy no-one.

I find no reference to these ideas of *early loss, deprivation* or *limited means* in any of the scores of works in my own library concerned with creativity, nor certain other ideas about the wellsprings of invention; and although that's another story, here's a tiny hint. Cortical neurons are undoubtedly susceptible to electrochemical noise. What we call thinking is a stream of *controlled processes disturbed by stochastic mechanisms*. Significant departures from deterministic, logical thinking caused by such neural noise may be more meaningful to a mind familiar with – and even comfortable with – perplexity, enigma and the dialectic, than one developed during a highly-structured and well-provided childhood.

GROWING UP LEAN

By about 6 years old, I was making model airplanes from strips of wood salvaged from packing-cases, begged from the local grocer. One served as the fuselage; a second, nailed cross-wise, was the wing; and there may have been a tail of sorts. Later, I built many flying, floating and rolling machines; and I was also beginning to discover, through my own *What If?* experiments, how switches, lamps and batteries behaved when wired in various combinations. I made a game in which questions on one board were wired to their answers on another; completing the circuit through a wire placed on corresponding pads illuminated a lamp.

My curiosity soon embraced chemistry, initially using utensils and common reagents from the kitchen; and electrochemistry, using batteries borrowed from our rented radio-set. (Not having street electricity at that time, we used only gas-lights and candles, and the house was heated in winter by a small coal fire in one room. Often, as I got ready for school, the bathroom window would be coated with ice. I wondered: *Why*? do the layers on the *inside* surface make beautiful fern-like patterns?).

One day, I wondered: *What If*? I place a pair of wires into this salt solution and connect them to the 120-V "HT" battery. Watching my jam-jar at an incautious proximity, I observed the reluctantly-electrified liquid was generating a greenish slime and a cloud of gas. I had discovered chlorine. Incidentally, I repeated this "experiment" when at last we had street electricity, this time using sturdy copper plates wired directly (!) into a 240-V AC outlet. Luckily, the salt solution must not have been very strong, because it didn't explode. But the liquid boiled almost instantly, and green gas proliferated. *What If*? I smell this stuff, I asked. So I placed my nose close to the fuming haze of lethal gas. This was just one of many times during the next few years that I almost killed myself, by letting *curiosity* lead to *reckless disregard* for the punch behind a power outlet, or for the internal energy stressing the bonds in certain nervously-bound substances. It is not wise to idly seek answers to the *What If*? question using live ammunition!

At about 8, using the metal girders, plates, pulleys and gears of my growing Meccano set, I built bridges, Ferris wheels, tractors, robots and steam locomotives. None ever came from How-To books or magazines. It was an unspoken (and unbroken) rule that the things I made had to be entirely the product of my imagination. For example, a new model boat might have begun as a solid bar of balsa wood. As I cut into it and removed pieces, a form began to appear. Soon, the form would take over, and from that point onward, the knife was at the command of the model: I merely watched.

For better or worse, this stubborn independence has remained with me throughout my life. Even today, solitude, a fresh pad of inviting paper, a fine-tipped pen and feline companionship better suit my temperament than life in the madding crowd.

A novel IC product often starts with ideas of the *How About*? sort. I deliberately leave the details unstated: all options remain open. Working with the elements, I gently persuade the product into adopting a certain shape: the broad outline of its function, and essential aspects of performance. At some point, a serviceable structure appears; but I give it considerable latitude to guide me. I allow it to *breathe*; to talk to me. I listen for signs of distress welling up from deep within its physics-bound heart, and attend to them right away. We work as a team, the structure and I, in this fluid and congenial fashion, always prepared to take big chances and make major changes as unexpected ideas for elaboration and refinement come along.

As the structure reveals its own primal shape, I'll often allow this to remain its form, even if different from my original vision. Each IC of the hundreds I have designed was shaped by forces deeper and richer than a *one-dimensional list of objectives*, even though these might have been subliminal guideposts. What finally emerges, in the best cases, is a well-balanced child of many such forces: a product well-trained, disciplined in the primary tasks it has to faithfully execute during its life on a circuit board, as learned by one deeply involved with issues of *usefulness and suitability*, not by the dictates of an inflexible and heartless *Product Definition*.

RADIO AND TV EXPERIMENTS

By 9, electronics had become my daily diet. I experimented with dozens of circuits, trying out new forms, blithely unaware of all the prior work. Replicating something found in a magazine was no fun at all. A sufficient few of these *How About*? circuits actually performed a useful function! This was how I discovered regeneration in a shortwave radio. I was too young to have the knowledge or the patience to perform a pen and paper analysis *before* picking up a soldering iron. Initially, these circuits used ancient components that were screwed down on to a thick wooden board, usually with another, thinner board forming a front panel for mounting switches, pots, lights and binding-posts. These *really were* 'breadboards' (Figure 4a).

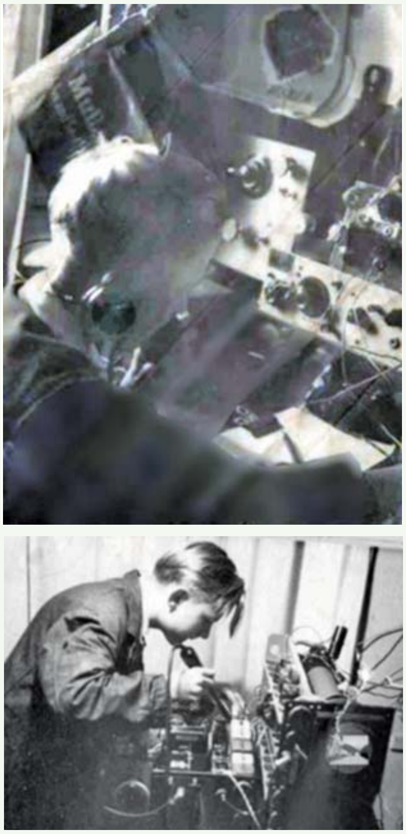

Figure 4: (a) In my natural habitat, the Happylab, about 1946; (b) Later, still there, probably at midnight, doing something gross to one of several home-brew TV receivers, 1951. My elder brother took these pix.

In an early trial, in 1946, I was experimenting with a simple amplifier. Its two stages were identical, comprising a triode with a resistive load from the anode to +120V. A capacitor from this first stage coupled the signal to the grid of the second-stage triode (Figure 5a). With my headphones connected to the second-stage anode through a DC-blocking capacitor, I noticed that touching my finger to the input resulted in a hum, emanating from the neighbors' AC supplies, mixed with the demodulation of the strongest of the AM signals. (It was more exciting to connect its input to the telephone wires on an outside wall of our house. We had no phone. The unused wires just hung alongside other lines. But *they* often *were* active, and their inductively-coupled conversations were quite clear; and often interesting!)

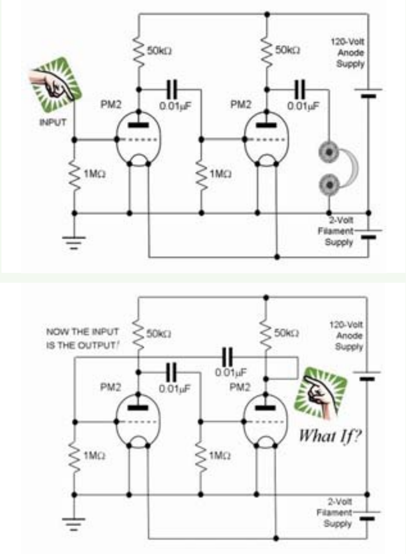

Figure 5: "Inventing" the classical multivibrator. (a) Starting with this two-stage amplifier, I asked *What If*? the output is connected back to the input. (b) Lacking a 'scope, I learned the circuit was oscillating only because of the radio interference it generated, the anode voltages being rich in harmonics.

On this occasion, with questions of the *What If*? and *How About*? sort sizzling in my head, I connected the output of this amplifier back to its input (Figure 5b). Immediately, the music on the family radio was hashed by fizzing whistles. Tuning over the frequency span of that receiver, I noticed "my" whistles came and went. More careful note-taking revealed that these squeals were spaced at regular frequencies and appeared to form low-integer ratios. I accidentally discovered two things that day: a basic type of *cross-coupled relaxation oscillator*; and its ability to generate not just *one frequency* but many, in perfect ratios!

Later checking books in the library, I found a similar circuit. In another of these books, I came across something wonderful called the *Fourier transform*, and realized that this was pretty useful, as it explained the ratios in my scribbled notes about that experiment. About two years later, I designed my own multi-band superhet receiver (Figure 6) learning entirely (although often painfully) by doing. Below decks, it was a terrible "rat's nest"; but it worked remarkably well!

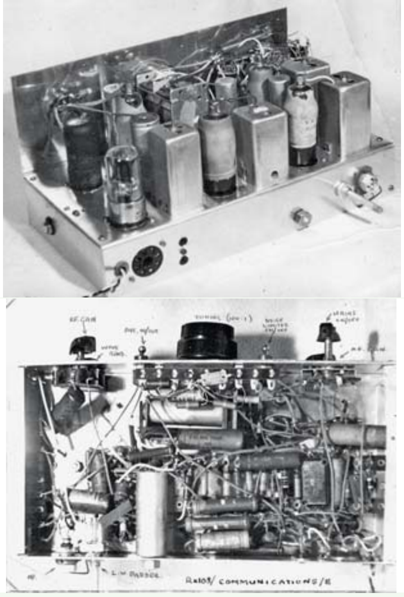

Figure 6: (a) The top-side of my first six-valve superhet and (b) the underbelly – not a pretty sight!

I enjoyed many windfalls. A lady for whom my mother housecleaned had also lost her husband in the war, and he had left a bonanza of 4- and 5-pin tubes, audio transformers, 3-inch long resistors that clipped into holders, fixed and variable capacitors, and other basic components, most still in their original cartons; and scores of spools of enameled copper wire, of assorted gauges, and green-silk-wrapped multi-strand "Litz" wire.

Another mecca was a radio repair shop, run by a certain Mr. Sparks (I assumed that was his real name). He allowed me to rummage in a back room, a storehouse of beautiful old telephones and crystal sets in walnut cases, with bright brass screw-terminals (I still have one – a *GEC Marconiphone*) and two- or three-tube "wireless sets", with fat tuning coils whose sturdy turns were held in place by heavy coatings of shellac, sporting ebony panels and overly-precise protractor dials. Inside one was an odd-looking rotating spherical coil, which I was told was a "goniometer." Of course, I bought as many of these treasures as I could afford.

Only a few years after the terrible attacks on Britain (and the equally terrifying attacks on Germany's heartland), a glut of government-surplus stuff appeared on the market. Among my many treasures from that time were 'rotary converters' (small motor/generators sets), electromechanical servo systems, IFF receivers and many strange, exotic tubes. But it was the radar displays that were my greatest inspiration. (Figure 7). One, an Indicator Unit 62A, included a 15-cm CRT and a feast of tubes; cannibalizing it and parts from a surplus UHF receiver, I built a TV receiver. Another provided the 9-cm CRT which became the heart of my first oscilloscope. I immodestly note that both of these were entirely of my own design. Building something was as much an adventure in learning as the provision of a new tool for my HappyLab.

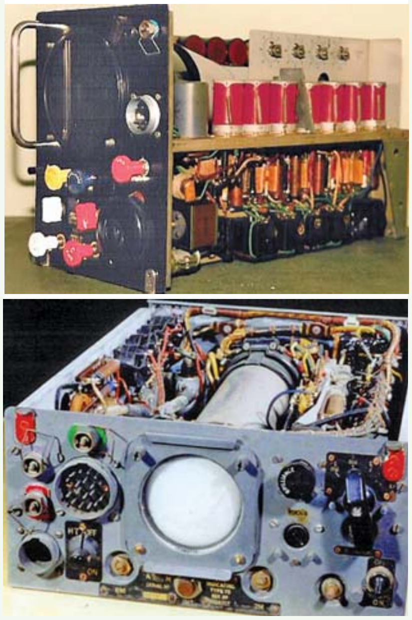

Figure 7: "Some radar 'Indicator Units purchased as WW2-surplus equipment.

Oscilloscopes were to become a special fascination for me, traceable to my exposure to these wondrous and enigmatic radar indicator units, and I designed several as a kid, experience that was to later prove invaluable in industry. However, until we got electricity in our house, I had to carry the heavy steel chassis of my first TV receiver on the saddle of my old bicycle, which I pushed to the home of a school-friend who lived about 2 km away. Their house *did* have power, and I painstakingly tested my awkward contraption on their kitchen table. The first time it was plugged in, a spot of about 2 cm in diameter appeared at roughly the centre of the screen. A propitious start, I thought; and back it went on to the bicycle. Over the course of numerous journeys, the spot became smaller and turned into a horizontal line; the line eventually turned into a raster. One day, after another long walk to Mark Dore's house, the raster finally revealed a snowy picture. It was upside down.

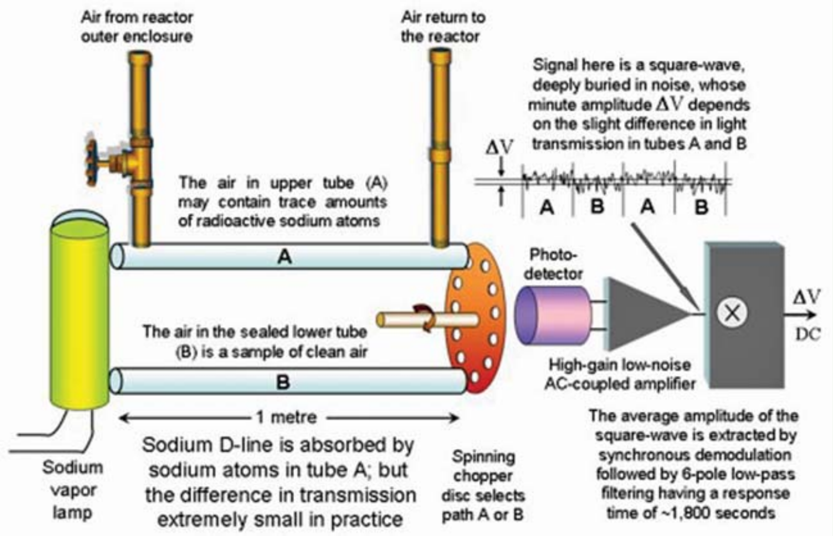

Figure 8: My leak detector monitored the status of a sodium-cooled nuclear reactor.

EARLY "WORKING" YEARS

At age 17, I started my first job, at SRDE (the Signals Research and Development Establishment, Christ church), as an "Assistant, scientific" in a group developing speech-encryption for narrow-band transmission. There I handled my first transistor, a frail point-contact type costing the Government an arm and a leg. It was one of three technologies being considered to replace the ECC81 double-triodes used in scores of shift-registers. The other two were trigger-tube or ferroresonant flip-flops. In the end, none prevailed, and the next generation of encoding systems would use miniature wire-ended vacuum tubes. This was fascinating and entertaining work. I recall building an 8-bit A/D converter using a special CRT with an encoded target.

But as a rookie in the job-market (to use today's jargon) I was naïve about the full scope of the charter at SRDE; and when, after a few months, it became clear that some very sinister military systems were also being developed there, I immediately left. Later, on trial as a pacifist, I was directed to work for two years in the local hospital, in lieu of military training. I provided general patient care in a ward for the elderly and the terminally sick. Many nights I would hold the hand of a dying patient and the next morning prepare him for the morgue. But electronics kept popping to the surface. I made a sensor that clipped on to the glass drip-window of an infusion set, and the associated circuitry, to display the drip rate on Dekatron counter tubes, and developed other sensors and displays to show vital signs. These simple aids could not be bought; medical electronics was yet to become a business; and the rotating plasma domain in the Dekatron was to become an important bridge between the magnetron and my carrier domain magnetron, described later.

At the end of the two years of mandatory service, my affection for the patients, staff and the hospital environment led me to request a transfer to their surgical operating rooms. The work was not always charming: more than once I carried a warm, freshly-amputated leg to the incinerator. But during these two further years I developed electronic devices of a less trivial kind for use in surgery. And, incredible as it must seem, I was eventually entrusted to monitor patients under anesthesia, maintaining their critical parameters and the gas-flow rates, whenever a major emergency led to a shortage of doctors; eventually even inducing anesthesia with Pentothal and Flaxedil (a powerful muscle-paralyzing agent). At other times, scrubbed-up and gowned, the surgeons allowed me to carry out minor steps in almost every kind of surgery. Today, of course, any hint of such of thing would be, appropriately, a litigious *cause célèbre*.

Dragging myself from hospital life with teary-eyed reluctance in 1958, and back in full-time work as an electron-director, I found myself at the part-time airplane company Vickers-Armstrong, I designed triply-redundant PID systems using early germanium PNP transistors, for controlling the insertion depth of the critical moderator rods in an experimental nuclear reactor at the Atomic Energy Research Establishment, located at Winfrith Heath, close to the same chalk cliffs where the magnetron had caused such excitement 18 years earlier. AERE's charter was the development of reactors for power generation, of the kind later used widely in Britain to provide electricity.

Seeing the need for a device that could detect trace amounts of leaking sodium, I proposed a detector system that chopped light between an air sample in a tube from the reactor housing and a second tube filled with outside air (Figure 8). Using synchronous demodulation and averaging over a very long interval (many minutes), I figured this scheme should be able to detect trace amounts of sodium vapor. No-one at Vickers showed any enthusiasm for the idea, so I built it. A need was recognized, and the solution provided, *before* *being requested*, which I believe to be the hallmark of the serious inventor. Whether or not this is a tenable position in these tiresome days of what is called "market-driven innovation," this has always been my personal mantra, and was to become an attitude I would encourage my team to adopt, and known as 'inciting to mutiny' at the Analog Devices NW Labs in Beaverton. Incidentally, this was the second-only remote design site of ADI, established in 1979, the first being that archetypical one in England from 1972-77 – a risky step that Ray Stata described in a 1985 article in Forbes Magazine [4].

A MAJOR EPIPHANY

After moving to Mullard, in 1959, I saw a Tektronix oscilloscope for the first time. Its ergonomics, its precision and ease of use inspired me to design an entirely new dual-channel *sampling plus real-time* oscilloscope along the same lines. I was never asked to do this, but I believed it would surely be needed soon, to provide 'millimicrosecond' measurement capabilities (the 'scopes of the day were limited to a bandwidth of about '10 Mc/s' with very poor geometry, spot size and almost no time- and voltage-calibration) while at the same time providing a useful demonstration what these things called 'transistors' could do, first, by publishing all of its circuitry in full detail in open papers, then using it to develop faster devices and circuits.

The L362 was a crude yet trail-blazing sampling 'scope, based on a design by Chaplin and Owens of the Royal Radar Establishment that had been commercialized by Mullard. One is visible on the left of Figure 9a. When it was learned that these oscilloscopes were failing by the phalanx in the field, my personal rationale to build it finally came along, and no-one was saying "No!" (nor even "Yes, *good* idea!"). The failures were due to the stresses caused by avalanche operation of its germanium alloy-junction PNP transistors. Being familiar with this mode of transistor operation, I was given the job of "finding a quick fix". Instead, I designed a radically new kind of oscilloscope, closely mimicking the appearance of the Tektronix 545 scope, as a sort of homage, but also to exploit familiarity and ease of operation (Figure 9b).

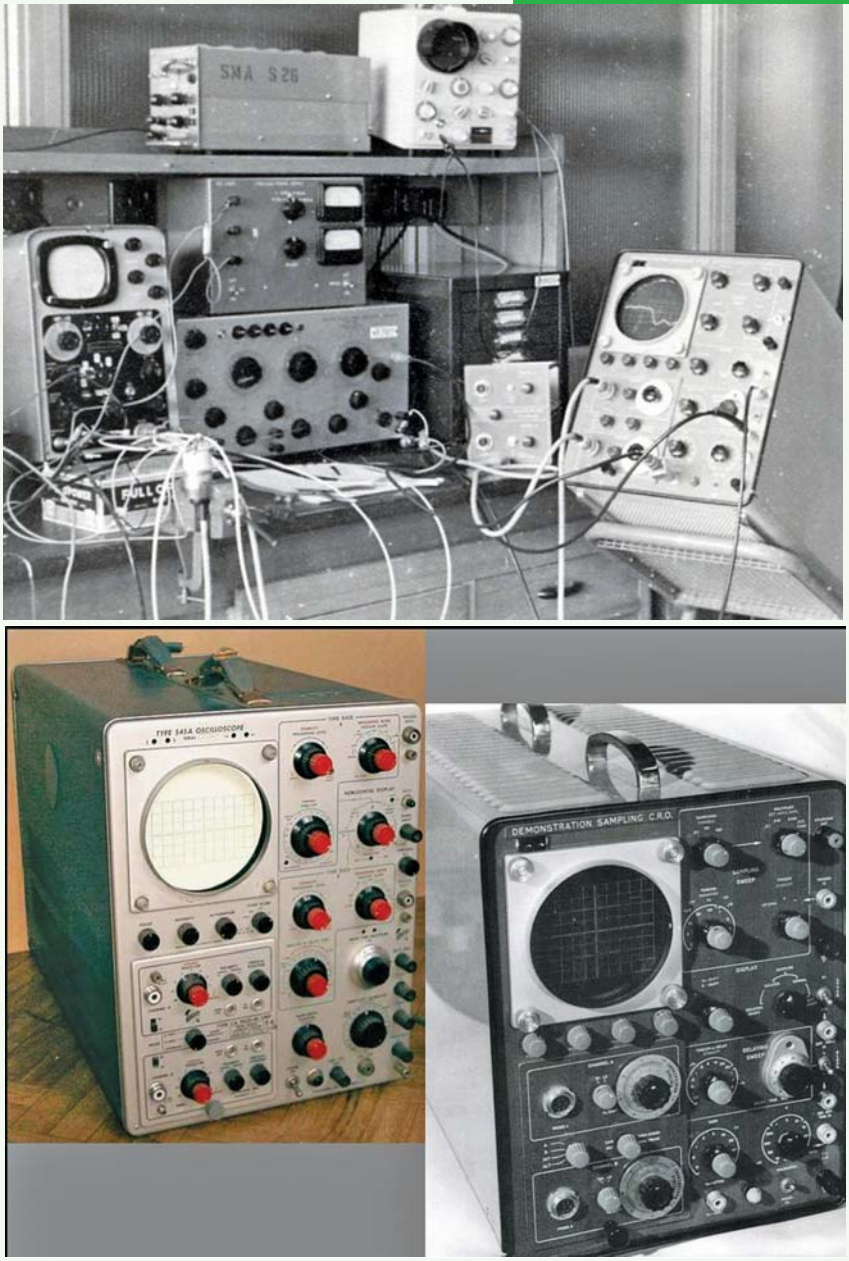

Figure 9: (a) The L362 oscilloscope (on the left) and my own sampling oscilloscope (on the right); a second plug-in can be seen. (b) Shows its similarity to the superb Tektronix 545 oscilloscope.

It was a rare occasion when I felt comfortable about emulating a masterwork. Its designers evidently had an exceptional understanding of the importance of *ergonomics* in crafting the human interface – the "front panel." The *presentation* of each of the functions (which were literally at one's fingertips, just behind each knob) were very clear; the *use of color* to identify these functions; the way in which this 'scope *faithfully and precisely* executed its promised behavior – all these were exemplary, and quite unprecedented. My interpretation of this was that the folks at Tektronix had *a deep empathy for the needs of the customer*. This was a powerful object lesson in itself, although it resonated fiercely with my own passion to put electronics at the service of people.

Whether designing systems, instruments or ICs, it is our job as creative engineers to make customers' lives a little easier, and *their* work more enjoyable. (In

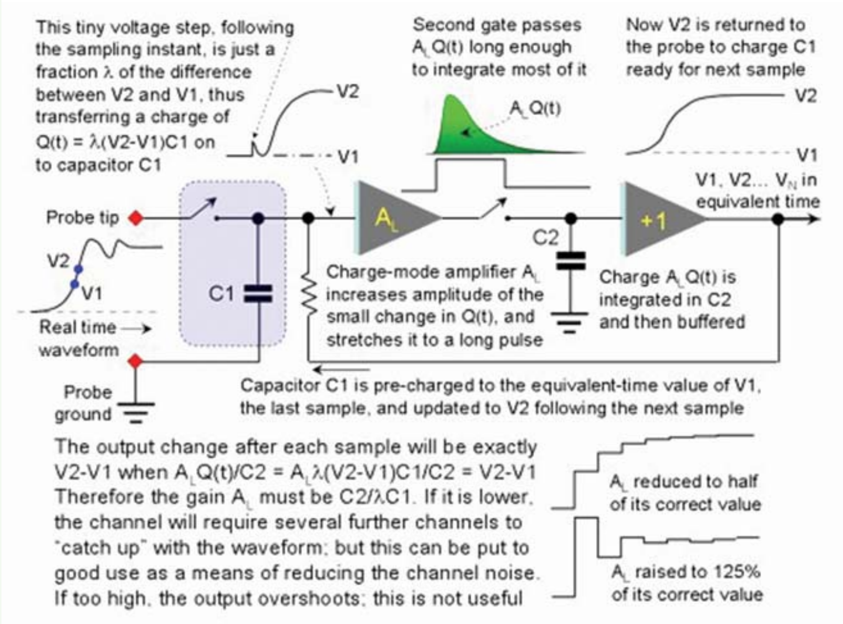

Figure 10: Sampling-scope processor using predictive feedback, novel in its day.

doing that, our lives will be enriched, too). A project must start with such questions as: *What Must Be?* (that is, what are the *external* requirements and constraints that put bounds on the project?); *What If?* I put myself into their shoes: how would I like this new product to work? *How About?* adding [some feature] to make it more useful? In this *empathic approach to design*, one constantly alternates between the customer's perspective – looking into the shop window – and one's *outward* view from the back-room workshops of novelty.

The design of this oscilloscope (and later in life, of ICs) came out of that philosophy. To begin with, I decided it should *look* like a 545 with the same familiar arrangement of controls and functions, allowing the user to immediately apply his knowledge about a similar instrument of this sort and feel comfortably expert. Thus, often the customer was, and is, myself, whether designing an instrument or a novel function IC. Later, Solartron made a hundred copies of a sampling add-on unit I designed (described in the references) to functionally and visually complement one of their low-cost 30-MHz 'scopes (top-centre, Figure 8a).

Just as fine art and great music projects a sense of effortless simplicity while concealing its complex root resources and techniques, my deceptively familiar-looking oscilloscope was a very different machine inside. It used the same Tektronix CRT and other parts, from the high-voltage-supply rectifier to their unique ceramic component mounting strips and control knobs; and it needed the help of a handful of 'valves,' for example, as high-input-Z cathode followers and CRT plate drivers. But beyond that, it was *fully transistorized*. One may wonder how I pulled this off, in 1959-61 since those early devices were pretty slow. But this is precisely the beauty of the sampling technique: in a single step, it can transform gigahertz phenomena into benign audio-bandwidth signals [5]. It is a sort of magic, a modern *léger de main*.

In the 'Delaying' mode, it operated as a conventional (real-time) scope: just as in the Tektronix 545, this slower 'B' timebase could be used to precisely delay a trigger to start the fast 'A' timebase, whose time-range was shown by a gating bright-up. When the 'Delayed' mode was selected (or using the 'A' timebase alone) this clever machine seamlessly converted to a dual-channel 700-MHz sampling oscilloscope, having the novel benefit of *high-impedance probes* (all early instruments used 50-Ω inputs). These probes included the sampling gate proper and the crucial "strobe pulse" generator, using a special transistor, the ASZ23, I had developed with the process people at Mullard, to operate reliably in the stressful, high-energy avalanche mode.

For the first time in a sampling oscilloscope, to my knowledge, a closed-loop system was used to ensure *near-perfect linearity*. In this scheme (Figure 10) the previously-acquired sampled voltage is fed right back to the load side of the sampling gate – *one step from the probe tip* – thus predicting the next output of this gate and allowing it to operate simply as an *error-detector*, affording a near-exact unity closed-loop gain. You could compare this to the operation of an op-amp connected as a unity-gain voltage-follower, though with a more complicated forward-gain path. It is also called a 'slide-back' scheme, a reference to Kirchoff's practical implementation of Hunter Christie's clever technique for measuring a voltage to state-of-the-art accuracy [6]. It allowed these probes to make multi-digit voltage measurements at the node being investigated, at any time-point on the waveform, and display these on an external DVM. Alternatively, the sampling channel could as easily be used simply as an accurate DC "preamplifier" thus avoiding the loading effects of a typical multimeter's high input capacitance. It occurred to me at the time that it would be wonderful if this digital data could be actually presented right on the CRT – an idea that later saw fulfillment at Tektronix.

Early in this development, I discovered that by lowering the gain of the loop amplifier (A_L), and exploiting the *high correlation* between adjacent samples in a periodic-stationary signal (such as a stable-frequency sine-wave or pulse-train), the noise on a displayed waveform could be greatly reduced, at the risk of some time-smearing. As has often been the case, the theory came later, and it is simple. So I exploited this, as a user-adjustable function, for each channel independently. Later called "smoothing", it became a standard feature of progressivetime samplers for averaging a wave vector. An ingenious advance, the random sampler, later invented by Frye and Zimmerman at Tektronix, no longer required the user to provide *a pre-trigger* in advance of the waveform segment of interest. This was a great step forward. However, the random locations of the sampling instants preclude the benefits of such smoothing.

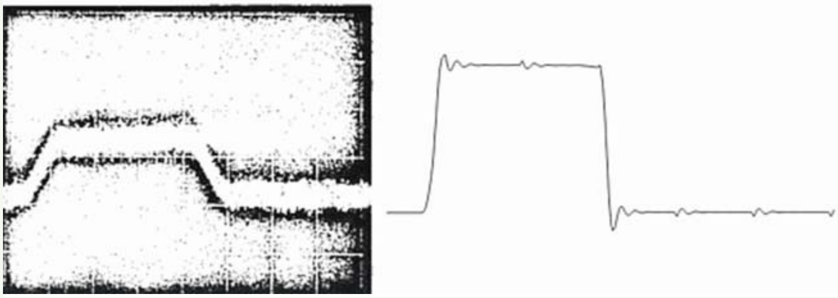
Figure 12: Pulse details buried in a noisy screen display are clearly revealed using rate-adaptive scanning.

I was understandably proud of these advances in oscilloscope design, much ahead of their time. Looking back almost 50 years, I wonder where I found the energy to do it, single-handedly, but for the invaluable help of an excellent mechanical engineer whose name I confess to have forgotten. (I recall he preferred the mature Mahler's 9th to my preference, at the time, of the spooky *nachtmusik* of the 7th.) Its two, matched, high-bandwidth channels with high-impedance probes, using the robust ASZ23 avalanche transistor, for strobe-pulse generation [7], the feedback sampling loop [8] the low-jitter timebase for real-time sweeps and precise trigger delay, and its linear nanosecond-scale timebase for equivalent-time modes [9] – all required entirely new approaches. All of its circuits were nonexistent transistor topologies in the 1960's, and they had to be implemented using the low-frequency alloy-junction transistors of the time.

The Monsterscope had other tricks up its sleeve. Simply by pressing a button, an accurate, *multi-color, plain paper* copy of the waveforms appeared effortlessly on an analog XY plotter. This was yet another novel, and obviously valuable, operational feature stemming from the time-translation process (comparable to the benefits of frequency-translation in a superhet receiver). However, it led me to stumble on an exceptionally powerful noise-reduction technique [10]. This was an unintentional benefit of the tiny analog computer (using the same old PNP transistors!) which I had initially incorporated for the following pragmatic reason. Conventionally, the *equivalent-time* sampling instant progresses at a *constant horizontal rate* across the waveform, tracked by the X-location on either the CRT or the plotting table. An abrupt change, such as the edge of a pulse, would cause the |dV/dt| of the time-transformed output to rise. But very rapid changes could not be tracked by the analog plotter's Y-axis servo, which first would be slew-rate limited and then severly overshoot, causing the plotted waveform to be seriously distorted. The problem could be averted by using an extremely slow horizontal progression; but this was an unsatisfactory way to cope with a few rare regions of rapid change.

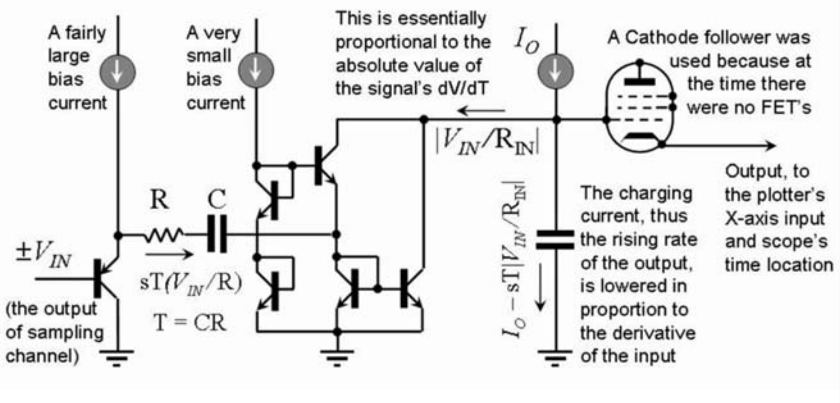

Figure 11: This simple analog computer ensures high-resolution in plotter-generated hard-copy.

The "analog computer" (Figure 11, updated here with NPN transistors) *subtracted a current proportional to |dV/dt|* from the fixed current which charged the capacitor in the plotting-specific timebase, which determined both the equivalent-time sampling instant and the plotter's X-position. At a pulse edge, the *|dV/dt|* reduced the charging current, slowing the progression of the sampling instant. Consequently, the *|dV/dt|* dropped. The *self-adjusting* dynamics of this control system resulted in the pen moving at a constant *scalar speed*, whether strolling across 'flatter' regions of the waveform or *climbing straight up near-vertical edges*. The reconstructed waveform geometry was completely free of the usual aberrations due to a plotter's mechanical inertia. Another amazing bit of *léger de main*, which could equally be applied to the CRT display.

Here's where some more magic made a welcome appearance. This speed-stabilizing process *incidentally* resulted in the transformed waveform being *trapezoidal in real time*. (Think about it). The glacial slope of this *intermediate representation* of the waveform allowed heavy averaging to be applied with no smearing of rapid pulse edges on the reconstruction; indeed, without being noticeable at all. Figure 12 – an actual CRT photo and pen-plot, extracted from [10] – illustrates the routine way in which this little analog computer exhibited mischievous disregard for the tyrannical rule of noise and averaging statistics. The nonlinear averaging of this *rate-adaptive* filter provides a far higher degree of noise reduction, over a given time interval, than is possible by linear filtering. To my knowledge, this neat technique hasn't been used since, although modern embodiments and applications would be straightforward.

For example, in a conventional spectrum analyzer, where the band of frequencies of interest is progressively scanned at a constant rate, the representation of signal power shows many sudden sharp peaks. These often limit the permissible minimum IF and video bandwidths, unless an inordinately slow scan can be tolerated. But these are benefits one may need to invoke: very low receiver bandwidths raise the resolution acuity for tiny, narrow-band signals nestling alongside much larger "interferers", as well as reducing the noise bandwidth. A technique such as just described could be very useful. Likewise, when vector data is pre-stored in RAM, the rate of withdrawal can be controlled, and DSP can perform the discrete-time differentiation of the signal.

High Jinx at Tektronix

Monsterscope had introduced several breakthrough in sampling scope design, and it became my *open sesame* to jobs in the US. In 1964, with a plane ticket to Hewlett Packard in Loveland, CO already in my hand, I switched preferences to Tektronix in Beaverton, OR (at a 10% lower salary) after an eleventh-hour phone-call from their VP Lang Hedrick. I joined a group designing sampling scopes (what else?), directed by the energetic Norm Winningstad. However, I was soon invited by Wim Velsink to join a new team to develop an exciting family of laboratory oscilloscopes, This team included a clever youngster named Les Larson, with whom I enjoyed a close collaboration.

Out of this *New Generation* project came the acclaimed 7000-series: an ambitious design, with many advances in structure, function and implementation. The first product would accept four plug-in units. Numerous new plug-ins were to be designed. Of special note were the exquisite low-noise differential amplifier with HP and LP filters designed by John Addis, the ultra-compact dual time-bases and sampling-scope plug-ins (using two of the available slots) designed from George Frye, Al Zimmerman, and Gene Cowen. It was to be permissible for any plug-in to be placed in any slot, in any combination: the 7000 had to operate as "expected". (Thus, one could swap the vertical plug-in and the time-base if one's head happened to be oriented 90° to the horizontal).

Figure 13: Howard Vollum (right) and I talk shop at Tom's Pancake House, 1968.

Furthermore, its back-plane/router (largely Les Larson's work, with some involvement on my part) needed to support very high vertical and horizontal bandwidths, since the plug-ins were expected to get faster as the years went by. The 7000-series had to last forever! Such grand objectives made even the *physical* design of the back-plane – the mechanical interfaces to the plug-ins, the choice of connector types and the fixed set of pin assignments extremely challenging – quite apart from how the signals were supposed to be routed to all the right places! And all this would, for the first time, make near-exclusive use of Tektronix ICs.

These instruments would also extend the practice – first used in the Tektronix 576 Semiconductor Curve Tracer – of showing the major operating conditions, set up by the control knobs, in the same area as the waveforms. Hiro Moriyasu wanted to use bundles of coherent fibres, illuminated in each plug-in unit by passing light through characters printed on plastic discs attached to the mechanical control shafts. As these were rotated, new characters would be projected through coherent optical connectors at the interface to the mainframe, then through more fibre bundles up to an area to the right of the CRT display. The plastic molding at the rear of these plug-ins still included the 5mm holes where Hiro's fibre bundles were expected to go; an indication of how close to production this approach had progressed).

While this scheme needed no extra "fancy electronics," in an already complex design, I felt it would be a mechanical engineer's nightmare, from the registration tolerances at the interfaces, to the snaking of dozens of fibre bundles from the dense plug-in motherboard up to the front panel alongside the CRT. It was also hopelessly inflexible, for an instrument intended to have a long production life. I frankly expressed these and other concerns to Hiro, who was, typically, quietly adamant that his was the best approach.

I already had all the key ideas for a novel, tight-knit set of ICs for a fully electronic 'knob read-out' (KRO) system, that would adventurously exploit the new possibilities opened up by custom analog integration, using Tektronix's new wafer-fab. But to prove the ideas I had to build a working demo. The crucial analog character "ROMs" (this was long before cheap IC memories) were made using paper circuits! A resistive paper known as Teledeltos (used for facsimile transmission) formed resistive boundaries onto which I placed my "emitters" – blobs of silver paint – whose physical location formed a set of eight points for each of about 40 alphanumeric characters. In the demo, these were written on the *same focal plane* as the waveforms by further time-sharing the one CRT. They displayed various operational settings, with independent control of *size, style, position and brightness*.

When I showed this to Howard Vollum, Tek's president, and one of the founders, he was visibly impressed, and very supportive.

Howard was always an ardent and enthusiastic engineer, deeply involved in the technical life of his engineers, to the point of sitting down with them sometimes over breakfast at Tom's Pancake House on Canyon Road and actually *talk-*

ing circuits! (Figure 13). What president of a large technology company now has the time to do that? (Answer: Every one of them has exactly as many hours today as did Vollum back then). Rather like the *Square and Compass* was 'the only pub in town' for the TRE folks, Tom's was just about the only restaurant in Beaverton, in the mid-1960's: close to the Tek campus, to the Satellite Motel with its garish flashing 'flying saucer' sign, and to the little airstrip where many Tekkies parked their planes. We thought nothing of flying to the coast, about 100 km west, for a change of scenery and a fully-stacked hamburger! We were all working in new and unfamiliar territories, feeling our way forward by instinct, rather than by reference to maps. But I was now in the hot seat to quickly deliver this eleventh-hour readout scheme, and at low cost. In one unusually productive year, I designed 15 ASICs for this unique synergistic system. Its most interesting aspects related to the design of the super-integrated character generators: the analog ROMs. These evolved in form, becoming more efficient in their structure over three generations of fast prototypes [11]. My decision to use *fully-analog data-coding* also raised a lot of eyebrows and was declared to be "unworkable." (However, when clothed in Teflon criticism-deflectors, it's easy to respond to naysayers with an absent-minded bemused smile). Two sets of ten-level analog-current sequences would access locations on a 10×10 matrix; about 50 corresponded to characters, the rest were special instructions, such as those related to shifting the interpretation of the data when attenuating probes were added. (I learned recently that when these inscrutable 10-level data codes had to be adapted to a new all-digital scheme for readout, they caused immeasurable grief!).

In those days, the schematics were hand-drawn on pale green engineering pads, and handed directly to the small layout team. After only a few rough sketches, they picked up their "scalpels" (Exacto knives) and began to make cuts on the thin red-plastic film bonded to a stable mylar backing. The maker's name for this material was *Rubylith*, so these masters were called "rubies". About a dozen rubies were needed to define all the photo-layers for Tek's first NPN-only process, having an f_t of 0.6 GHz. After cutting the polygons corresponding to one layer of the final IC (say, transistor emitters) the red film in all these regions had to be manually peeled off, making many clear windows; then each was hung on a large back-lit surface and photographed at ×500 reduction. It became the designer's responsibility to check the accuracy of the rubies using a multi-color ×100 set of these images, overlaid in the actual sequence of process steps.

In this tedious process, errors were easily missed. For example, the hundreds of 10-µm contact polygons for emitters, as cut regions of film, were only 5 mm square on the ×500 rubies, and often not stripped off. This oversight could easily go unnoticed in examining the 'overlays,' as a missing 1 mm opening. An easily-committed error, with disastrous consequences. But in spite of all the labor-intensive steps in going from HB pencil-lines to a complete and accurate set of rubies, then the IC masks and the waiting days in wafer-fab, first silicon invariably worked well enough to be final silicon. On a wall at Tek where Les Larson still works, he proudly displays the schematic of their first production IC, the M001. The 7000-scope took us up to about M059 (a 4-decade superintegrated counter/latch/quad-DAC of mine, for a DVM integral to the readout).

TRANSLINEAR TOMFOOLERY

In my spare time – my *best* times – at Tektronix I developed an extensive new class of current-mode circuit-cells, based on what I later named the *Translinear Principle* [13,14], and also vigorously exploited what I called *super-integration*. These included super-compact logic cells, a foretaste of I2L [15], and an intriguing class of semiconductor devices based on *current domains* – narrow, mobile regions of current injection which can be *physically positioned* on the chip either by magnetic fields or applied voltages, to realize *components* such as solid-state potentiometers and common functions such as analog multiplication [15]. Many of these inventions were announced in ISSCC papers, and to my surprise, they garnered a clutch of 'Best Paper' awards.

My first ISSCC paper [16] was one such. It described some ideas that are especially neat, and was later expanded into a pair of JSSC papers [17,18]. I am told these were the first JSCC papers to have been cited at least 100 times; and I've been asked to comment on the impact of this body of inventions. One way to assess their impact is to note that for decades thereafter scarcely an issue of the JSCC went by without at least one reference to one of these papers. Another is the fact that only today I devised yet another unique topology within this tight genre of 'stem cells'. Yet another is to note that, in my office, I have a do-it-

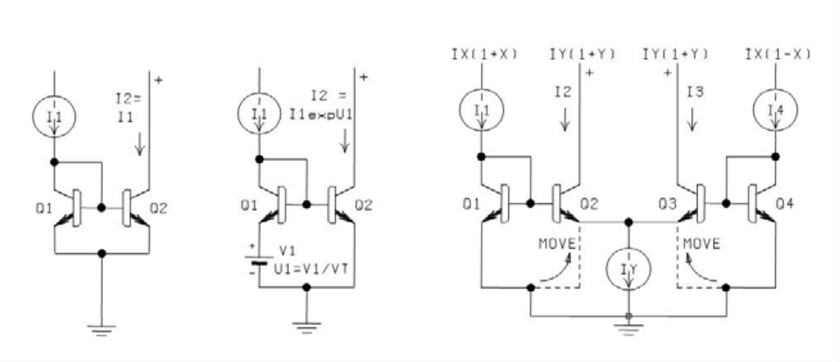

Figure 14: Transformations of the current mirror, leading to a new multiplier form.

yourself crystal-set kit, presented to me on my 60th birthday, on whose cardboard box a friend generously wrote: "*The only radio that does not contain a Gilbert Mixer!*" Let's leave it at that; the truth is always more nuanced.

Those early papers only scratched the surface. A much deeper lode was already being mined, even as I wrote them, namely, the *translinear* gold-mine, although I coined that term later, and didn't publicly advocate its use until 1975, in a brief *Electronics Letters* item. The ubiquity of these ideas quickly became evident, and led to scores of other papers, at first by myself, and later by others, including Evert Seevinck (I was his Ph.D. advisor) who added, to my initial twenty or so basic translinear topologies, some ideas about formal synthesis; and with my agreement wrote the first book on the topic [19]. Special Issues in many of the Journals, and full Conference sessions, followed.

What was the Big Deal? As much as anything else it was the arrival of '*current-mode*' as an eminently practical and advantageous signal processing paradigm, enabled by the BJT. As ideas go, it was deliciously rebellious, and potentially iconoclastic, while also of immediate value. More recently, I have tried to discourage the lax usage of the term *current mode* in papers, since in practice, good circuit design requires the use of whatever "modes" – and thus the principle state variables – as are appropriate at each stage of the processing chain [20]. However, so far, my sage advice seems to have gone unnoticed! One can still find numerous papers with titles like *A Novel Current-Mode Filter*; but no-one is staking claims to *A Novel Voltage-Mode Filter*. Yet both must equally depend on the *interchange* of voltage *and* current states.

The *current-mode paradigm* all started with the *current mirror*, a cell that had no equivalent in vacuum-tube design, mostly because tubes are "depletion-mode" devices. Since a mirror accepts a current and delivers a current, and the voltages associated with the cell are largely incidental, it was the first genuinely useful *current-mode cell*. Its "gain" is also described in current-transfer terms, and in the basic form of the mirror, this is fixed by the ratio of emitter areas, A_2/A_1 (Figure 14a). In fact, it's easy in principle to electrically alter this gain (Figure 14b); but I was curious about another possibility. *What Would Happen If?* I were to set two mirrors side-by-side (Figure 14c) then, *after severing the emitter branches* of just the *output* transistors from their roots, I enjoined them *to hold hands, one-to-one*? A marriage made in Imagination!

My matchmaking efforts fostered a radically different cell concept: a new creature. Two mirrors were transformed into a tightly-knit – indeed, indivisible and enduring – unit of four transistors. Now, the collector currents I_{C1} through I_{C4} were forced to honor and obey the (yet to be codified and ratified) Law of Translinearity: which requires that $I_{C1}.\ I_{C3} \equiv I_{C2}.\ I_{C4}$ under certain trivial and readily-met assumptions. In other words, here was a circuit form that did not process signals as *voltages mixed with currents*, but thrived entirely on a diet of *current-ratios*. Such ratiometric representations were a totally new sort of signal processing-paradigm. And *that* was the Big Appeal.

By casting the inputs I_{C1} and I_{C4} into the *complementary* form shown, using the notion of a *modulation factor X* acting on a fixed bias I_X, and supplying *a tail current* I_Y, we find that *Y*, the modulation factor in the output, is simply identical to *X* , over the full *large-signal range* $-1 \le X \le +1$. This identity doesn't depend on I_X and I_Y, nor the transistor scaling, nor the technology, nor temperature, nor (in moderation) on supply voltages. Even the BJT's finite beta does not impair this identity! Viewed as a novel linear amplifier, the gain is simply the *ratio* I_Y/I_X. No amplifier before (or since!) could claim to be linear *to the extremities* of the signal range that is, from the limit $X = -1$ *right up to* $X = +1$. Further, by varying I_Y, we had an elegant, wideband, inherently linear *two-quadrant multiplier*. The extension to four-quadrant operation was easy.

In fact, the actual trajectory of the invention was slightly different. It started with another rudimentary cell, the differential pair – the topology assumed by Q2 and Q3 in Figure 13 (c), once their emitters were joined – which forms a crude *transconductance* multiplier. But this cell is *nonlinear* with respect to what may be called its "X" input, the voltage V_{B2}-V_{B3} (the tail current I_Y being the "Y" input). I asked: *How About?* using a similar nonlinear pair to cancel the inherent tanh form of this transconductance. (I refer to this design-think as an appeal to a 'homeopathic cure' – the elimination of a cell pathology by appealing to a mathematically similar one in an inverse mode). The first account also avoids any reference to *intermediate* and merely *incidental* voltages and thus holds true to a pure current-mode theme. And it demonstrates how tiny gene-slips in the chromosomes of an analog topology can strongly impact the near-identical mutant, having critically modified its DNA (Design, Nature, Applications).

During a leave of absence from Tektronix (1970-77) to expose my young family to a taste of life in Europe, and before being 'discovered' by Ray Stata of Analog Devices in 1972, to set up the first ADI remote design center, I took a job as Group Leader at Plessey Research Labs, managing a variety of ambitious projects. One was a holographic memory: a translucent cube of about 25 mm on a side was written by several lasers; we hoped to cram a gigabyte of data into it – unthinkable at that time. To my surprise (and only because the Department Head died of a heart attack) I also briefly managed MOS memory development. As these became faster and denser, the holographic research was eventually eclipsed. Another of my project responsibilities was the development of a new high-speed optical character recognition (OCR) system. Its front-end image processing circuitry used what I called *multi-channel adaptive threshold*. (Today, these circuits would be classified as 'neural networks'). The Plessey 4200 systems that were currently in the field had 160 analog adjustments, each of which needed an expert in the field to align. I insisted that a key objective for the new system (intended for the British Post Office) was that it should have no adjustments. In the end, there was one: an iris in front of the camera lens! In reading the addresses on sometimes fuzzy or faintly-typed envelopes at very high throughputs, its recognition accuracy was the highest ever reported.

I also had ‘spare time’ to design several communications ICs at Plessey. In one, an HF modulator, the distortion generated by the DVBE nonlinearities of a BJT differential pair were sensed as they *re-appeared in a differential cascode* and applied to an auxiliary gm cell, which added correction currents in anti-phase at the final output – a technique I named *feedforward correction*. Such ‘homeopathic’ techniques, first exploited in the earlier “current-mode” cells at Tekronix, addressed both the *signal-dependent nonlinearities* and the much slower time-dependent VBE errors associated with the p*ower-induced temperature shifts* in these transistors. They provide a good example of the “*continuity of concepts*” themes that permeate one’s life.

Incidentally, Plessey were hopelessly unsupportive. They saw fit to ignore the patent disclosure I filed on those thermal correction techniques. And after having had a previously-cleared paper submission to the ISSCC accepted, they refused to pay for travel to the conference and a hotel. So I paid my own way. Apparently shamed by this, they reneged a month after I returned.

Later, back at Tektronix, I shared the thermal-correction concept and later elaborations of the cells with Pat Quinn. It became widely used to avoid the previously serious thermal distortion in vertical (Y-axis) deflection amplifiers, and known as the *CasComp*. Today’s BJTs, fabricated on silicon-on-insulator (SOI) processes, exhibit thermal resistances often higher than 10,000°C/W. Extraordinary care is needed to combat the effects of non-isothermal operation – one of the firm promises made by transistors when they first roamed the planet. Translinear cells fare especially badly: for I_C = 1mA and V_{CE} = 1V, the ΔT could be 10°C; at, say –1.8mV/°C, this translates to a whopping –18mV of ΔV_{BE}, causing a 2:1 current-ratio error in a TL loop! This concern led me to introduce thermal modeling into our simulator’s BJT equations at ADI, about 20 years back, now standard for all processes. It is sobering to watch the consequences of turning the self-heating terms back on again, after briefly being off.

I had developed an excellent rapport with ADI and a great respect Ray Stata – an “engineeer’s engineer” like Howard Vollum – while designing the first laser-trimmed IC multiplier (AD534), the first monolithic RMS-DC Converter (AD536/636), and first IC V/F Converter (AD537) [21, 22, 23]. But my life-long fascination with oscilloscopes and my regard for Howard remained strong: now my loyalties were in an awkward tension. When the family traveled back to the USA, in 1997, this angst compelled me to return to what I had come to regard as my *alma mater*, Tektronix, where I felt there was unfinished work to flush out of my system. Anyway, I could still “do ICs” there, I reasoned. (My car sports IDO ICS plates).

A LINK TO MAXWELL

A memorable assignment took me back to the lair of Philip Dee (remember him?) – the Cavendish Labs at Cambridge University, to spend time in the company of the world’s largest vacuum tube, their 2-Angstrom electron transmission microscope. This monster was nearly a metre in diameter at the viewing ports on the ground floor. From there it rose up through three floors; at the top, the cathode was supplied with _700 kV, donated by a huge transformer and rectifier inside a shielded room.

My thing was to provide the electronics to measure the cathode current. It used a V-F converter I had designed at Analog Devices (the AD537 – the first monolithic V-F, still in the catalog). One of the useful features of this empathy-borne IC was that I’d made sure it could optionally supply large currents to an LED at its square-wave output. The buzzing light then dropped down through the three floors on a thin glass fibre, to the working desks at the anode level where the scientists struggled to see Very Tiny Things through very thick windows, fiddling with “my” cathode current, I suspect, in a struggle to improve the contrast of these images.

Once, my host mischievously defeated the safety interlocks and opened the door to the EHV room while the supply was operational. I felt my hair being tugged forward by the fringing field just outside. With the power off, and the interlocks again grounding everything in sight it was safe for me to enter and work on the cathode-current monitor. But of course, to make my calibration adjustments, the microscope had to be fully operational; so I blissfully toiled in this little room at 700 kV “below sea-level”!

As an invited lecturer at Cambridge University, I was delighted to learn that the classroom in which my talks were to be presented was the very one used by James Clarke Maxwell, while teaching his new mathematical theory of electromagnetism. The musty atmosphere descended on me with the full weight of history. The students’ desks were the original ones, with initials and other cryptic symbols carved deeply into the noble dark wood, rising toward the back from the speaker’s level, and the long demonstration bench, on which Maxwell rested his palms in an earlier age. Standing there, soaking up the vibes, and dismissing my modern audience to invisibility for a moment, I felt oddly like a distant ancestor, William Gilbert (1544-1603), who wrote *De Magnete, Magneticisique Corporibus* and, bless his wooly socks, coined the word electricity. In this venerable setting, I took the opportunity to remind the audience of the work ethic of another great electronics engineer, Michael Faraday [24]:

> ***“Faraday never could work from the experiments of others,*** *however clearly described. He knew well that from every experiment there issues a kind of radiation, luminous in different degrees to different minds… And here, for the sake of younger inquirers, if not for the sake of us all, it is worth while to dwell for a moment on a power which Faraday possessed in an extraordinary degree.* ***He united vast strength with perfect flexibility.*** *His momentum was that of a river, which combines weight and directness with the ability to yield to the flexures of its bed. The intentness of his vision in any direction did not apparently diminish his power of perception in other directions; and* ***when he***

attacked a subject*, expecting results* ***he had the faculty of keeping his mind alert, so that results different from those which he expected should not escape him through preoccupation.”*** [emphases mine]

“MY MAGNETRON”

I started this piece by describing the marvelous magnetron. While at Cambridge, one of my lectures concerned a superintegrated solid-state device which I had devised and fabricated at Tektronix [25], but had not yet tested. It invoked the same intertwining of magnetism and electricity, and because of that, my blithe interlude with the ghosts of Maxwell and Gilbert was especially poignant. In 1970, during the working period back in England, samples of this *carrier-domain magnetometer* (CDM) were supplied to Prof. Greville Bloodworth (University of York) and Prof. Henry Kemhadjian (University of Southampton), and later successfully demonstrated [26]. Among several Ph.D. projects spawned by this concept, Martin Manley provided an elaborate mathematical treatment of its temperature-dependent scaling coefficients, and demonstrated a robust compensation ruse. Sadly, he was killed in a car accident far to soon thereafter.

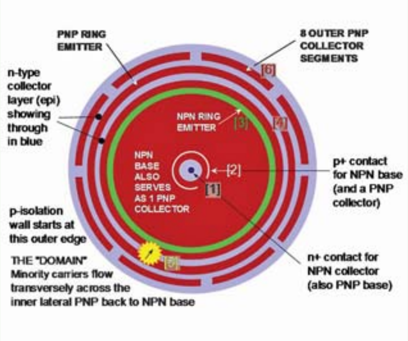

Figure 15: My “magnetron”: a super-integrated carrier-domain magnetometer.

The CDM was unique in two distinctly valuable ways: first, in its ability to convert magnetic field strength *directly to frequency*, by virtue of a *circumferentially-rotating domain*; second, in having an *integrating response*, meaning that in principle even the *weakest H-field* caused a slow, but readily measurable rotation – a very low frequency output. Figure 15 shows the principle elements of a representative device. A junction-isolated disc of n-type collector is contacted only at its center, ‘1.’ Over it, and grounded only at inner contact ‘2,’ is another disc, a p-type base; just inside its circumference is diffused an n+ ring emitter, contacted uniformly all around its perimeter, thus at an equipotential, being biased by a fixed current. Beyond the p-base edge is a coaxial ring, another p-type diffusion, ‘4,’ also contacted uniformly around its perimeter and biased by a fixed current. This ring acts as the emitter of a lateral PNP, whose local base is also the n-type collector for the NPN section, and whose (inside) collector is the edge of the p-disc ‘2,’ which simultaneously forms the base for the NPN section. Notice that the only path for the minority carriers (holes) issuing from this LPNP’s emitter is underneath the NPN disc-base, where the sub-emitter (‘pinch’) resistance is very high.

Thus, even small currents from the LPNP in the vicinity of its emission zone can raise the localized NPN V_{BE} thus *raising its emission* exclusively in that zone. Although an elemental PNPN structure exists all around the circumference, *only one* confined region of intense current injection, ‘5’, can be supported. Since the currents I_{EN} and I_{EP} are finite, the *spatial feedback* process is bounded (the PNPN loop can’t ‘latch up’); it serves only to force both n- and p- injection into a small angular range. This is the *carrier domain*: a mobile *filament of current* (roughly analogous to an ‘isolated north pole’) of a few microns in length, flowing laterally from the p-ring back to the p-base. In a perfect world, the domain would arise in a totally random location at power-up; in practice, it won’t. Either way, it is thereafter obliged to chase around the circumference under the intoxicating influence of the magnetic field perpendicular to the page, in a tantalizingly-reminiscent fashion as did in ancient times those electrons grazing the anode rim of the new-born magnetron, glowing with self-satisfaction on Dee’s bench.

Just outside the p-emitter, I placed p-type sectors forming *outer* collectors, ‘6,’ in a location analogous to the cavities of a magnetron; and while these are not microwave resonators, comparisons to the magnetron are irresistible. After all, this CDM *really* is an RF oscillator, although unlike the magnetron its frequency is proportional to the H-field strength, fulfilling its lesser destiny as an ‘H-*f* ’converter. Which is pretty neat; but beyond that, these things are inherently (and uniquely, I’m pretty sure) integrating magnetic sensors. Acting as it *should*, a domain will stroll leisurely around this circus-ring at a slow angular velocity even for minuscule fields. The direction of its stately promenade, thus the *field polarity*, can be sensed by the phasing of the current pulses generated by the outer sectors, while its *magnitude* can be ratcheted up in a counter.

Unfortunately (although predictably) my first devices suffered from a malaise I called ‘*electrostiction*’. Mask-alignment skews gave the domain the determination to wake up in its ‘home state’. This forced us to go chasing after a few mega-Teslas to overcome its stubborn will, long before MRI-grade superconducting magnets came on the scene. We finally did track down a cast-off from some early NMR work (really!), quietly rusting in a dark corner of the Southampton University campus. This sticking-point was later addressed. I asked *How About?* applying a large *alternating field* having a mean value of zero, exactly as I’d once done in my home-brewed tape-recorder to thwart magnetization hysteresis in the medium. The *net angular drift* of the domain due to a small superimposed DC field should now be measurable, using up-down counters to integrate the pulses as it rushes in a CW- then CCW-swirling tornado.

It worked! – thus making the CDM a viable *integrating magsensor* and the only such concept to have been reported. Incidentally, when the magnetic field lies *across* the device, it acts as an electronic compass (and yes, the cosine law bears on the frequency scaling in off-perpendicular cases). I also devised *linear* structures for operation in a field-nulling feedback loop to convert an H-field directly to a proportionate DC current. Although this work was gleefully presented in lectures all over the map, in memos, letters and peer-reviewed papers, none of it was ever patented, largely for lack of time on my part. (Others gladly rushed in to fill that vacuum). The original work has found its way into a 2004 textbook by G.W.A. Drummer of electronic's most noteworthy inventions [27]. And, just as the terms '*current-mode*' and '*translinear*' have been rampantly misapplied, it is regrettable that so has '*carrier-domain,*' being used in subsequent work on linear-mode (non-integrating) magnetic sensors.


Figure 16: Scots Experimenter/Tinkerer/Inventor (ETI) Baird fiddles with his CRT-based TV receiver (1927).

GLANCING BACK

It has been my good fortune to have grown up through the most prolific period of genius in electronics: to have witnessed its major inventions, not as a journalist, but as a user, being intimately involved in exploiting them in numerous applications; to have welcomed the arrival of the first, fragile point-contact transistors, not in a newspaper headline, but as an *experimenter*; to have immersed myself in silicon technologies, reaching into their rich treasure trove of possibilities, not by replicating the advances of others, but as a stubborn and fiercely independent *inventor*. Today, much of what is called electronics is block manipulation and re-use. One needs to know little about *electronic fundaments* to design many of today's IT products.

Understandably (although regrettably), few of today's students of microcircuits have a *visceral awareness* of the electronics of the past century. So here's a micro-history. Perhaps the most ingenious and seminal advance was the invention of the triode tube, by Lee De Forest in 1906. However, we cannot say that '*electronics*' arose at that time. The word was not even coined until 1927, in an obscure professional paper. In that same year, using a primitive 'cathode-ray tube', the Scottish genius John Logie Baird demonstrated the first practical TV system (Figure 16). In 1930, Sam Weber launched the influential periodical *Electronics*. Our journey on Big Maps had begun.

Baird's TV was a profoundly important milepost, by applying tubes to a far *broader scope of functions* than previously found in telegraph, telephone and radio. It, and radar, spawned clever circuits of every imaginable kind for specialized waveform- and pulse-generation: all described for my boyhood pleasure in the biblical *Waveforms* [28], just one of the cornucopia of books in MIT's Radiation Lab series, published after the war (1949). Many of these circuits sported mystical descriptors, while others were weighed down by their names, some of portmanteau proportions ("*Hey Joe! The Phantastron sure beats the Pentode-Miller-Sweep-with-Integral-Suppressor-Grid-Gating!*"). Just as any war has propelled technology, WW2 was the essential engine of advances in electron-beam optics, which would one day become the open sesame to creating the ultra-fine spot-size of the magnificent CRT found in thousands of Tektronix 545's; and one more, stealthily hiding in my monster-mutant.

From 1930 onward, technologies for vacuum-tube and electron-optics developed rapidly, to a broad peak around 1950, during which time numerous and diverse types were developed, as the scope of applications grew exponentially. This progress radically expanded peoples' faith in science and technology, and expectations of a coming dream-world, already elevated beyond reasonable hope of consummation. (Even washing machines were hyped as "Designed for the Atomic Age." Nowadays, we have "Digital-Ready" loudspeakers (?), microprocessor-controlled toothbrushes (?) and "Digital-" everything else, including digital war; while Paradise is postponed).

In that same mid-century year, the transistor – the BJT – was gearing up to change the world even more dramatically. It's known as a Bell Labs "invention", but its history is very different. First, it was an *accidental discovery* of bulk conduction, in their fruitless attempt to develop a field-effect device [29], although an upstaged Shockley must be credited with having predicted *minority-carrier transport*. Second, merchant-ship wireless-telegraphers were experimenting with HF oscillators (that is, with circuits that require *power gain*) using two, differently-biased whiskers on a chunk of galena *as early as 1915* [30]. Third, the refinement and commercialization of transistor technology – the essential know-how of semiconductor processing, the growing awareness of the yield losses due to particulate matter, the development of protective packaging techniques, and a better understanding of device behavior and the creation of models – emerged incrementally over a period of many years, and was spread over many companies and universities. No-one was the "Father of the BJT."

From 1955 onward, the use of vacuum tubes declined; twenty years later, they were practically obsolete. They now sleep in private museums, such as Prof. Tom Lee's collection of 10,000 (and mine of about 100!). But the accumulated knowledge of managing *electron beams in a vacuum* persisted. It was firmly established during the development of specialized CRTs for radar, television, oscilloscopes, medical-, analytical- and industrial-instrumentation, and countless other information displays; in the design of transmission (TEM) and scanning (SEM) electron microscopes; in complex photon detectors equipped with high-gain secondary-emission multipliers for use in such applications as neutrino detection; in *gas-filled* variants, such as the thyratron, or as gated-rectifiers using *mercury vapor,* in power control devices (roughly doing the same as a CMOS switch in a regulator, but controlling a million times the energy); and in huge triodes for generating the RF power used in industrial induction heating applications (frequently in semiconductor processing); and in other exotic ways. Tube-museum web-sites such as [31] and [32] offer an inspiring visit.

While few of the small, ordinary tubes remain in use today, specialized types continue to have great practical value, and in fact are still being developed. Viewed as *extended structures* having a plurality of *functionally distinctive sections,* each of these clever inventions is a *System in a Tube* (SiT?). From this modern perspective, they bear a certain relationship to the contemporary analog *System on a Chip* (SoC). Of special relevance in this respect was the development of the *traveling-wave tube* (TWT) and the *klystron*, both of which are RF power amplifiers. The *reflex klystron*, and the ineffective and transitional *split-anode magnetron*, which was soon trumped hands down by the powerful *cavity magnetron* – are RF power oscillators.

These tubes deserve comparison to the SoC because they co-integrate such elements, for example, as *low-loss lumped-element transmission lines* for velocity-matching (as in the TWT, and in the advanced ultra-wide-band CRTs developed at Tektronix) or the *ultra-high-Q resonators* found in magnetrons and klystrons. These modulate, manage and magnify electron flow or direction in novel ways. Formerly, in a vacuum tube, the only way to control this flow was by one or more *grids* (six in the *octode*). However, combinations of two, three or even four independent active devices were developed, some with integrated passive elements; others, such as the "Magic Eye", widely used as a tuning indicator, integrated a vacuum tube with a tiny phosphor screen. A study of Adler's 1946 inscrutably-complicated wave-weaving Phasitron tube [33], once used in FM broadcasting, should convince you of the validity of the 'SiT' notion – if it doesn't leave your head spinning.

THE GEARS OF GENIUS

These experiences form a long chain whose links remain unbroken, and which is still growing in length, sixty years after I became an avid Experimenter/Tinkerer/Inventor –an ETI – in *real* electronics: to wit, the *analog domain*, where circuit concepts and topologies are Diverse, Dimensional, Durable and downright Difficult [34]. This chain is an uninterrupted continuum of constantly-developing knowledge, orbiting a nucleus of only a handful of seminal themes. In today's immensely complex world, few can hope to excel as professionals in a broad range of disparate endeavors. Most of us have just one *bag of tricks*. We reach into it numerous times, to again extract inspiration from our expanding museum of ideas; and each time we put an idea back into our bag, it will have become a little smarter, and shine a little brighter the next time it pops out.

I have three, maybe four, seminal themes: my daisy-chains of concepts. The chain *magnetron*-to-*dekatron*-to-*carrier-domain-magnetometer* provides a great example of the *persistence-of-envisioning*. They all involve electrons – sometimes as plasmas – that are persuaded to *bunch in preferred locations* and then *rotate around a circular outer perimeter*, where they do something useful. For the first and third links in this particular chain, the persuasion comes from a magnetic field. In the second, it is discrete plasma transference, instigated by clock pulses, and in *that* regard it bears a closer resemblance to another daisy-chain – the super-integrated string counters of [14]. Indeed, it was my exposure to (and as a user of) the Dekatron counter tube as a kid that inspired the invention of this and subsequent "string" counters (which are extremely efficient in their use of chip area).

I suspect most careers are characterized by such 'continuity phenomena' as the *daisy-chain-of-concepts*, the *persistence-of-envisioning* and the *little-bag-of-tricks*. But these daisy-chains are gregarious: they intertwine. In my experience, many of the resulting cross-connections have led to branching ideas of equally satisfying quality.

As well as these, we also carry around in our head *models* – imagination-maps which give us a sense of *location*, *direction* and *intention*. The topological map of a metro such as Tokyo's will seem arcane to the casual visitor: yet a resident must understand its details, and the lines and stations for daily travel must be committed to memory. However, if we like to explore the roads less traveled, to venture forth to an invigoratingly different place, to risk, to remoteness, to travel up through Tohoku to Hokkaido, then a geographically-faithful map is indispensable.

Absorbing the *key aspects* of the metro map (many lines and stations may need to be ignored, for now) is like acquiring a firm foundation in the *fundaments* of electronics. Numerous equations, criteria, methods, models and minutiae must be assimilated, filed and sorted in one's mind. While many (say, Bessel functions) can be overlooked, for now, all the rest must be distilled down to everyday essentials. *What is the noise-spectral-density of a $50\ \Omega$ resistor at 300K? What is the value of the electron charge? Why does* V_{BE} *decline linearly over temperature? Can it really fall right down to zero, for practical conditions*? Such issues must be at one's finger-tips, as numerous individual, intellectual knowledge objects: but beyond that, they must be integrated into the instinctive, emotional fabric that *is your core being*. You won't get very far on the metro if you need to consult the map each day as you travel to work, and scrutinize every station-name beyond the window as something perplexingly new.

On the other hand, for most ETIs, a thorough grasp of the business of contemporary electronics – as a phenomenon, as an enterprise, as an industry, as a competitive forum – comes slowly, and requires us to take some long and lonely journeys on Big Maps. Like this one, articles in the SSCS Newsletter describing such journeys – situations encountered in technical, business and emotional places very far from the reader's own familiar landmarks, or the sentimental recollections of someone else's youthful adventures and irrepressible aspirations – serve to refresh us. Informed by these vicarious expeditions, the reader can return to the detailed challenges of daily work with a new perspective, a little better equipped to examine issues under a brighter light.

Younger engineers: you'll find the world is full of naysayers, who should be firmly but politely ignored. Rebut the accepted wisdom, but reserve respect for the wise. Understand the reason for my insistent repetition of the power-questions *What Must Be?, How About?, Why?* (and *Why Not?*) and rising high above them all, *WHAT IF?* These are your launchpads to novelty; they are your gilt-edged Invitation to Mutiny; they're your instruments of invention; they're the primary drive-line gears of genius.

Take big risks. It is to be hoped that all the little histories of a thousand minor past-players such as myself will add up to a powerful testament to *risk-taking*. Without going out on a limb, novelty is unlikely to emerge from one's work. Walk out onto the fragile canopy of thin limbs as often as you dare. You risk a break through, and may be in for a big fall; and what's wrong with that, I want to know. Don't *wait to be told* what to do: do it anyway. Anyway, *never* do as you are told: or rather, do it only when it seems the right and smart thing to do; then go 100% beyond what you were *asked* to do, and 200% beyond what you were *expected* to do, and 300% beyond what you *thought* you could do, rising to the pinnacle of what you *really can* do. Do it soon.

I'm starting to sound suspiciously syrupy, so here's a sobering post-script: In 1966, Sir Robert Alexander Watson-Watt, at age 64, married Dame Katherine Jane Trefusis-Forbes. Jane died five years later, leaving him hopelessly confused in a sea of jumbled memories suffering from what was likely the dreaded Alzheimer's. A few days before Christmas, 1973, unnoticed in a nursing home in Inverness, this Scot, this giant gear of genius, Sir Robert died alone. Buderi, in *The Invention that Changed the World*, called him "a scientist, a kind of philosopher, even a poet; and a bad businessman." Now *that's* an epitaph to live for.

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A Precise Four-Quadrant Multiplier with Subnanosecond Response

Barrie Gilbert, Member IEEE

Reprinted from the IEEE Journal of Solid-State Circuits, Vol. 3, No. 4 (1968), pp. 365-373.

It has been said that "Barrie Gilbert knows more about VBE than anyone else." His 1968 paper has become the fifth most frequently cited JSSC article, the first JSSC essay to be cited over 100 times, and was independently chosen by two separate ISSCC subcommittees in 2003 as among the most signficant in the 50-year history of the conference.

This popularity is easy to explain. Gilbert's brilliant insight was in recognizing that the dependability of a bipolar transistor's nonlinearity can be exploited to realize exceptionally linear systems. A current mirror, for example, may be viewed as the cascade of a logarithmic current-to-voltage converter with an exponentiating voltage-to-current converter. Despite these nonlinearities, the overall input-output behavior is linear in the current domain. The four-quadrant current-domain multiplier described in the paper shows how to extend such linearizing predistortion well beyond the case of a simple mirror. Gilbert's demonstration of the counterintuitive – that nonlinear elements may be used to create a rich variety of linear systems – has tickled, aligned and nourished neurons for forty years.

Thomas H. Lee,
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A Precise Four-Quadrant Multiplier with Subnanosecond Response

BARRIE GILBERT, MEMBER, IEEE

***Abstract*—This paper describes a technique for the design of two-signal four-quadrant multipliers, linear on both inputs and useful from dc to an upper frequency very close to the f_t of the transistors comprising the circuit. The precision of the product is shown to be limited primarily by the matching of the transistors, particularly with reference to emitter-junction areas. Expressions are derived for the nonlinearities due to various causes.**

I. Introduction

An IDEAL FOUR-quadrant multiplier would perfectly satisfy the expression

$$Z = \text{constant}, XY \qquad (1)$$

for any values of X and Y, and produce an output having the correct algebraic sign. Ideally, there would be no limitation on the rate of variation of either input.

All practical multipliers suffer from one or more of the following shortcomings.

1) A nonlinear dependence on one or both of the inputs.
2) A limited rate of response.
3) A residual response to one input when the other is zero (imperfect "null-suppression").
4) A scaling constant that varies with temperature and/or supply voltages.
5) An equivalent dc offset on one or both of the inputs;
6) A dc offset on the output.

In the field of high-accuracy medium-speed multipliers, the "quarter-square" technique has gained favor [1]. This method makes use of the relationship

$$XY = \tfrac{1}{4}[(X+Y)^2 - (X-Y)^2] \qquad (2)$$

and employs elements having bipolar square-law voltage–current characteristics, together with several operational amplifiers.

Much work has been put into harnessing the excellent exponential voltage–current characteristics of the junction diode for multiplier applications, either by using single diodes (or transistors) in conjunction with operational amplifiers [2], or, more recently, pairs of transistors connected as a differential amplifier [3]–[6]. In the majority of cases, the strong temperature dependence of the diode voltage proved a problem, and at least two commercially available multipliers are equipped with an oven to reduce this dependence.

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Another problem of the "differential-amplifier" multiplier, analyzed in [7], is the nonlinear response with respect to the base-voltage input. To achieve useful linearity, the dynamic range on this input must be restricted to a very small fraction of the full capability, leading to poor noise performance and worsened temperature dependence, including poor zero stability.

The problems associated with this type of multiplier can be largely overcome, however, by using diodes as current–voltage convertors for the base inputs, thus rendering the circuit entirely current controlled, theoretically linear, and substantially free from temperature effects. This paper is concerned mainly with the determination of the magnitude of the nonlinearities in a practical realization, and the analysis draws heavily on the groundwork laid in [7]; some mathematical expressions will be quoted directly from this paper without proof here.

II. The Basic Circuit

The basic scheme is shown in Fig. 1. It is comprised of two pairs of transistors, $Q2$-$Q3$ and $Q5$-$Q6$, having their collectors cross-connected, driven on the bases by a further pair of transistors, $Q1$-$Q4$, connected as diodes. It is the addition of this pair of diodes that linearizes the circuit. The X signal input is the pair of currents xI_B and $(1-x)I_B$. The Y signal is yI_E and $(1-y)I_E$, where x and y are dimensionless indexes in the range zero to unity.

It was previously shown [7] that the *ratio* of the emitter currents in the $Q2$-$Q3$ and $Q5$-$Q6$ pairs is the same as that in the $Q1$-$Q4$ pair and independent of the magnitudes of I_B and I_E (neglecting second order effects). We can thus write

$$
\begin{aligned}
I_{C2} &= xyI_E \\
I_{C3} &= (1-x)yI_E \\
I_{C5} &= x(1-y)I_E \\
I_{C6} &= (1-x)(1-y)I_E.
\end{aligned} \tag{3}
$$

The *differential*[1] output is

$$I_{\text{out}} = I_{C2} + I_{C6} - I_{C3} - I_{C5}. \tag{4}$$

Thus, the normalized output Z is

$$
\begin{aligned}
Z = \frac{I_{\text{out}}}{I_E} &= xy + (1-x)(1-y) \\
&\qquad - (1-x)y - (1-y)x \\
&= 1 - 2y - 2x + 4xy.
\end{aligned} \tag{5}
$$

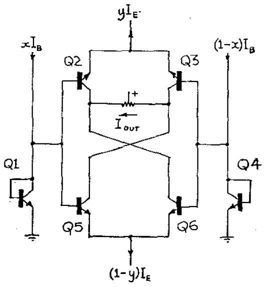


Fig. 1. The basic four-quadrant multiplier.

It is seen that the circuit is balanced when x and y are equal to 0.5. If we apply bias currents such that *bipolar* signals X and Y can be used as the inputs, and substitute

$$
\begin{aligned}
X &= 2x - 1 \\
Y &= 2y - 1
\end{aligned} \tag{6}
$$

where X and Y are in the range -1 to $+1$, the output is

$$Z = XY. \tag{7}$$

This is an exact large-signal analysis, and makes no assumptions about temperature. It did, however, assume that the transistors had 1) perfectly matched emitter diodes, 2) perfect exponential characteristics (no ohmic resistance), and 3) infinite betas.

The extent to which departures from this ideal case impair the linearity will now be analyzed.

III. Distortion Due to Area Mismatches

In [7] it was found that "offset voltage"—the voltage required to balance the emitter currents of a pair of transistors in a differential amplifier—could be expressed more conveniently as a ratio of the saturation currents (or areas) of the two emitter junctions. For the four-transistor amplifier "cell" discussed in that paper, the mismatch ratio

$$\gamma = \frac{I_{S2}I_{S4}}{I_{S1}I_{S3}} \tag{8}$$

was defined. It was then shown that for $\gamma \neq 1$ (imperfect matching), the output currents were no longer simply in the same ratio x as the input currents, but had the form

$$a = \frac{\gamma}{1 + x(\gamma - 1)} \cdot x. \tag{9}$$

This can be expressed in a form that shows the nonlinearity due to area mismatches as a separate term D_A

$$a = x + D_A = x + \frac{x(1-x)(1-\gamma)}{1 + x(\gamma - 1)}. \tag{10}$$

For $\gamma \approx 1$, this simplifies to

$$D_A \approx x(1-x)(1-\gamma). \tag{11}$$

This is a parabolic function of x having a peak value $\hat{D}_A$ of $0.25(1-\gamma)$, which leads to the useful rule of thumb

$$\hat{D}_A(\text{percent}) \approx V_0(\text{mV}) \text{ at } 300°\text{K} \tag{12}$$

---

[1] The output may also be taken as a single-sided signal from the collectors of $Q2$ and $Q6$, in which case it is $Z = \frac{1}{2}(1 + XY)$.

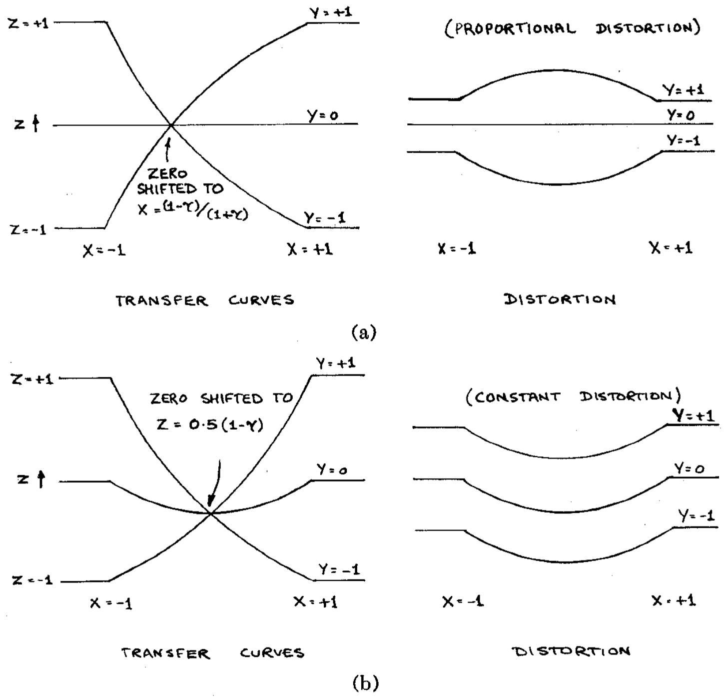


Fig. 2. Distortion introduced by area mismatches (exaggerated). (a) $\gamma_1 = \gamma_2$. (b) $\gamma_1 = 1/\gamma_2$.

where $V_0 = (kT/q) \log \gamma$, the total loop offset voltage. However, notice that $\hat{D}_A$ is not a function of temperature.

In the case of the four-quadrant multiplier, there are two such circuits working in conjunction, so we must define two area ratios

$$\gamma_1 = \frac{I_{S2} I_{S4}}{I_{S1} I_{S3}}$$

and (13)

$$\gamma_2 = \frac{I_{S5} I_{S4}}{I_{S1} I_{S6}}.$$

The total distortion (with respect to the x-input) will now be a function of y. For example if $Q1$-$Q2$-$Q3$-$Q4$ match perfectly ($\gamma_1 = 1$) but $Q1$-$Q5$-$Q6$-$Q4$ do not ($\gamma_2 \neq 1$), there will be no distortion when $y = 1$, becoming maximal when $y = 0$.

The output can be expressed as

$$Z = XY + 2yD_{A1} - 2(1-y)D_{A2} \tag{14}$$

where

$$D_{A1} \approx x(1-x)(1-\gamma_1)$$

and

$$D_{A2} \approx x(1-x)(1-\gamma_2). \tag{15}$$

It will be seen that the linearity of Z with respect to the y input is not affected by area mismatches.

For the purposes of demonstration we can consider the cases where $Q1$ and $Q4$ match perfectly, but

1) $Q2$ and $Q3$ have the same mismatch as $Q5$ and $Q6$, that is $\gamma_1 = \gamma_2$;
2) $Q2$ and $Q3$ have the opposite polarity mismatch of $Q5$ and $Q6$, but the same magnitude, that is $\gamma_1 = 1/\gamma_2$, or $\gamma_1 \approx -\gamma_2$.

In the first case,

$$Z = XY + 2x(1-x)(1-\gamma)(2y-1). \tag{16}$$

When the y input is balanced, $Y = 0$, $y = \frac{1}{2}$. Thus $Z = 0$ for all values of X. Stated differently, the null suppression with respect to the X input is unaffected by this mismatch situation.

The general form of the transfer curves and distortion products for this case is shown in Fig. 2(a), which also shows that the common point of intersection P (where $dZ/dy = 0$) is shifted to $X = (1-\gamma)/(1+\gamma)$, $Z = 0$. Notice also that the nonlinearity is always of the same sign as the output slope, and *varies in proportion* to it.

For the second case

$$Z = XY - 2x(1-x)(1-\gamma) \tag{17}$$

which corresponds to a constant parabolic distortion component *added* to the signal. In this case, when the Y input is balanced, there is a *residue* on the output of peak amplitude $0.5(1-\gamma)$. The point P is thus at $X = 0$, $Z = -0.5(1-\gamma)$, as shown in Fig. 2(b).

The general co-ordinates of P are

$$P(X, Z) = \left(\frac{1-\sqrt{\gamma_1\gamma_2}}{1+\sqrt{\gamma_1\gamma_2}}, \frac{\gamma_2-\sqrt{\gamma_1\gamma_2}}{\gamma_2+\sqrt{\gamma_1\gamma_2}}\right). \tag{18}$$

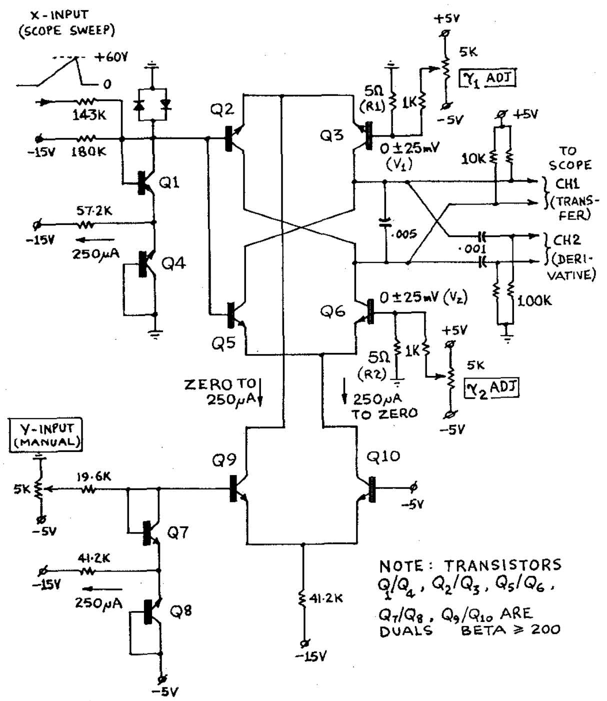


Fig. 3. Experimental circuit for investigation of nonlinear effects.

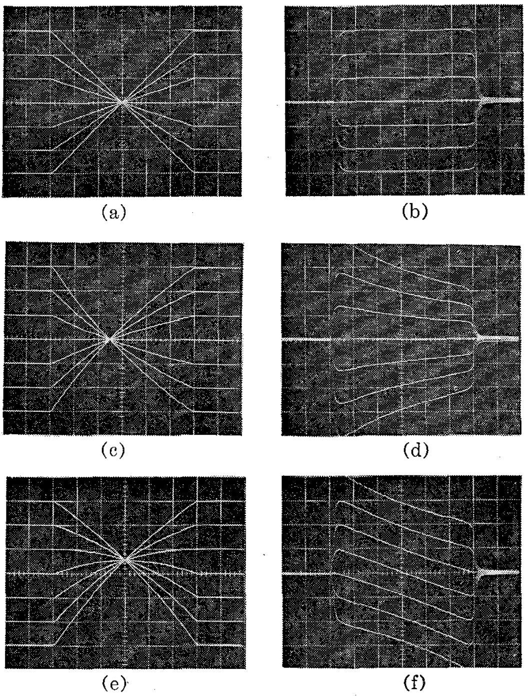


Fig. 4. Demonstration of distortion due to area mismatches. Scales are arbitrary.

Verification

To verify the above theory, and demonstrate the two cases discussed, a circuit was built as shown in Fig. 3. Use was made of the equivalence of area mismatches and offset voltage. The equivalent areas of $Q2$, $Q3$, $Q5$, and $Q6$ could be varied by the bias voltages V_1 and V_2, giving

$$\gamma_1 = e^{qV_1/kT}$$

and (19)

$$\gamma_2 = e^{qV_2/kT}.$$

The devices were operated at low powers ($I_B = I_E = 250\ \mu\text{A}$, $V_C = 2.5$ volts) so that the junction temperatures were close to 300 °K. The use of low operating currents also eliminated the distortion due to ohmic resistances, discussed later.

To demonstrate the nonlinearity more clearly, a linear ramp was used as the X input, and a simple R–C differentiator produced a waveform corresponding to the incremental slope of the transfer function. This technique provides a very convenient sensitive measurement of distortion, and became a valuable tool during the investigation of improved multiplier designs, without which it would have been necessary to resort to tedious point-by-point DVM measurements to reveal the nonlinearities.

Fig. 4(a) shows the transfer curves with V_1 and V_2 adjusted for minimum distortion, and Fig. 4(b) are the derivatives. Seven static values of Y, from -1 to $+1$, are shown. These demonstrate the excellent linearity that can be achieved with well-matched transistors. The departure from constant slope is within $+0$ -1 percent over 75 percent of the dynamic range. In terms of the nonlinearity term D_A (which is a measure of the deviation from the ideal line), this amounts to less than 0.3 percent at any point.

With $V_1 = V_2 = -10$ mV, ($\gamma_1 = \gamma_2 = 1.47$) the theoretical point of intersection is shifted to $X = -0.19$. The actual point is at -0.18, as shown in Fig. 4(c). Notice that the slope [Fig. 4(d)] falls as X varies from -1 to $+1$, starting 30-percent high and finishing 30-percent low. The deviation from the ideal line is now about 8 percent; of course, an offset voltage this large would be exceptional.

With $V_1 = +10$ mV, $V_2 = -10$ mV ($\gamma_1 = 1.47$, $\gamma_2 = 0.68$) the theoretical value of Z at $X = 0.0$ should be -0.197. This is close to the value of -0.185 measured from the waveforms of Fig. 4(e). An interesting feature of the derivatives shown in Fig. 4(f) is the one for $Y = 0$. Its linear form confirms the parabolic shape of the distortion term.

IV. Distortion Due to Ohmic Resistances

Fig. 5 shows the circuit with the addition of linear resistances in the emitters of all the transistors. These represent all the bulk resistances of the diffusions, particularly the base resistance, referred to the emitter circuit. In fact, these elements will be current dependent, due both to crowding effects and beta nonlinearities. However, if the device geometry is such that the cur-

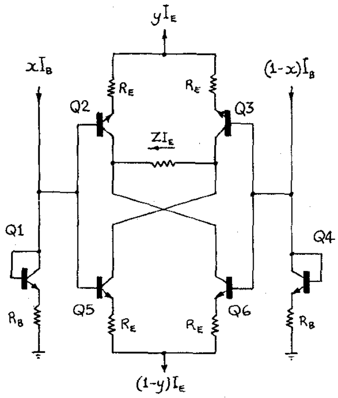


Fig. 5. Circuit having ohmic emitter resistances.

rent-density distribution is equalized in the appropriate sets of devices, the current dependence can be neglected.

Using the variables shown in Fig. 5, the loop equation for the quad $Q1$-$Q2$-$Q3$-$Q4$ under these conditions becomes

$$\frac{kT}{q}\log\left[\frac{x(1-a)}{a(1-x)}\right] = I_BR_B(1-2x) - yI_ER_E(1-2a) \qquad (20)$$

which has no explicit solution for a in terms of the other variables. However, guessing that the distortion will be small, we will make the substitutions

$$a = x + D_R \qquad (21)$$

and

$$\log(1 - D_R) \approx -D_R$$

where D_R is the fractional distortion due to resistances. Equation (20) simplifies to

$$\frac{kT}{q}\frac{D_R}{(x + D_R)(1-x)} = yI_ER_E(1 - 2x - 2D_R) - I_BR_B(1-2x). \qquad (22)$$

Solving for the distortion term, and changing input variable from x to X,

$$D_R = \frac{q}{kT}(y\phi_E - \phi_B)\,\Delta(X) \qquad (23)$$

where

$$\phi_E = I_ER_E$$

and

$$\phi_B = I_BR_B, \qquad (24)$$

these representing the extra voltages in the emitter and base circuits due to resistances, and

$$\Delta(X) = \tfrac{1}{4}X(X^2 - 1) \qquad (25)$$

which describes the form of the distortion, and has peak values of ±0.096 at $X = \pm 0.577$, and zeros at X ±1 and 0.

Equation (23) makes the reasonable assumption that ϕ_E and ϕ_B are small compared to kT/q. For example, assume $R_E = 1$ ohm and $I_E = 2.5$ mA, giving $\phi_E = 2.5$ mV, about 10 percent of kT/q at 300°K.

Using the above approximate analysis, we can state a rule of thumb for the peak magnitude of D_R, for the quad $Q1$-$Q2$-$Q3$-$Q4$:

$$\hat{D}_{R1} \approx \pm 0.37(y\phi_E - \phi_B) \qquad (26)$$

for ϕ_E, ϕ_B in millivolts, at 300°K, and $\hat{D}_{R1}$ in percent. Similarly, for the $Q1$-$Q5$-$Q6$-$Q4$ circuit, we have

$$\hat{D}_{R2} \approx \pm 0.37\,\{(1-y)\,\phi_E - \phi_B\}. \qquad (27)$$

The *net* nonlinearity will come from both circuits, and vary with the y input. The outputs of each quad (and hence the distortion terms) are also weighted by y and connected out of phase. Thus

$$\begin{aligned}\hat{D}_R &= \hat{D}_{R2} - \hat{D}_{R1}\\ &= \pm 0.37[\{y\phi_E - \phi_B\}y - \{(1-y)\phi_E - \phi_B\}(1-y)]\\ &= \pm 0.37(\phi_E - \phi_B)Y \quad \text{(percent)}, \qquad (28)\end{aligned}$$

with the substitution of $Y = 2y-1$. The nonlinearities introduced by *balanced* emitter resistances can be summarized as follows.

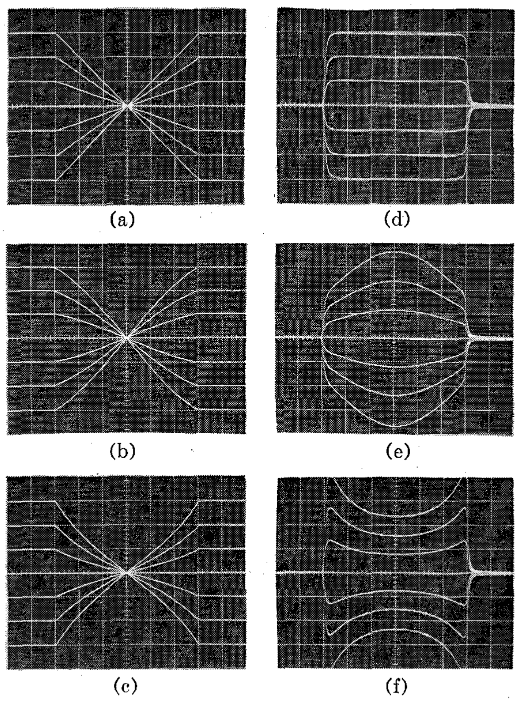
1) The distortion with respect to the X input has a symmetrical form and is a fixed percentage of the output Z.
2) There is no distortion with respect to the Y input.
3) The common point of intersection of the transfer curves is always at $X = Y = Z = 0$.
4) No distortion arises when $\phi_E = \phi_B$.

Thus, quite large ohmic resistances can be tolerated (that is, it is possible to use devices with high base resistance and/or low beta), provided that the base and emitter voltage terms are balanced. By scaling the device geometrics in the ratio I_E/I_B, the closeness with which $\phi_E = \phi_B$ is then a matter of device matching.

In practice the resistors labeled R_B in Fig. 5 will not be equal. It can be shown that under these conditions there will be a residue in the multiplier output for $Y = 0$, having the S-shaped form described by (25), and having a peak amplitude (at 300°K) of

$$\hat{D}_R \approx \pm 0.05\, I_E(R_{E2} + R_{E3} - R_{E5} - R_{E6}) \qquad (29)$$

where $\hat{D}_R$ is in percent, I_E in milliamperes, R_E in ohms. Notice that this residue term is independent of ϕ_B, a fact that has been experimentally confirmed. It will be apparent that linear emitter resistances reduce the output swing capability because in the limit (when the diode voltages are small compared to the "ohmic" voltages) the circuit becomes completely cancelling for all values of X or Y. Also, the case where these resistances are unbalanced will give rise to an equivalent offset on one or both of the inputs.

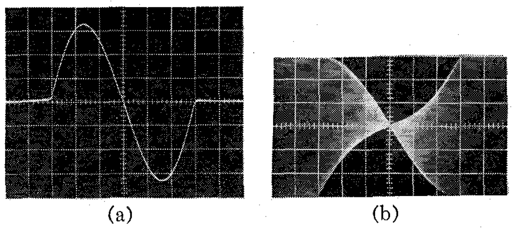


(a) (d)

(b) (e)

(c) (f)

Fig. 6. Demonstration of distortion due to ohmic resistances.



(a) (b)

Fig. 7. Characteristic distortion due to mismatched resistances. (a) Vertical scale expanded to 0.33 percent/div. (b) 3.3 percent/div.

Verification

Using the test circuit of Fig. 3, to which emitter resistors were added, these nonlinearities were demonstrated. In Fig. 6(a), all resistors were 50 ohms and $I_B = I_E = 250$ μA; thus $\phi_E = \phi_B = 12.5$ mV. The derivative waveform, shown in Fig. 6(b), shows little degradation of linearity over the full dynamic range.

By omitting the resistors in the $Q2$-$Q3$ and $Q5$-$Q6$ emitters, a net error of $\phi_B = 12.5$ mV remains. Equation (28) predicts a nonlinear term of ±4.5 percent at $Y = \pm 1$. The measured value is ±3.3 percent. (Due to the approximations, (28) will err on the high side when ϕ_B or ϕ_E become comparable with kT/q). See Figs. 6(c) and (d). By omitting the resistors in the $Q1$-$Q4$ emitters, the distortion is of the opposite polarity, as Figs. 6(e) and (f) demonstrate.

The most typical distortion is due to the case where the ohmic voltages do not match, due probably to mismatches in r_b and beta. This can be demonstrated, too, by inserting the 50-ohm resistors in just the $Q2$-$Q3$ pair, when (29) predicts a peak distortion of ±1.25 percent of full scale with the Y input balanced. The measured nonlinearity is shown in Fig. 7(a), in which the display was expanded vertically 50 times and the distortion has peak values of ±1.1 percent. Fig. 7(b) gives the appearance of the distortion when the Y input was modulated to a depth of about 20 percent.

V. DISTORTION DUE TO BETA

The final imperfection to consider is that of finite beta. Three cases can be considered:

1) the transistors have identical, constant beta;
2) the transistors have differing, but still constant, beta;
3) the transistors have identical, current-dependent beta.

The first case was dealt with in [7] where it was shown that the only error is that the output current is reduced by the factor alpha (for I_E less than βI_B). In the version of the circuit driven by a single-sided input current (as, for example, the test configuration shown in Fig. 3), a small offset term also arises, and the dc output for $Y = 0$ is approximately

$$Z(X, 0) = (1 - \bar{\alpha}) \frac{I_E}{I_B} \qquad (30)$$

where $\bar{\alpha}$ is the large-signal common-base current gain.

The second and third cases have not been completely analyzed, and it is doubtful whether explicit expressions involving all the betas and their nonlinearities would be of any value. Clearly, there is now the possibility for distortion terms to arise. However, the variations in beta from device to device, and over a small current range, are usually sufficiently small that no serious distortion should arise using typical transistors with betas in the neighborhood of 100.

VI. THERMAL DISTORTION

The topic of thermal distortion in this category of circuits was dealt with in [7], where it was shown that theoretically no distortion arises due to the differential heating of devices if the power dissipation in the inner and outer pair are equal. This can usually be arranged, and, if necessary, the circuit can operate with I_E less than I_B.

In practice, using monolithic circuits the thermal distortion in response to a step input is very much less than 1 percent of the output amplitude, and persists for no more than a few microseconds.

VII. TRANSIENT RESPONSE

Because of the very small voltage swings at the inputs, and the cross connection of the transistors, the aberrations due to capacitances are very small, especially when properly balanced inputs are used. The main speed limitation is the f_t of the transistors.

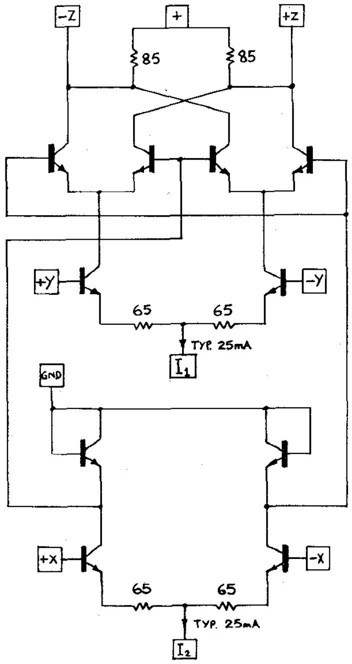


Fig. 8. Circuit used to examine high-frequency behavior.

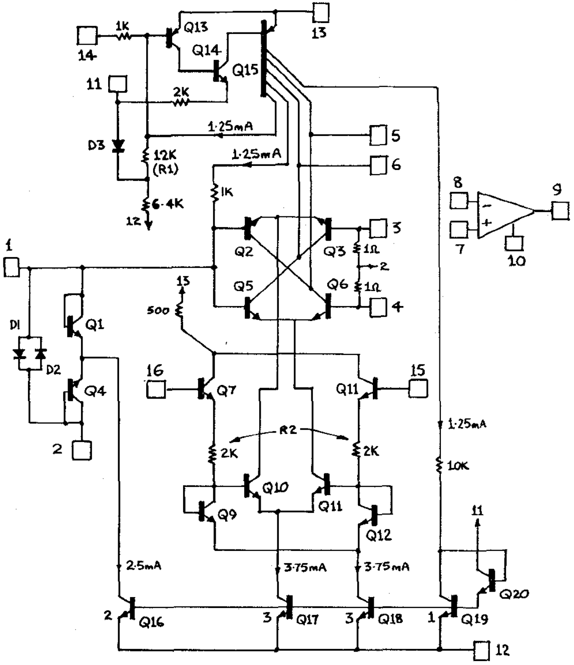
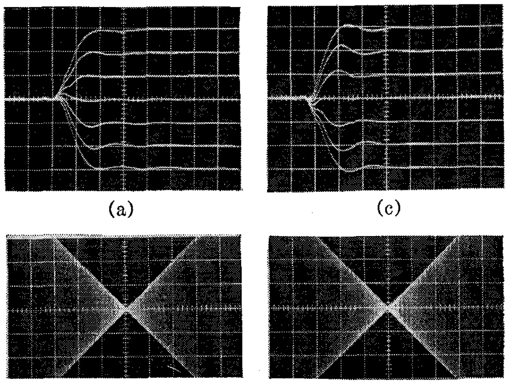


Fig. 10. Complete monolithic multiplier.


(a) (c)

(b) (d)

Fig. 9. Performance of integrated version of Figs. 8. (a) and (b). Transient response on X and Y inputs, respectively, at 1 ns/div. using dc control on other input. (c) and (d) 200-MHz carrier on X and Y inputs, respectively, staircase voltage on other input. Peak swing is 90 percent of full scale in all cases.

At $Y = \pm 1$, one of the transistor pairs $Q2$-$Q3$ or $Q5$-$Q6$ is producing all the output. The 3-dB bandwidth is, thus, about $f_t I_E / I_B$. At $Y = 0$, each pair receives $I_E/2$, and the bandwidth is doubled. We would, therefore, expect a risetime variation in response to a step on the X input of about two to one between these extremes. The step response to the Y input should be fairly independent of the X amplitude.

Measurements on an early integrated multiplier were made to examine the high-frequency behavior. The circuit, shown in Fig. 8, uses an "inverted" pair of input diodes [7], which are conveniently driven from pairs of emitter-degenerated stages for the X and Y inputs. Transient response for each input is shown in Fig. 9(a) and (b). Figs. 9(c) and (d) show the CW response for a 200-MHz input, with the other input driven by the staircase output of the sampling time base in the oscilloscope used to examine the responses. The null suppression was better than 20 dB at 500 MHz.

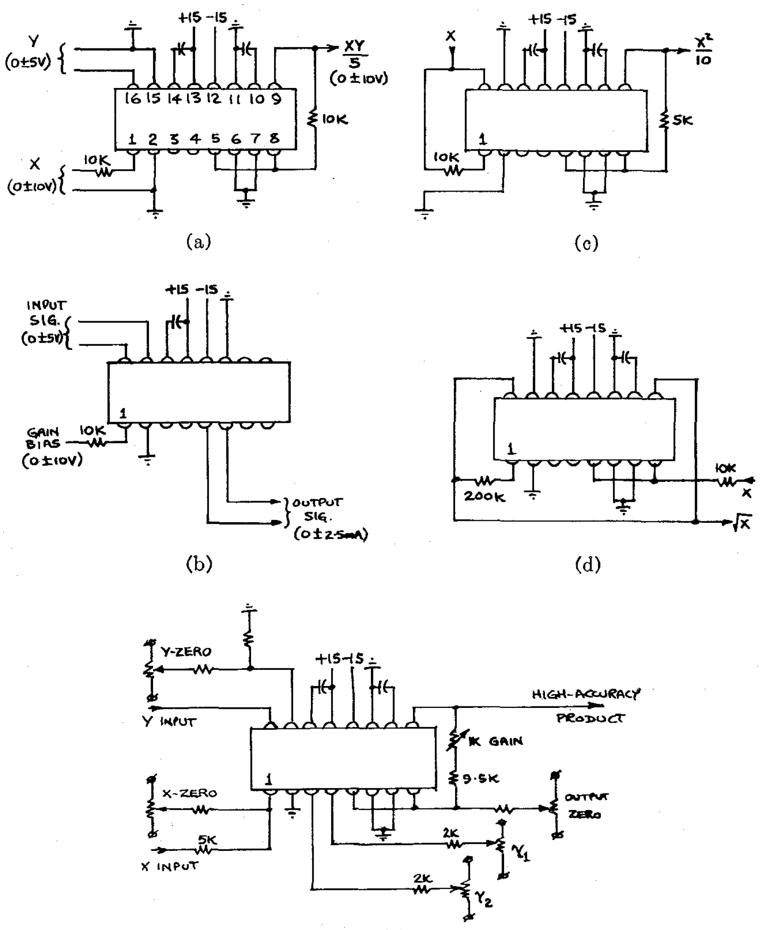
VIII. A. COMPLETE MONOLITHIC MULTIPLIER

Fig. 10 is the circuit of a complete multiplier suitable for integration. It is designed so as to be usable with a minimum of additional components to achieve medium-accuracy operation, or with extra components to perform at a higher accuracy. Wide-band operation (dc to >100 MHz) is available, or more versatility can be obtained by using the built-in operational amplifier to give division, squaring and square-rooting modes. These variations are possible by pin changes only. The X input is a single-sided current I_x into a summing point at ground potential, in the range 0 ±1 mA. The y input is a differential voltage V_Y into a high impedance (approx. 400 kΩ) in the range 0 ±5 volts. It can be shown that the output from pin 6 is

$$I_Z = \frac{I_x V_y}{5} \qquad (31)$$

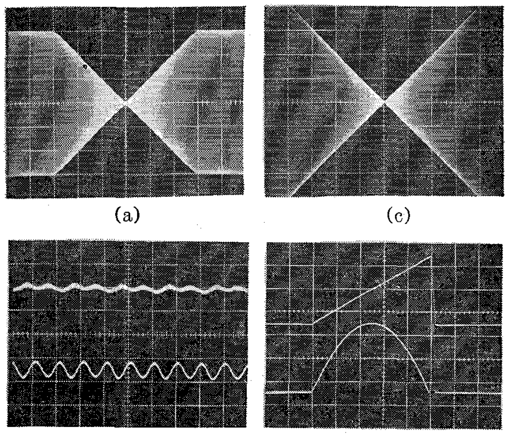
the scale factor being determined by the +15-volt supply and the ratio of R_1 to R_2. The diode D_3 ensures temperature stable scaling, and also makes the scaling factor proportional to the positive supply over a limited range.

Input and output current balance, and the rest of the circuit currents, are determined by the five-collector



(a) (c) (b) (d) (e)

Fig. 11. Circuit of Fig. 9 connected as (a) medium-accuracy multiplier, (b) wide-band gain and polarity control, (c) squarer, (d) square-rooter, and (e) fully corrected multiplier.



(a) (c) (b) (d)

Fig. 12. Typical performance. (a) As balanced modulator, carrier frequency 5 MHz, peak output swing is 90 percent of full scale. (b) Output expanded ten times in vertical and horizontal axes—vertical now 1.67 percent of full scale/div. (c) Null suppression for full-scale 5-MHz carrier on X (upper trace) and Y (lower trace), expanded to 0.1 percent/div. (d) Offset ramp applied to both inputs produces the parabolic output, 1 μs/div.

lateral *p-n-p*, $Q15$. The matching of the currents to the five collectors (base diffusions) is vital to balanced operation. Measurements indicate that matching errors considerably less than ±2 percent can be achieved. Notice that one of the collectors is connected in an operational configuration, through $Q13$ and $Q14$. This loop has to be stabilized by an external capacitor connected between pins 13 and 14. The second collector supplies a nominal 1.25 mA to balance the X input; collectors 3 and 4 supply the output balance currents; collector 5 sets up the current tails for the multiplier via $Q16$ through $Q20$.

Pins 3 and 4 give access to the bases of $Q3$ and $Q6$, allowing linearity-connection voltages to be applied. For perfect connection, these voltages should be proportional to absolute temperature. The aluminum 1-ohm resistors come close to this ideal, having a temperature coefficient of 0.38 percent per °K, slightly greater than the coefficient of kT/q at 300°K.

The operational amplifier increases the versatility of the device by permitting several modes to be implemented. Pin 7 is normally grounded, and the inverted output from the multiplier, pin 5, is connected to pin 8; pin 6 is also grounded. Hence, the multiplier block $Q2$, $Q3$, $Q5$, $Q6$ works with a collector-base voltage of 0 ±100 mV (the base voltage swing). The overload diodes, $D1$ and $D2$, must, therefore, be Schottky-barrier diodes having negligible conduction for most of the working voltage range at the X-input summing point, but being able to conduct heavily before the collector diodes of $Q2$ and $Q5$ under overload conditions. These may now be fabricated along with the standard silicon circuitry.

Fig. 11(a) through (e) illustrate the versatility of the circuit. The waveforms in Fig. 12 show linearity and null suppression at 5 MHz, and the output in the squaring configuration.

IX. SUMMARY

A technique has been described that overcomes the inherent temperature dependence and nonlinearity of a transistor four-quadrant multiplier, and the feasibility of producing a complete monolithic multiplier with a worst-case linearity error of the order of 1 percent on either input has been demonstrated. Better linearity is possible by adjustment of transistor offset voltages. Bandwidths of over 500 MHz have been measured.

ACKNOWLEDGMENT

Thanks are due to the Integrated Circuits Group at Tektronix for the fabrication of many experimental circuits, and to G. Wilson and E. Traa [8] for helpful discussions.

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Tales of the Continuum: A Subsampled History of Analog Circuits

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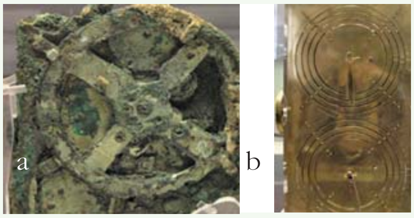
Prologue

Contending with the Aegean's capricious weather has been a fact of life for Greek mariners throughout recorded history. And so it was just another unremarkable October squall that delayed Dimitrios Kondos and his crew from returning home in the fall of 1900. With not much else to do while waiting for the weather to clear, the ship's team of sponge divers went to work where nature had boxed them in, off the coast of Antikythera (an isle not far from Crete). While diving about 60 meters below the surface, Elias Stadiatos was stunned by the surreal sight of life-size (and lifelike) statues seeming to reach for him through centuries of silt. His excited, near-incoherent ramblings about "a heap of dead, naked women" worried his crewmates that he'd suffered a serious problem with his air supply [1].

Another, more violent, Aegean storm had claimed a cargo vessel there two millennia earlier. Excavations yielded a bounty of treasure from the wreckage of what likely had been a ship bound for Rome. Aside from the spectacular bronze and marble statuary that had startled Stadiatos were piles of coins (whose features helped date the wreck to between 85 and 60 B.C.E.), jewelry, and the usual assortment of utensils, amphorae and other everyday objects. Almost overlooked among the debris was what appeared to be a wheel embedded in some rock. When researchers got around to examining the artifact more closely, they found that the "rock" contained parts of a remarkably sophisticated device, now called the Antikythera mechanism. Thanks to modern imaging technology, archeologists have been able to read about 95% of the text inscribed on the components. Better yet, this same technology has enabled a reconstruction of most of the device. This work has shown the mechanism to be an orrery – a machine for illustrating the motions of the planets. So advanced is the craftsmanship that it predates by fourteen centuries any machinery of comparable complexity and precision.



a) Main fragment of Antikythera mechanism; b) A modern reconstruction. (Wikipedia, "Antikythera mechanism," retrieved 18 Sept. 2007.)

The Antikythera mechanism is in fact an analog computer, where *analog* is used in the original sense of the term. The universality of physical laws often allows a problem in one domain to be reformulated as an analogous problem in another domain, where solutions might be found more readily. This universality underpins the operation of the Antikythera computer, whose hand-cranked array of some three dozen gears models celestial mechanics with physical mechanics. Aside from being conveniently smaller than a solar system, an orrery can also run its simulation forward or backward in time, allowing the prediction of important celestial events, as well as enabling a study of the past. Although we don't know whether the Antikythera mechanism was actually used for such astronomical purposes or was simply an expensive toy for a wealthy Roman patron, its mere existence is evidence of an ancient and conscious appreciation of the analog idea.

Because physical variables are continuous quantities, the use of analog computers to model real-world phenomena led to *analog* gradually acquiring its modern association with continuity in time or amplitude. As digital computation displaced analog computation, the earlier meaning of the word faded somewhat into obscurity, and now serves mainly as the answer to a trivia question.

Introduction

Computation is one of the traditions that gave rise to modern analog electronics. Others include communication and instrumentation, and this list is by no means exhaustive. The vastness of these topics individually, to say nothing of them collectively, makes a comprehensive examination impossible. We offer this article instead in the spirit that a sub-Nyquist sampling is better than none, and present an admittedly incomplete, biased selection of some analog circuits that may fairly be deemed "classic" by virtue of their historical priority or influence on later developments. We apologize in advance for the inevitably gross errors of omission. We can aspire here only to avoid serious errors of commission.

Analog Electronics in Computation and Control

After a long gestation, the idea of analog computation re-emerged in earnest in the late 19th and early 20th centuries. An important and oft-cited example is Kelvin's *harmonic synthesizer* of 1878 [2]. The synthesizer, designed by William Thomson before becoming Lord Kelvin, was a special-purpose mechanical device (in this case, for predicting tide heights), just as was the Antikythera mechanism. Several decades later Vannevar Bush and Harold L. Hazen of MIT elaborated on many of Kelvin's ideas to develop the Differential Analyzer in the early 1930s [3]. The Analyzer was the first general-purpose analog computer, and in its first incarnation was capable of solving sixth-order differential equations.

Even though the mechanical Differential Analyzer could solve complex problems considerably faster than humans, the second World War brought an urgent need for still faster computation. Appreciating that electronic means would be far more agile than the Analyzer's sluggish mechanicals, David Parkinson and Clarence Lovell of Bell Laboratories proposed in 1940 what would eventually become the M-9 Electrical Gun Director [4][5]. The M-9 development team included future EE "household names" Hendrik Bode, Claude Shannon and Richard Blackman. Operating in real time on aircraft tracking data supplied by an SCR-584 radar unit, the M-9 analog computer not only predicted trajectories, it also controlled the aiming and firing of artillery to maximize the probability of a hit. When used in conjunction with proximity-fuze equipped ordnance, these technologies reduced by over an order of magnitude the amount of ammunition required. The astonishing speed with which the art matured on several fronts simultaneously is evident from the fact that just four of 104 V-1 flying bombs launched toward London in late August of 1944 made it to their target [6]. Only two months earlier, before this equipment and trained crews could be deployed, over 80% of the fast, low-flying bombs had managed to slip through British air defenses to devastating effect.

At the heart of the gun director's computers were vacuum-tube feedback amplifiers configured to perform mathematical functions such as integration, inversion and summation. A classic paper by Ragazzini, Randall and Russell (submitted in April of 1946) describes the details of how this magic works, and in the process introduces a now-familiar term [7]:

> *As an amplifier so connected can perform the mathematical operations of arithmetic and calculus on the voltages applied to its input, it is hereafter termed an "operational amplifier.*

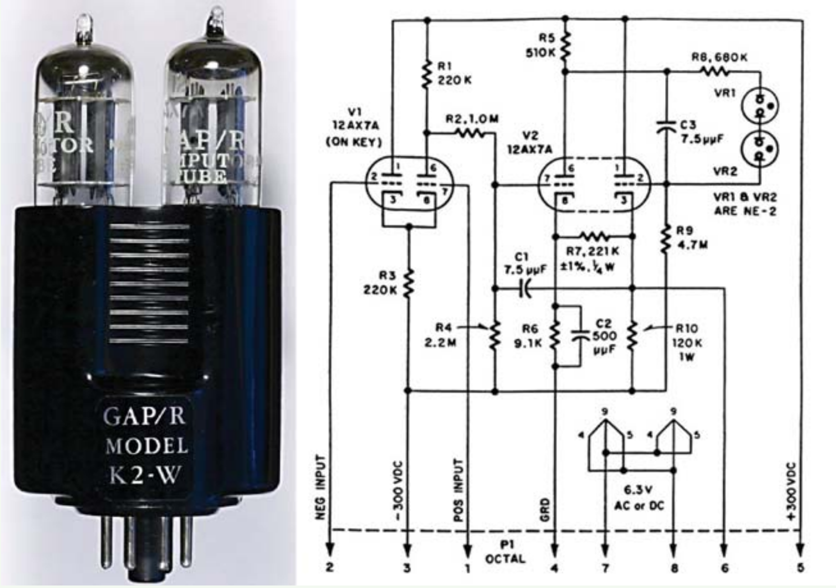


Figure 1: K2-W operational amplifier: a) Photo (courtesy of Joe Sousa, http://www.philbrickarchive.org/); b) Schematic (from a K2-W datasheet; courtesy of Bob Pease, National Semiconductor)

The paper also perfunctorily acknowledges L. Julie and G. A. Philbrick without detailing the nature of their contributions. Under subcontract to Philbrick (who in turn had a contract to develop an analog computer for bombing simulators), Loebe Julie had greatly simplified and otherwise improved the prototype op-amps used early in the war, and evidently passed this knowledge on to Ragazzini's co-authors [8]. In 1952 George A. Philbrick Researches went on to introduce the first commercial op-amp, the K2-W (see Figure 1), whose influence on subsequent op-amp development is incalculable.

This DC-coupled amplifier operates off of +/-300V power supplies, and manages +/-50V swings into 50kΩ loads. Possessing a unity-gain frequency of 300kHz, a minimum DC gain of 10,000 (and typically about twice that), and a list price of $22, the K2-W was an instant classic.

The K2-W's minimalist design reflects one of the lessons learned during the M-9's development: Keep the dynamics simple to facilitate stability. With just two stages of amplification, the K2-W satisfies that dictum. To make up for the associated tradeoff in DC gain, the K2-W employs positive feedback around the second gain stage (through R7), boosting the gain by approximately a factor of five. The use of positive feedback here may surprise the many engineers who acquire the belief somewhere in their EE education that positive feedback is only good for making oscillators or latches and is otherwise to be avoided. The successful use of positive feedback by the K2-W powerfully refutes that unfortunately widespread misapprehension. Indeed, as we'll discuss later, not only did positive feedback precede the use of negative feedback in electronics, it in fact enabled the age of electronics to begin in earnest.

The K2-W also exploits the Miller effect to assure simple dynamics. The second stage's high voltage gain assures that the effective capacitance seen by the first stage is many times the value of C1 (imagine trying to lift an object when the other end is pulled by an opposing force; the apparent increase in weight is the essence of the Miller effect). Although this Miller multiplication of capacitance certainly reduces bandwidth, it also assures near-single pole behavior over a broad frequency range. This latter attribute is valuable for a general-purpose building block, as it allows engineers to use the amplifier in a variety of feedback configurations without having to worry too much about instability. Miller compensation remains a standard way of producing single pole dynamics.

Level-shifting in modern IC designs is facilitated by the availability of complementary devices (one device shifts upward in voltage, its complement shifts voltages downward). Because vacuum tubes are of one polarity only, the K2-W uses an alternative method: Two neon bulbs act as downward level shifters (effectively a battery in series with the signal) in going from the output of the second gain stage to the input of the cathode-follower buffer stage. Each neon bulb drops perhaps about 55V, for a total level shift of approximately 110V, centering the output voltage range about zero, as desired.

The influence of the K2-W is evident in both discrete and IC op-amp designs through the ages, and its echoes are still discernible today [9].

The Father of Analog Integrated Circuits: Robert J. Widlar

At a time when even discrete solid-state op-amps had not yet succeeded in displacing their vacuum tube counterparts, and the very value of the integrated circuit idea was still a legitimate topic of debate, Bob Widlar ("wide-lar") almost single-handedly established the discipline of analog IC design. After receiving his bachelor's degree in 1962 from the University of Colorado at Boulder, he took a job with Ball Brothers Research, where his virtuosity at circuit design attracted the attention of engineers at one of their components suppliers. Despite the breach in protocol inherent in aggressively recruiting a customer's key employee, Fairchild induced Widlar to leave Ball in late 1963. In an amazing debut, abetted by Dave Talbert's brilliant process engineering, Widlar was able to put the world's first integrated circuit op-amp into production by 1964. Development of the µA702, as Fairchild called it, proceeded despite a general lack of enthusiasm for the project at the company.

The Fairchild µA702

Like the K2-W, this op-amp consists of two primary voltage gain stages (Figure 2). As in most differential designs, there is the problem of how to convert to a single-ended output without sacrificing half of the gain (the K2-W simply makes that sacrifice). Here the young Widlar solves this problem with a circuit that presages his later use of current-mirror loads. To the extent that Q3 and R3 behave as a high-gain amplifier (an "op-amp within the op-amp," if you will), the voltage at the base of Q3 moves much less than that at the collector. As an idealization, assume that the base voltage of Q3 simply doesn't move at all.

If an applied signal increases the collector current of Q1 by some amount, the drop across R1 then also increases. Since the base voltage of Q3 doesn't move much, the increased voltage drop across R1 shows up as an increased voltage at the top of R1. Now, differential symmetry says that an increase in Q1's collector current is accompanied by an identical decrease in Q2's collector current. The voltage drop across R2 consequently diminishes, supplementing the effect of the increased voltage at the top of R1. Hence, both halves of the differential pair contribute an increase in the signal that ultimately drives Q4, so that the differential-to-single ended conversion takes place (ideally) with no loss in gain.

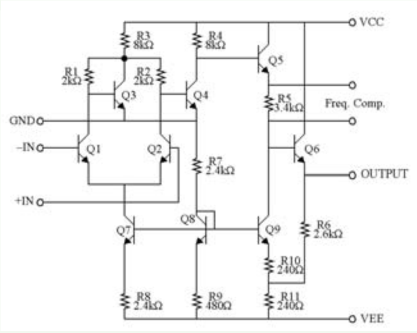


Figure 2: µA702A

The second gain stage is a textbook common-emitter stage.

As with the K2-W, the all-NPN 709 presents a level shift challenge; each successive gain stage tends to drive swings ever closer to the positive voltage rail. Widlar solves this problem with a resistor (R5) in series with a current source (Q9), rather than a neon-bulb network, to implement the downward-level shifting "battery." Widlar being Widlar, however, the level shifter is not quite a simple as that: the battery voltage is not constant.

A second emitter follower (Q6) provides reasonable output drive capability. The loop it forms with R6/R10/R11 and Q9 is a positive feedback loop (an homage to the K2-W). Thanks to the voltage gain boost provided by the positive feedback, typical gain exceeds 3,000.

Later versions of the op-amp provide access to the emitter of Q5 (as shown in the figure), allowing the user to shunt R5 with a small capacitance. This connection counteracts the effect of any capacitance present at the bottom end of R5, boosting stable closed-loop bandwidths to as high as 30MHz. This remarkable achievement would not be matched by IC op-amps for another decade.

The µA709 (1965)

Despite its innovations, the 702 was not a commercial success. Its initial price of approximately $150-$300 limited potential sales to military and aerospace customers. The relatively low gain and limited output drive capability, the somewhat peculiar power supply voltages (e.g., +12V/-6V), and the uncomfortably small input common-mode range (forced in part by the grounding of the emitters of Q3 and Q4), further constrained the part's appeal.

Widlar responded by developing the first analog IC that was a certified "smash hit." The 709 op-amp's generous open-loop gain (~ 60,000), respectable bandwidths (~1MHz) and an input common-mode range that accommodates positive voltages, made it a credible competitor to the K2-W in many applications (Figure 3). It was also the first IC op-amp to use the +/-15V supply voltages that

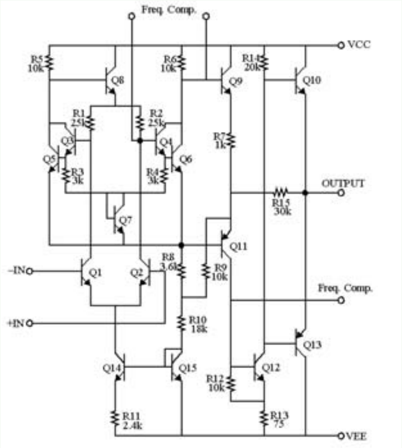


Figure 3: µA709

had recently emerged as a standard for many discrete solid-state op-amps (e.g., the GAP/R P65).

The 709 clearly shares a great deal with its progenitor, the 702, while going well beyond it. The resistively-loaded differential input stage (Q1/Q2, biased by current source Q14 which, in turn, is slaved to Q15), performs a differential-to-single ended conversion with a slightly more sophisticated implementation of the same idea used in the 702 (here, Darlington-connected Q3/Q5 and emitter follower Q8 together comprise the “op-amp within the op-amp”). Transistors Q3 and Q4 are biased to a low current without the use of large-value area-consumptive resistors by making the voltage across current-setting resistor R3 depend on the small difference between two diode voltages (those of Q5 and Q7). This same trick synthesizes a low current in Q14 without requiring absurdly large resistor values. This clever circuit (known, sensibly enough, as a Widlar current source) is an early expression of a Widlar IC-design rule: “Replace passives by transistors wherever and whenever possible”. This philosophy remains an important guiding principle of analog IC design.

The second gain stage is a resistively-loaded common-emitter amplifier using Darlington pair Q4/Q6. Emitter follower Q9 participates in a downward level shift, in conjunction with common-base lateral PNP transistor Q11. The 709 is the first commercial product in which a lateral PNP transistor makes an appearance (an IC for the Minuteman II missile had used one a bit earlier). Widlar’s design accommodates the dreadful characteristics of these early devices (made out of re-purposed NPN parts), which include a β that is nominally two. Widlar’s design allegedly continues to function (if one parses the word function generously) even if β is as small as 0.2.

To achieve the high open-loop gains demanded by users of op-amps, this design has a third gain stage, with Q12 in a resistively-loaded common-emitter amplifier. The presence of a third stage complicates using the 709, however, owing to the challenges of stabilizing a feedback amplifier that contains three cascaded stages. Widlar consequently makes externally accessible every high-impedance node in the op-amp to allow the user great flexibility in connecting a host of RC networks (many of them suggested by Fairchild in the 709’s data sheet and applications notes) to achieve satisfactory stability, bandwidth and settling time. Sometimes, the user even succeeded.

The output of the third gain stage drives a textbook complementary emitter follower. The PNP transistor Q13 can be (and is) implemented as a vertical PNP device, whose characteristics are better matched to those of an NPN than is a lateral PNP. A simple complementary buffer unfortunately possesses a well-known “dead zone” in its input-out-put transfer characteristic; there is roughly a 1.4V range of input voltages over which neither transistor conducts. Widlar employs local negative feedback around the output stage (through R15) in an effort to reduce the resulting distortion.

Fairchild’s applications notes make a game (and unintentionally amusing) attempt at moderating a user’s fears about the output driver’s robustness:

> *Although it is not clear from the schematic, the output stage is actually short-circuit-proof for a short period of time* [10].

Murphy guarantees that *your* short circuits will always persist just a little longer than that unspecified “short period of time.”

The spectacular success of the 709 quickly drove prices down as it drove production volumes up (despite yields that were simply terrible for a long time; Dave Fullagar assumed the task of solving the yield problem). This op-amp, introduced in November of 1965 at approximately $70 ($50 in large quantities), was the first to break through the $10 barrier (and then the $5 barrier by 1967), guaranteeing extremely widespread use. By 1969, op-amps were selling for around $2. Unable to compete against exponential price reductions, the K2-W was retired in 1971, its twentieth year of continuous production.

Widlar didn’t just work on op-amps at Fairchild, he also designed a popular pair of comparators (the 710 and the 711), whose 40ns response time represents an order-of-magnitude improvement over the speeds achieved by contemporary general-purpose op-amps reluctantly impressed into service as comparators.

Widlar’s last design for Fairchild, the µA726, rolled out in 1965. The high-precision differential pair’s on-chip temperature-controlled heater enables offset drifts of 0.2µV/°C over the entire military temperature range. In two years, Widlar had put five ICs into production and firmly established analog IC design as a legitimate (and profitable) discipline.

He was just warming up.

The LM101 (1967) and LM101A (1968)

The success of the 709 emboldened Widlar to request a substantial upgrade in his compensation. When Fairchild declined to provide it, he and Talbert left the company in December of 1965 for what eventually became part of National Semiconductor. His first IC for National was a voltage regulator (the LM100). His next design was an op-amp intended to repair several shortcomings of the 709. He sought to outdo his earlier creation by providing a larger input common-mode range, lower input current, higher open-loop gain and

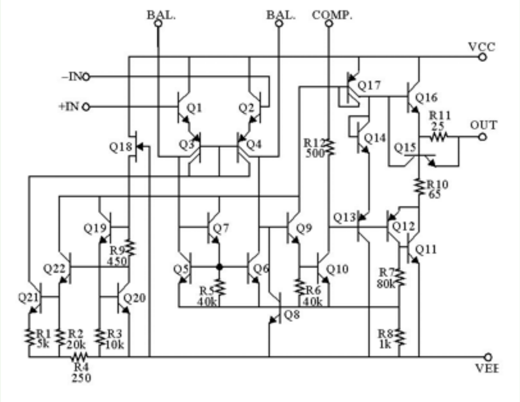


Figure 4: LM101A

simpler compensation. Finally, he wanted to protect the part against output short-circuits of arbitrary duration. The LM101 was the result, with an improved version, the LM101A, following within a year (Figure 4).

A good way to solve the level shift problem is to alternate NPN- and PNP-based stages, whose common mode shifts can cancel. Unfortunately, the poor performance of lateral PNPs normally precludes their use. Widlar's circuits manage to use these inferior PNPs in ways that mitigate their deficits to a surprising degree.

The LM101A's input stage magically mimics a PNP-based differential amplifier by combining good NPNs with the level-shifting polarity of the not-so-good PNPs. The pair of NPN input emitter followers (Q1/Q2) enable low base current, and the differential common-base configuration of PNPs (Q3/Q4) solves the level-shift problem. The fast common-base configuration also minimizes the bandwidth impact of the slow PNPs.

The LM101 is the first op-amp to use active loads, enabling much higher gains per stage, and also the first to use a mirror load to perform differential-to-single ended conversion. These remain standard analog circuit idioms, forty years after the LM101's debut.

The second stage similarly achieves high gain, thanks to current-source load Q17. Two level-shifting devices, Q13 and Q14, function to bias the complementary emitter follower (Q11/Q12/Q16) to avoid the dead zone problems of the 709.

Again because of the poor characteristics of PNPs, the output follower departs somewhat from standard textbook configurations: the pulldown device is a *compound PNP* (also known as a complementary Darlington pair) – a combination of an NPN (Q11) and a PNP (Q12) that mimics the basic polarities of a PNP. At the same time, the overall effective β is the product of NPN and PNP β's, allowing the combination to possess the good current drive characteristics of an NPN.

A welcome refinement is the ability to tolerate output short circuits to ground indefinitely, instead of the 709's "short period of time." This feat is accomplished by explicitly limiting the maximum output current to a sustainable value. Transistor Q15 is normally off, but if the op-amp attempts to source a current in excess of about 25mA, the drop across R11 causes Q15 to turn on. Doing so robs Q16 of base current, limiting further increases in output source current.

To protect the op-amp from *sinking* excessive current is a little more involved. If the voltage drop across R8 gets large enough, Q8 turns on and steals current from the base of Q9, thus ultimately limiting the output sinking current to a safe value. The LM101A tolerates short circuits to ground for *any* length of time.

Thanks to the current-source loads, two stages suffice to provide a nominal DC gain of over 500,000 (limited, in fact, by thermal feedback). The small number of stages (two) simplifies frequency compensation, which is provided by connecting a suitable network between the collector of Q4 and the pin labeled "comp." In many cases the network can be as simple as a single Miller compensation capacitor. Widlar's achievement is all the more remarkable for its having been accomplished with no computer simulation tools.

The chief difference between the 101A and the 101 is a modified input bias generator. The 101's first-stage bias current is roughly constant, but the strong positive temperature coefficient of β results in a base current with a strong negative temperature coefficient. To produce a more constant input current, Widlar biases the 101A's input stage with currents that are proportional to temperature. Transistors Q19-Q22 effectively form a thermometer to provide the desired behavior. As a bonus, the transconductance of the input stage, which is proportional to I_{bias}/V_T, also becomes much more temperature independent.

If R4 and R9 may be neglected for the moment, the voltage that appears across R1 is the difference between two pairs of diode voltages. Such a voltage is PTAT (proportional to absolute temperature), so the current through R1 would itself be PTAT if the resistance were stable over temperature.

Resistor R9 is added to reduce supply voltage sensitivity. As the supply voltage increases, the current through Q18 increases. The voltage at the base of Q22 would consequently increase, causing an undesired increase in amplifier bias currents. Inserting R9 provides an additional voltage drop that reduces the base voltage of Q22, thus offsetting the increase in Q18's current. Indeed, in the limit of very large current in Q18, the currents in Q21 and Q22 ultimately tend toward zero. A plot of output current vs. input current reveals a definite maximum (at an input current V_T/R9), so this type of current source is known as a "peaking current source." At the peak, the output current has a zero first-order sensitivity to input current. Centering the nominal input current about this peak provides supply-insensitive bias. Familiarity with the peaking current source is not nearly as widespread as it should be. The basic principle even works in CMOS technology.

"Easy to use" wins: The µA741 (1968)

Back at Fairchild, Dave Fullagar had successfully debugged the 709's process problems. He learned of National's 101 and,

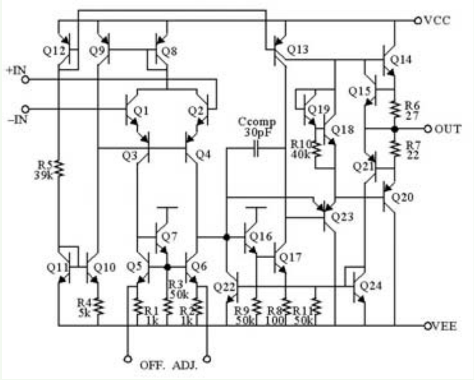


Figure 5: One variant of the 741

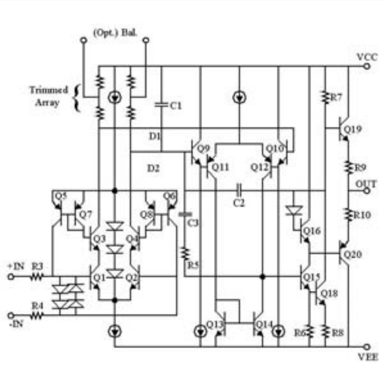


Figure 6: OP-07 (simplified)

according to his colleague George Erdi, wondered why it did not include an on-chip compensation capacitor. He felt that Fairchild's process technology could practically accommodate this goal, and speculated that National's could not yet do so [9]. His answer to the LM101 was the 741, the most popular op-amp of all time. Fullagar chose to retain the key architectural features of the LM101: the input stage is the same compound differential combination of an NPN emitter follower and PNP common-base amplifier, a mirror load provides high gain and single-ended conversion, and the second stage remains a current-source loaded common-emitter amplifier (Figure 5). A straightforward complementary emitter follower provides an output drive current that is limited to the same maximum value, and in the same asymmetrical way, as in the 101.

There are some differences, to be sure. Rather than using an elaborate replica bias circuit, the input stage employs simple feedback biasing to establish the base and collector currents. A Widlar mirror converts the ~700µA master current in Q11, Q12 and R5 into a 20µA collector current in Q10. Transistors Q1 through Q4 act collectively as a single PNP transistor for common-mode inputs, and act together with Q8 and Q9 to form a Wilson mirror. The feedback connection of the Wilson mirror supplies the appropriate PNP base current automatically. George Wilson no doubt would have found the combination of the two mirrors amusing (if dissonant), as his own invention (at Tektronix) was stimulated by the appearance of the Widlar mirror in the 709.

Those minor differences aside, the chief appeal of the 741 is its internal compensation capacitor. The popularity of the 741 validates Fullagar's implicit assumption that engineers are basically lazy (that is, very time-efficient). Engineers seem not to mind that a fixed capacitor degrades performance in most configurations. Ease of use, coupled with "good enough" performance, seems to be more important.

After a subsequent tenure at Intersil, Fullagar went on to co-found Maxim Integrated Products.

The Quest for Precision: The OP-07 (1975)

Although it is certainly true that Bob Widlar gets credit for a disproportionately large share of the analog IC innovations of the 1960s and 1970s, it would be terribly unfair to convey the impression that no one else was contributing to the development of the art. Fullagar's 741 and George Erdi's OP-07 from Precision Monolithics (now a part of Analog Devices) show that others were hard at work as well (Figure 6).

The three-stage OP-07 introduces two valuable techniques. One is the use of active base current cancellation. The other is trimming to reduce offsets by more than an order of magnitude over conventional approaches.

Current at the input terminals is reduced by well over an order of magnitude by measuring it, and then supplying it internally. That is, the amplifier makes use once again of a special-purpose analog bias computer within the op-amp. Here, transistors Q3 and Q4 are not conventional cascodes at all. Rather, they are dummy devices whose sole purpose is to allow the measurement of base current. To the extent that the base currents of the cascoding transistors match those of the main input transistors (Q1/Q2), then the mirrors Q5/Q7 and Q8/Q6 will supply to the bases of Q1 and Q2 precisely the right amount of current. The external sources driving the op-amp input terminals only have to supply (or sink) the current resulting from incomplete cancellation.

The resistively loaded first stage contains numerous series-connected resistive segments, each having a reverse-biased junction in parallel with it. At wafer test time, the offset of the amplifier is measured, and an algorithm computes which resistive segment(s) should be shorted out to minimize the offset. Thanks to the magic of bipolar device physics, nulling out an offset this way tends also to minimize offset drift (if only it were so with MOS transistors). Then, a large current is passed through the corresponding reverse-biased junction, causing the aluminum metalization to spike through the junction and short out the resistor in question. Although it may seem that this brutal "zener-zapping" couldn't possibly be reliable, it allows the routine and robust attainment of sub-100µV offsets, even if it's a bit rough on probe tips.

The second gain stage is a follower-driven PNP differential amplifier. Conversion to a single-ended output is performed the usual way, with an NPN mirror. Erdi bypasses around the slow PNP stage at high frequencies with R5 and C3, effectively turning the OP-07 into a two-stage op-amp where it matters. Miller compensation is provided around the remaining two stages with capacitor C2, and the dynamics of the overall amplifier are much like those of a 741 when all is said and done. The resistively-loaded common emitter third stage (Q18/R7) drives a standard complementary emitter follower Q19/Q20 to complete the op-amp.

The combination of high gain, very low offset and low drift, coupled with 741-like dynamic behavior, assured the enduring popularity of this op-amp.

George Erdi left PMI in 1981 to co-found Linear Technology.

Voltage References

The op-amp may be the archetypal analog circuit, but it is certainly not the only important one. Voltage references are needed just about everywhere, if for no other purpose than to set supply and bias voltages to desired values. Data converters fundamentally require them also, if the mapping between bits and volts is to have any absolute quantitative meaning.

Somewhat ironically, the rising prominence of digital logic stimulated important advances in analog integrated circuits. As the digital revolution started to gain a head of steam in the late 1960s the need for regulated +5V supplies to power up the growing "gate farms" of TTL ICs became increasingly acute. Widlar foresaw a need for a simple, adjustment-free regulator chip, and set about to design it.

The problem, of course, is how to implement the fundamental voltage reference. Conventional alternatives, such as the zener diode, provide "reference" voltages after a fashion, but the actual voltages are not traceable to any reliable physics. The loose tolerances preclude realization of trim-free circuits without expensive component selection. A diode's forward drop of "about 0.6V" might be somewhat more reliable (then again, maybe not), but the large negative temperature coefficient (of about 0.3%/°C) limits the useful temperature range.

As were most analog engineers, Widlar was well acquainted with a diode voltage's large negative temperature coefficient. Rather than being stymied by it, however, he used this behavior as a starting point. A common rule of thumb is to expect about a 2mV drop in forward voltage for every degree Celsius increase in temperature. The temperature coefficient is current-dependent (higher currents decrease its magnitude), but for a given fixed value of current, the temperature coefficient is nearly constant over an extremely wide temperature range. This type of behavior has been dubbed CTAT, for *complementary to absolute temperature*. More remarkable than this near-linear behavior is that the value of forward voltage extrapolated to absolute zero is the same for all diodes, and equal to the bandgap. The appearance of a voltage that is traceable directly to reliable physical constants (the bandgap, in this instance) is what makes trim-free voltage references possible.

To exploit these observations to make a voltage reference one must add a voltage that is PTAT (proportional to absolute temperature) to one that is CTAT. We've already witnessed Widlar's familiarity with PTAT current sources, for they are part of the bias circuitry in the LM101A. Without putting too fine a point on it, if you add a line that goes up, to a line that goes down, the sum will still be a line. And if the lines have equal and opposite slopes, the sum will be a constant. This flat condition occurs if the voltages sum to the bandgap voltage which, for silicon, is about 1.2V [we ignore in this discussion the second-order effects that one must consider when seeking to design a good bandgap reference].

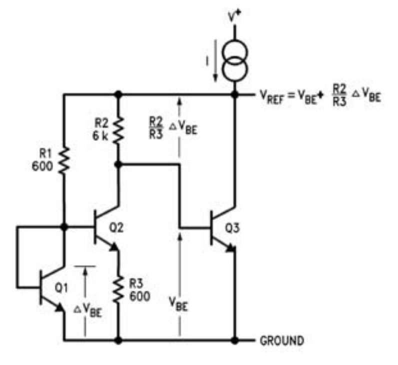


Figure 7: Simplified Widlar bandgap voltage reference

Widlar's translation of this recipe into circuit form appears in Figure 7 [11][12].

A Widlar current source (Q1 and Q2) establishes a voltage across R3 that is the difference between two junction voltages. The associated current is PTAT, as desired, but some scaling is needed to obtain the correct slope. To the extent that emitter and collector currents are substantially equal, the voltage across R2 is simply PTAT as well, but scaled by the ratio R2/R3. This voltage is added directly to the base-emitter voltage of Q3, so that the output reference voltage is the sum of a CTAT component (Q3's VBE) and a PTAT one (a scaled ΔVBE). When the ratio R2/R3 is chosen to produce an output voltage of about 1.2V at any one temperature, the output voltage remains very close to that value at all temperatures. This bandgap cell lies at the heart of Widlar's LM109, the first three-terminal, trim-free voltage regulator IC. Variable volts may go in, but a constant 5V comes out. As a bonus, the LM109 offers both current limiting and thermal overload protection, making the part robust as well as easy to use.

The instant popularity of the LM109 speaks to the brilliance of Widlar's particular implementation of the bandgap reference principle (and to his marketing insights). Nevertheless, Paul Brokaw of Analog Devices understood that the bandgap's full potential remained to be realized. Brokaw set about systematically identifying effects that degrade performance. In bipolar transistors, collector current and base-emitter voltage are fundamentally linked through dependable physics, but the Widlar cell depends on a secondary linkage between emitter and collector current, making it vulnerable to errors

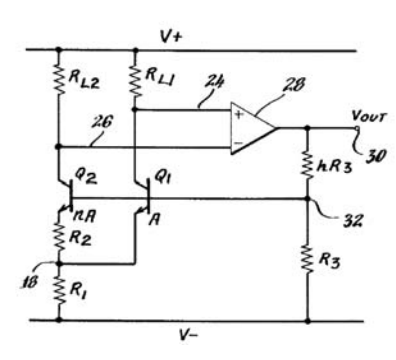


Figure 8: Brokaw bandgap cell [13]

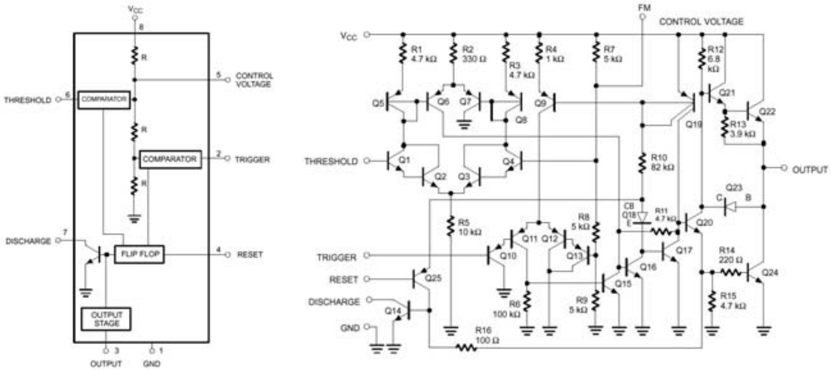


Figure 9: NE555 timer chip; block diagram and schematic (from the Philips Semiconductor datasheet)

of the second order. The simplified schematic of Figure 7 shows that nonzero base current is an important source of such errors

Within a short time, Brokaw devised an alternative implementation of the bandgap reference that does not suffer from these sensitivities (Figure 8):

This elegant circuit evades many of the second-order effects that degrade the Widlar cell's performance. Assume for simplicity that the collector load resistors RL1 and RL2 are equal. The negative-feedback loop involving the op-amp assures an equality of collector voltages, and thus, an equality of collector currents. The two transistors have unequal emitter areas, however, so the current *densities* are unequal. In turn, operation at different densities assures a calibrated difference in base-emitter voltages. This difference appears directly across R2, giving us a PTAT voltage, and an associated PTAT current through the resistor (and thus, through Q2).

The currents through Q1 and Q2 are equal and PTAT, and the current through R1 is therefore PTAT as well. From examination of the circuit, it should be clear that Brokaw has cleverly arranged for the common base connection to have a voltage expressible directly as the sum of a PTAT term (the voltage across R1), and a CTAT term (the base-emitter voltage of Q1). By ratioing R2 and R1 properly, the bandgap voltage appears at the base connection. If desired the feedback to the base from the op-amp can include the voltage divider shown, allowing the overall output voltage to be a multiple (here, 1+h) of the bandgap voltage. The AD580 2.5V reference from Analog Devices has the distinction of being the first product to use the Brokaw bandgap cell, with the highest-accuracy versions offering total errors (including drift) of about 0.5% over the entire military temperature range.

The best-selling IC of all time

Almost every EE or hobbyist has encountered the 555 timer IC at some point, either in a lab class, or "just hacking around." Few of them, however, probably know much about who designed it, and how it came to be. And even fewer probably know that the 555 remains by far the best-selling integrated circuit in history, with about a billion units still sold each year, more than 35 years after its introduction.

The creator of the 555 is Hans Camenzind, who joined Signetics in 1968 with the intention of building the world's first integrated phase-locked loop (PLL). The NE565 PLL debuted in 1970, and quickly found widespread use in diverse applications. For example, the famous Altair 8800 computer that is often credited with kick-starting the PC revolution had an optional cassette tape interface for data storage. The two-tone frequency shift keyed (FSK) data was demodulated with a 565-based circuit. Today, PLLs are so widely used that it is hard to identify systems that don't have one or more of them. Camenzind's 565 went a long way toward converting PLLs from analog exotica into common functional blocks.

After putting the 565 into production, Camenzind took a leave of absence to write a book. He decided not to return to Signetics as a full-time employee but did agree to work for them on a contract basis. It was during this time that he designed the 555 timer chip (Figure 9). The proximate motivation was an outgrowth of his PLL work, with its recurrent need for stable, voltage-controlled oscillators. Camenzind expanded the scope of the project to make the chip a general-purpose timer IC. No marketing study guided this decision. He needed such a component, and he simply assumed that others likely would, too [14].

Engineers quickly discovered that the particular complement of blocks chosen by Camenzind allows the 555 to perform a remarkably wide range of functions well beyond acting merely as a PLL adjunct. It is hard to imagine that any sort of marketing study would have resulted in its choice of two comparators, a flip-flop, a totem-pole output driver, and an open-collector transistor. And yet, somehow, this particular collection of analog atoms has enabled generations of engineers, hobbyists and tinkerers to create a rich variety of circuits and systems. Future archeologists, puzzled and intrigued by the seeming ubiquity of the 555, no doubt will conclude that it was the glue that held civilization together.

Bill and Dave, and the Wien bridge

The story of how Bill Hewlett and Dave Packard got their start is the stuff of legend. The two Stanford engineering students were encouraged by their advisor, Fred Terman (often known as "the father of Silicon Valley"), to found a company of their own. Hewlett had already designed an audio oscillator, and the pair chose that instrument as HP's first product. They dubbed it the model "200A" to mask the fact that it was the company's first product. A year later, in 1939, the sale of eight model 200B oscillators to Walt Disney Studios set the company on the path to history.

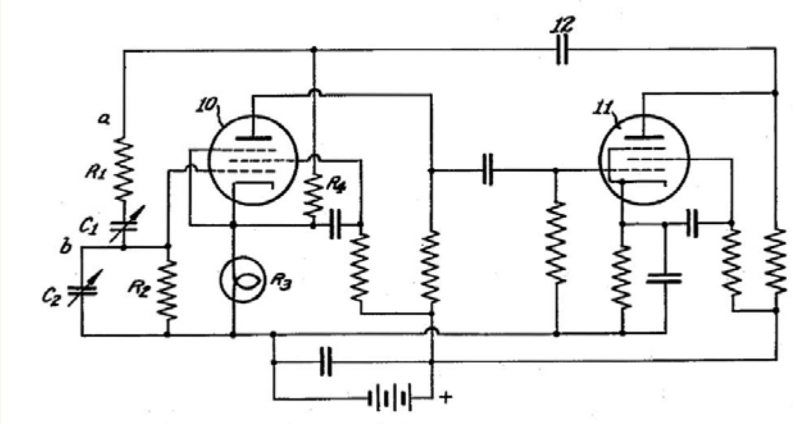


Figure 10: Hewlett's Wien-bridge oscillator [15]

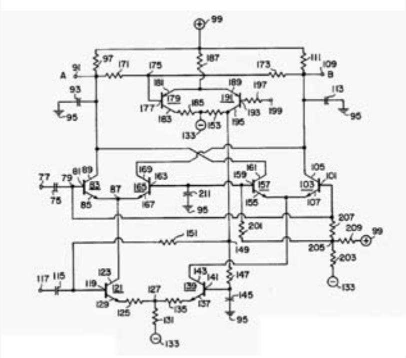


Figure 11: Circuit due to Jones [17]; input and output quantities are voltages

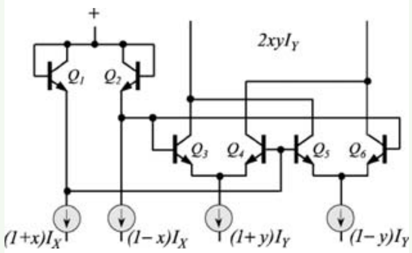


Figure 12: Gilbert cell example (with predistorting pair Q1/Q2); variables are currents [18]

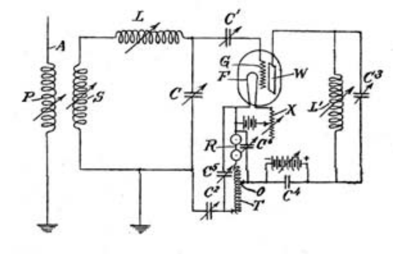


Figure 13: Armstrong's first great invention: Regeneration [19]

Many engineers have made amplifiers oscillate by accident, so building an oscillator on purpose might seem easy. However Murphy guarantees that, much like washing your car in order to make it rain, things often don't work as desired. Hewlett's HP200 not only oscillates, but generates low-distortion sine waves over decades of frequency.

The core of the oscillator, not surprisingly, is a positive feedback loop (Figure 10); there is no net inversion in going from the control grid of vacuum tube 10 to the plate of vacuum tube 11.

A bandpass filter R1-C1-R2-C2 closes that feedback loop. Use of this type of RC network in a bridge configuration for measuring impedances was reported in 1891 by Max Wien (perhaps the most often misspelled name in the EE literature) [16]. The useful feature of this network here is the zero phase shift it exhibits at the bandpass filter's center frequency, allowing oscillation there. To produce a low-distortion sinusoidal output, the amplitude of this oscillation needs to be controlled by some mechanism. One could imagine an infinite variety of methods for doing so, but it's hard to imagine a more clever, elegant solution than Hewlett's: Monitor the amplitude with a *lightbulb*, and exploit the latter's thermal sensitivity to servo the amplitude to a controlled value. The oscillator thus has two feedback loops – a positive feedback loop to enable oscillation in the first place, and a negative feedback loop to stabilize the amplitude of that oscillation.

Resistors R4 and (lightbulb) resistor R3 close the amplitude control loop. It is perhaps noteworthy that this loop uses current-mode feedback to the cathode of vacuum tube 10; the technique is therefore not nearly as modern as some seem to think. If the amplitude grows, the bulb's filament heats up, and the corresponding resistance increase causes the magnitude of the negative feedback to increase as well, opposing the amplitude increase. The nominal bulb current is so low that no visible glow is evident, and the bulb's lifetime typically well exceeds that of other components in the instrument.

The Gilbert and Jones Multipliers/Mixers

A circuit that resides at the intersection of analog computation and communication is the mixer. A multiplier is in fact a mixer; the choice of nomenclature is primarily a matter of context. When it comes to mixers (or multipliers), almost every communications engineer immediately thinks of the "Gilbert cell" or "Gilbert mixer." However most textbooks, and a great many journal and conference papers, actually describe an earlier invention by Howard E. Jones, instead of Barrie Gilbert's superficially similar multiplier (see Figures 11 and 12) [17][18].

The difference is seemingly trivial, but is in fact profound: Gilbert's brilliant insight is that representing variables entirely in the current domain can enable spectacular linearity, despite the famous exponential nonlinearity of bipolar transistors. The fundamental idea may be viewed as employing predistortion to undo precisely the inherent nonlinear transfer characteristics of the core circuitry. The reliable nature of a bipolar device's nonlinearity enables such cancellation to succeed.

Despite earnest attempts by Gilbert himself to correct this misapprehension, it is hard to undo decades of error overnight [18].

Analog Electronics in Communications

What we call electronics today was once mainly wireless. The Widlar of wireless was Edwin Howard Armstrong, who explained to Lee de Forest, inventor of the triode vacuum tube how it actually worked, and then exploited that understanding to invent circuits and systems that still dominate today. Those contributions include the superheterodyne receiver (which popularized the mixer), and wideband FM. His first important discovery, however, was the boost in amplification provided by positive ("regenerative") feedback, using circuits such as shown in Figure 13 [19].

This circuit uses a transformer *T* to couple signals from the plate ("wing," *W*) back to the cathode (filament, *F*). As far as this feedback loop is concerned, the vacuum tube operates as a (non-inverting) common-grid amplifier, and so the connection constitutes a gain-boosting positive feedback amplifier.

Thanks to regeneration, the vacuum tube transformed from an expensive, erratic curiosity into the very basis for a new field – electronics. Early vacuum tubes struggled to evince voltage gains of five when used without feedback, but regeneration enabled arbitrary gains – even oscillation. For the first time, engineers had fully electronic high-gain amplifiers and compact oscillators at their disposal, allowing electrical engineering to move rapidly beyond its power-engineering origins. Positive feedback's importance is underscored by the difficulty of engineers to appreciate the value of negative feedback. The idea of throwing away precious gain seemed absurd to a generation of engineers who had enjoyed high gain for the first time. Paradigm shifts of that magnitude take time.

Armstrong's invention of the superheterodyne receiver in the closing days of the first World War is all the more remarkable for its overwhelming dominance even as it approaches its 90th year. Unprecedented ease of operation conferred by the single required tuning control, coupled with circuit improvements and cost reductions made possible by better vacuum tubes, made the superhet the dominant architecture by 1930. Generations of engineers have never known another.

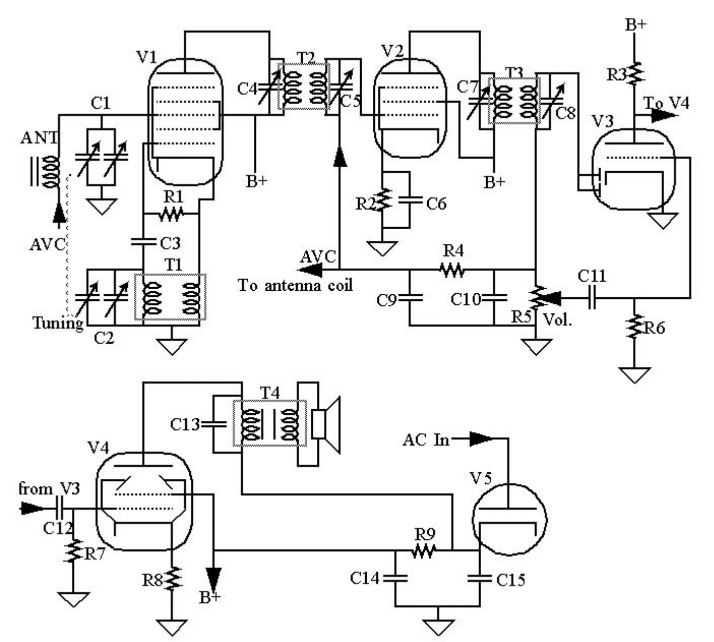


Figure 14: The "All-American Five"

Modesty wins again

Decades after Armstrong's invention of the superhet, and decades before the iPod, there was the "All-American Five." For about thirty years, this AM receiver was the most popular tabletop radio. The All-American's complement of five vacuum tubes kept costs low, while delivering satisfactory performance (Figure 14).

The first tube is a pentagrid converter, which acts as both local oscillator and mixer. In some sense, it may be viewed as an early integrated circuit. The local oscillator part of this circuit is an echo of Armstrong's original regenerative oscillator. The cathode current couples back to the first grid through transformer T_1 whose tuned secondary controls the oscillation frequency and, therefore, the channel selected, as in all superhets. Simultaneous tuning of a simple bandpass filter at the RF input port aids image rejection. The tuning capacitors for both circuits are mechanically linked ("ganged") so that the consumer only has to turn one knob to change frequency.

Grid 2 is incrementally grounded, and acts as a Faraday shield to isolate the oscillator and RF circuits. The RF signal feeds grid 3, and nonlinear interaction within the tube performs the mixing action. Grids 4 and 5 are incrementally grounded, and remove the Miller effect and suppress secondary electron emission, respectively.

The output of the first stage is coupled through a doubly-resonant IF bandpass filter to a single IF amplifier, a 12BA6 (V2), operating at 455kHz. The 12BA6 is a pentode, and thus behaves much like a cascode, allowing one to use filters on both the input and output ports without worrying about detuning or instability from feedback.

Demodulation and audio amplification take place in V3, a 12AV6, which contains two diodes and a triode within one glass envelope. The diodes perform envelope detection, and the triode amplifies the demodulated audio. The demodulated output in turn feeds two destinations. One is the output power amplifier, V4. The other is an additional low-pass filter, the output of which is the average of the demodulated output. This signal is used to control automatically the gains of the front-end and IF amplifier as a function of received signal strength. The greater the demodulated output, the more negative the bias fed back to those stages, reducing their gain. This automatic gain control (AGC) or automatic volume control (AVC) thus reduces potentially jarring variations in output amplitude as one tunes across the dial.

V4 is a 50C5 beam-power tube used in a Class A audio power amplifier configuration. Transformer coupling provides the necessary impedance transformation to deliver roughly a watt of audio into the speaker.

A 35W4 (V5) power rectifier generates the B+ plate supply for the other tubes.

With minor variations, the All-American was widely copied, and clones could be found all over the world. Once it caught on, high manufacturing volumes drove down the cost of these five particular tube types, so anyone designing a new radio intended for a cost-sensitive application tended to use the same tubes, and thus used similar circuits. Variations among different versions are really quite slight (e.g., small resistor or capacitor value differences, absence or presence of cathode resistor bypass capacitors, etc.), and the basic schematic of Figure 14 suffices for most troubleshooting purposes.

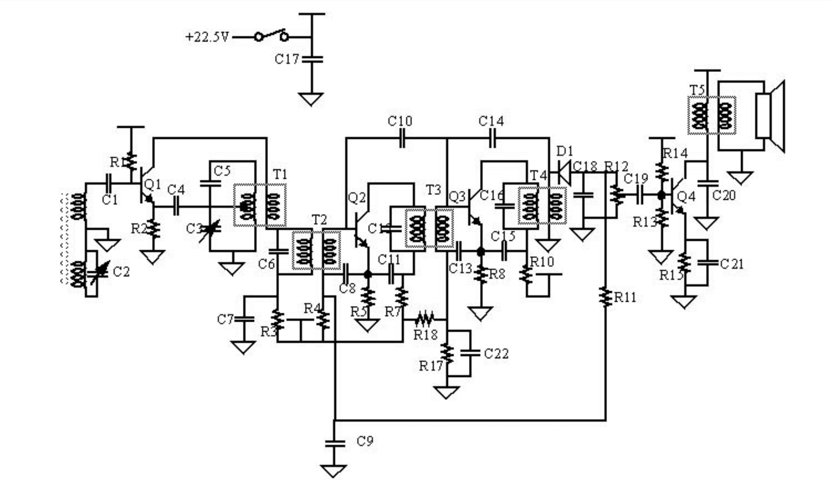


Figure 15: Schematic of the Regency TR1 [20]

Early Personal Audio: The Regency TR-1 Transistor Radio

The first portable transistor radio became available in time for Christmas in 1954 and was the result of a conscious effort by a young Texas Instruments to create a mass market for transistors. Up to this time, the only commercial use for transistors had been in hearing aids. As the father of the project, Patrick Haggerty, later noted, the thinking was that "...a dramatic accomplishment by [us would] awaken potential users to the fact that...we were ready, willing, and able to supply [transistors]" [20]. TI arranged a deal with a small company called IDEA (Industrial Development Engineering Associates), whose Dick Koch modified TI's first-pass circuit (principally designed by Paul D. Davis and Roger Webster) to reduce cost and improve manufacturability. The task was challenging as no one had much expertise with transistors yet. To make a tough job even more difficult, the germanium transistors then available were quite poor by today's standards (f_T's of only a few MHz at best, and β's of 10-20), while their cost was high. Compounding those difficulties was the lack of off-the-shelf miniature components to complement the small transistors. It was quite a struggle to cram all of the circuitry into a case small enough to fit in a shirt pocket (indeed, early advertisements used a custom-made shirt with oversized pockets). In a first for consumer electronics, printed-circuit technology was chosen for the TR1 in order to facilitate interconnecting such densely packed circuit elements. The newness of the technology presented many daunting manufacturing challenges.

Calculations showed early on that no more than four transistors could be used or IDEA and its Regency division would not be able to make a profit at the targeted sale price of $49.95. The four transistors accounted for about half of the cost of the materials. At a time when an All-American Five could be purchased for about $15, it was difficult to imagine that there would be a significant market for such an expensive device. As it happened, demand outstripped production capacity for quite some time.

As seen in Figure 15, four transistors were enough. In this circuit, the first transistor, Q1, functions as an oscillator-mixer, just as the first tube does in an All-American Five. Transformer coupling between collector and emitter circuits provides the positive feedback necessary for oscillation.

The incoming RF signal is tuned using a mechanism called "absorption," developed by the German company Telefunken around World War I. In this technique, an LC tank coupled to the input circuit shorts out (absorbs) signals at all frequencies other than the resonant frequency of the tank. The RF signal can pass to the base of Q1 only when this shorting disappears, at the absorbing tank's resonant frequency (determined by C2). The inherent nonlinearity of the base-emitter diode provides the mixing action. Hence, in addition to the local oscillator signal, the collector current also has a component at the sum and difference heterodyne terms. The difference signal is then fed to the first IF amplifier, Q2, through an *LC* bandpass filter tuned to the IF of 262kHz. The unusually low IF allows the low-f_T transistors to provide useful amounts of gain, but exacerbates an already bad image rejection problem. The variable capacitor in the absorptive LC front-end tank is ganged with the LO variable capacitor. The degree of image rejection achieved here is best described as adequate.

The second IF amplifier, Q3, is connected in a manner essentially identical to Q2. The large $C\mu$ values (probably about 30-50 pF) are partially cancelled by positive feedback through *C*10 and *C*14 (a technique introduced in the 1920's as the Neutrodyne circuit).

A standard envelope detector performs demodulation, and then feeds a single stage of audio amplification. Transformers couple signals into the detector and out of the audio amplifier.

AGC action is provided in a familiar manner: the demodulated audio is further RC filtered (here by R_{11} and C_9), and the resulting negative-polarity feedback signal controls the gain of the first IF stage by varying its bias.

The success of the TR-1 had important consequences beyond establishing TI as a leader in the semiconductor business. Of particular significance is that IBM quickly abandoned development of new vacuum tube computers, with Thomas Watson, Jr. reasoning that if transistors were mature enough for high-volume consumer gear, it was time to consider them for computers. As he later told the story, every time one of his subordinates expressed doubt about transistors, he'd give him a TR-1, and that usually settled the argument [21].

A young company called Sony introduced their own transistor radio, the TR55, soon after Regency's TR1 debuted. The company would soon dominate the consumer market for portable electronics.

Sophisticated Low Tech: Three-Transistor Toy Walkie-Talkie

Although vacuum-tube "toy" walkie-talkies had appeared as hobby projects in the years following the second World War, they were too expensive for anyone to consider manufacturing them in volume as actual toys for children. The development of the transistor made such a toy a practical possibility. Jerry Norris, an engineer at Texas Instruments, was the first to act on this insight, and in so doing developed in 1962 the ancestor of all toy walkie-talkies [22]. This widely copied and ingenious circuit uses a single-transistor *superregenerative* amplifier/detector (yet another Armstrong invention), followed by two stages of audio amplification in receive mode (see Figure 16). When transmitting, the superregenerative stage becomes a stable crystal-controlled 27MHz oscillator, amplitude-modulated by an audio amplifier built out of the other two transistors. The speaker doubles as a microphone in this mode.

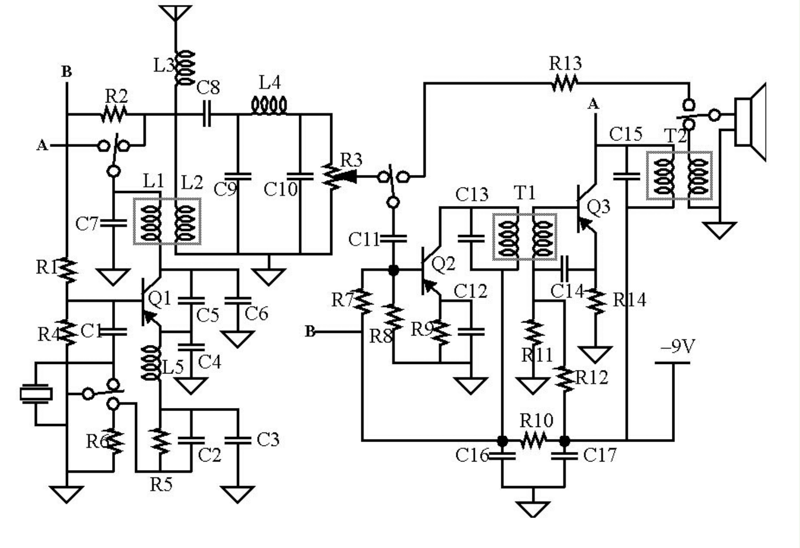


Figure 16: Jerry Norris' superregenerative CB walkie-talkie [22]

Transistor Q1 does all the RF work in this circuit. In receive mode, Q1 is configured as a Colpitts oscillator with *unstable* bias. An incoming RF signal establishes an initial condition from which oscillations build up exponentially, providing remarkable sensitivity. The bias is arranged to cut off ("quench") the oscillations periodically at a rate high enough to sample the modulation at a super-Nyquist rate (this periodically quenched oscillation distinguishes superregeneration from regeneration). Thanks to ever-present nonlinearities, the transistor also amplifies the modulated RF signal asymmetrically. Hence, the collector current contains a component roughly proportional to the modulation itself. A low-pass filter consisting of C_9, L_4 and C_{10} removes the RF component, passing only the modulation to the two-transistor audio amplifier made of Q2 and Q3.

While Q1 acts as a self-quenched LC oscillator in the receive mode, a quartz crystal is used to control the frequency of oscillation during transmit. Resistor R_6 is shorted out during transmit to prevent quenching.

The oscillator amplitude is roughly proportional to the collector supply voltage, so varying the supply voltage with an audio signal from Q2/Q3 amplitude-modulates the carrier. Although the distortion from this process hardly meets the standards of high fidelity audio, it is certainly adequate for voice communications, and most definitely adequate for a toy.

Because this simple circuit provides such large gain with so few transistors, it continues to dominate the toy walkie-talkie market, having been copied and modified countless times by manufacturers. The influence of Norris' circuit is evident from having traced over twenty superregenerative walkie-talkie circuits over the years. In all of them, just one transistor does all of the RF work, with the remaining two (sometimes three) transistors serving as audio amplifiers. As with the All-American Five, variations among different manufacturers are relatively minor.

The world is analog

Although it is perhaps a little ironic that the story of linear circuits itself seems to have been so nonlinear, a linear narrative would have been a distortion of history (beyond those already committed). As the world allegedly "goes digital," these histories help remind us that we live in an analog world, after all.

Analog epilogue: A bit more about Widlar

Widlar essentially created the analog IC business, and so perhaps it is appropriate to say a little more about him in this sidebar.

The individualism evident in his circuit designs reflects his independent, idiosyncratic personality. While still at Fairchild, he acquired a reputation as a hard-working, hard-drinking prankster. By the time he'd joined National Semiconductor, his antics were well on their way to becoming legendary, as is evident from a sidebar accompanying an August 1968 article by him in *EEE* ("Bob Widlar of National Semiconductor speaks out on what makes a good IC").

He was famous for total immersion when working on a design. He could work nonstop into a state of such exhaustion that he found relief by driving his beloved '66 Mercedes 280SL convertible to the airport and purchasing a ticket for "the next flight out."

The mere fact of his having a gun collection might have made some of his colleagues a bit nervous; knowing that he used, for target practice, beer cans with the names of those not in his esteem probably unnerved the rest.

The reporter who interviewed him noted that Widlar's apartment was stocked only with scotch, beer and glasses. "His refrigerator is bare if you don't count the ice cubes." This comment only hinted at the magnitude of Widlar's ability to imbibe.

When National, along with the rest of the electronics industry, suffered during a recession a couple of years later, the groundskeeping staff was eliminated as part of a corporate cost-cutting plan. Widlar didn't like the unkempt look of the facilities as the weeds grew. His response was to drive with Bob Dobkin to someplace south of San Jose and purchase a sheep (some say it was a goat, but look at the photo in Figure 17 and decide for yourself). Upon returning to National, "someone" called a reporter at the San Jose Mercury News, and a photographer appeared soon after to document National's new lawn-mowing technology in action.

The groundskeeping staff was rehired soon afterwards.

Later that day, Widlar took the sheep with him to Marchetti's, a popular National watering hole in those days. He left it with the bartender. History does not record what the bartender did with the sheep.

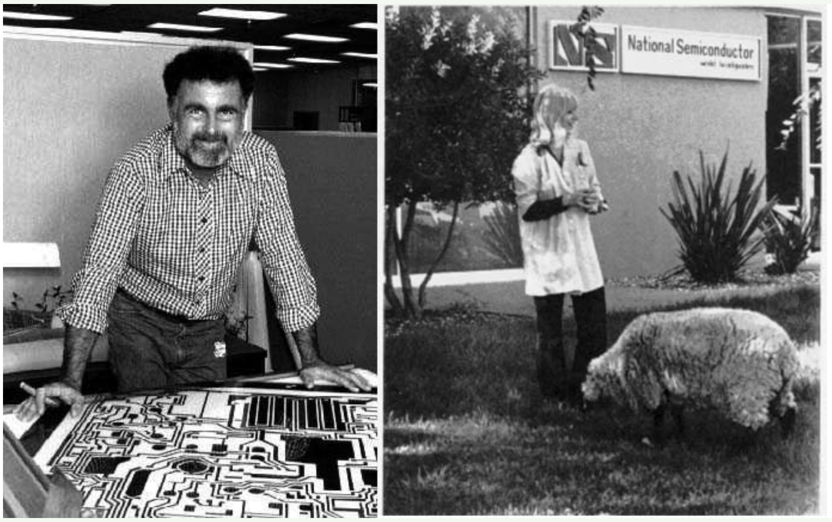


Figure 17: Bob Widlar (standing over a chip plot of the LM10); the infamous groundskeeping sheep (with a bemused National employee, Vickie Darst, looking on). Both photos courtesy of Bob Pease and the National Semiconductor Archives.

Only a few years after joining National, Widlar's stock options had appreciated sufficiently (thanks in large part to his designs) that he "retired" from National Semiconductor at about 10:30 PST, 21 December 1970. Not long after, he drove his Mercedes down to Puerto Vallarta, Mexico, where he lived the rest of his life. He had celebrated his 33rd birthday just the month before.

After a brief period of time in which he worked with a fledgling Linear Technology (co-founded by Bob Dobkin of the sheep adventure), he returned to designing for National Semiconductor on a contract basis. During this time he designed an op-amp (the LM10) that delivered 741-like specifications while operating off of a single 1.2V supply. If that weren't impressive enough, he included a bandgap voltage reference (the reader will note that the nominal supply voltage does not exceed a bandgap voltage). He followed that achievement with the LM11, a bipolar op-amp with 25pA input bias current. His next design represented a leap from one power extreme to the other: The LM12 is an operational amplifier capable of 10-ampere output currents and 80W continuous dissipation (800W peak). Its integral protection is so comprehensive that considerable effort is required to destroy it.

After a life of extreme habits, he eventually adopted a healthier lifestyle, and began jogging regularly. On one of these jogs in early 1991, he suffered a fatal heart attack near his home in Puerto Vallarta. He was only 53 years old.

Acknowledgments

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A History of the Continuously Innovative Analog Integrated Circuit

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The analog circuit has to perform signal processing on time varying signals with a continuum of levels in either voltage, current or charge. In contrast the digital circuit only has to resolve one of two signal levels that represent a 0 or 1. While an analog signal has a theoretically infinite resolution, the signal degradation caused by noise (random variations) and non-linearity (distortion) that are present in the analog circuit are inherent design considerations that must be managed by the circuit designer.

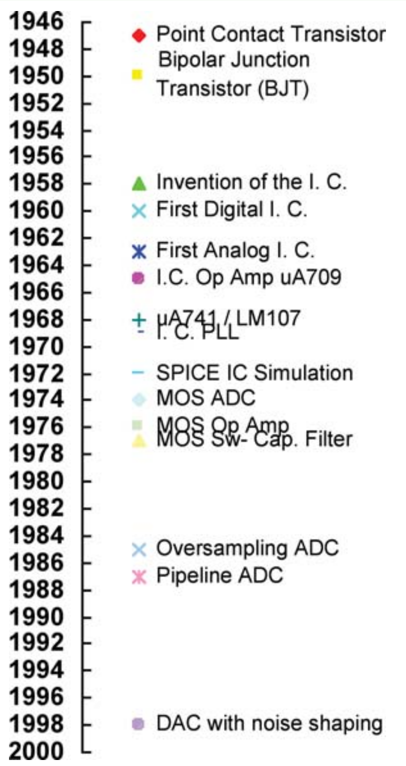
The analog integrated circuit is different from the discrete analog circuit in that it is fully integrated onto a single monolithic piece of silicon; where the selection of individual elements is not possible. The analog integrated circuit designer has to work within the constraints of circuit elements, their range of values and their tolerances that the process technology allows. This article will trace some of the key innovations that became the major turning points in what has been an innovative history for analog integrated circuit design.

The following is a list of analog circuits and their building blocks that have become the standard techniques for analog IC design. They range from the basic sub-circuits, to the building blocks, and the more complex functional blocks.

a) Basic Analog Sub-Circuits: Current Mirror, Trans-conductor, Amplifier, Linear Multiplier, Level Shifter, Limiting Amplifier, Comparator, Current driver, voltage mode driver.
b) Circuit Building Blocks: Operational Amplifier, Wideband Amplifier, High speed/High sensitivity input buffer, Low Noise Amplifier, RF Tuned amplifier, RF Mixers, Temperature Sensor, Precision Voltage Reference (the band-gap), Voltage Regulator.
c) Analog Functional Circuit Blocks: Digital-to-Analog Converter, Analog-to-Digital Converter, Frequency Filters, Oscillators, Phase Locked Loop, Delay Locked Loop.

This article will cover the history of the invention and development of the monolithic integration of these circuits, creating the field of the solid-state analog integrated circuits.

While the invention of the first transistor, the point contact transistor, at Bells Labs in late 1947 was demonstrated with the transistor in an amplifier circuit for an audio microphone and then an oscillator to show power gain [3], analog circuit design using discrete solid-state semiconductor transistors began in all practicality after the invention of the bipolar junction transistor (BJT) [1], [2] in 1950 when transistor fabrication in volume became a reality [3], [4]. Analog circuit design using BJTs was enabled through the contributions of pioneers J. M. Early, J. J. Ebers and J. L. Moll. J. M. Early developed the basic understanding of the operation of the BJT which was needed for circuits [5] (and his name is used today whenever we describe the output resistance of Bipolar transistors – the Early Voltage). Also J. J. Ebers and J. L. Moll [6] created the large-signal model to describe the DC and large signal transient behavior of the BJT (Ebers-Moll model). All three pioneers were at Bell Telephone Labs.



History of Analog Integrated Circuit Innovation

i) The beginning of the Monolithic Analog Integrated Circuit

As the BJT operation and its analytical models continued to be understood better, the first solid-state transistor amplifier and oscillator circuits were explored and demonstrated [7].

The monolithic analog integrated circuit design did not get to make significant progress until after the first digital integrated circuits were fabricated monolithically in Fairchild Semiconductor's BJT planar process [8, 9, 10] that had aluminum metal interconnect and diffused resistors. This process enabled designers to design monolithic analog integrated circuits that achieved higher frequency operation and lower power than discrete circuits. Three years later in 1963 the first monolithic analog integrated circuits were introduced commercially; the five-transistor 100MHz µA703 RF-IF amplifier (1963) [11] characterized specifically for RF operation. This was followed by the first operational amplifier µA702 (1964) and the highly successful µA709 (1965) nine-transistor operational amplifier, all from Fairchild Semiconductor [11]. Also around this time there were a number of BJT and JFET analog integrated circuits proposed but it was the planar bipolar process that became the mainstream analog integrated circuit process.

While the process technology that combined bipolar junction transistors with junction field effect transistors (JFET) took many years to become practical, the bipolar transistor process with a vertical npn and lateral pnp provided the transistor performance and process simplicity so that high perform-

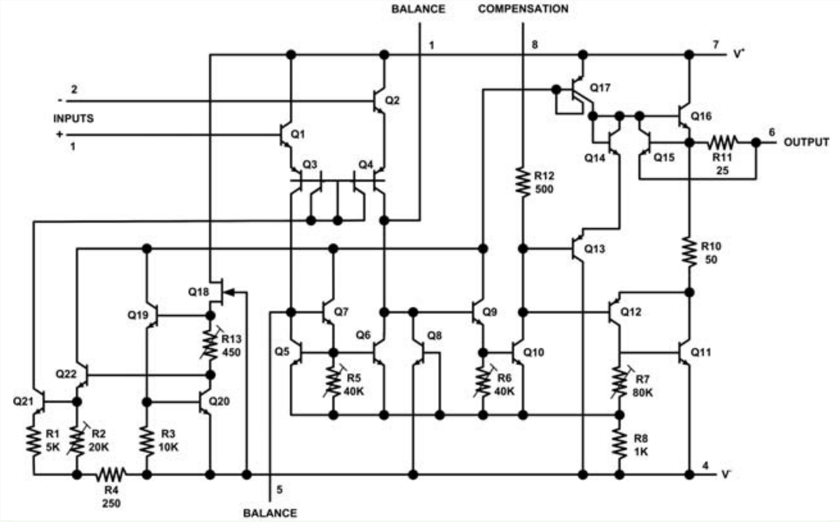


Figure 1: Schematic of LM101.

ance, high volume analog circuits were able to be designed and manufactured. This was only possible through the innovative circuit design techniques of analog circuit pioneers such as Robert Widlar [12, 13] (working at Fairchild Semiconductor and then later National Semiconductor), Barrie Gilbert (working at Tektronix) [14], George Wilson (working at Tektronix) [15]. These circuit designers, along with others working in these companies during this period, created the new field of solid-state analog circuit design - the monolithic solid-state analog integrated circuit. They had to design the circuit under the constraint of using strictly transistors and passive elements with parameters that were available in the integrated circuit process – npn transistor, pnp transistor, (and their pn diodes), diffused resistors and capacitors. The designer did not have the option to "cherry-pick" select from a catalog the current gain, the f_t, the early voltage (R_{out}), and emitter or collector current drivability for each transistor in the circuit. However designers found unique attributes that the monolithic integrated circuit provided; for example all the bipolar junction transistors on the die had the same Early Voltage, the V_{be} between two identically layed out transistors were closely matched versus collector current characteristic, lateral pnp devices had poor AC performance but they could be used for current sources and active loads. (If pnp devices were in the signal path, they were limited in use to configurations that provided the fastest operation such as the common base configuration.)

Barrie Gilbert pioneered understanding of wideband amplification with BJTs and linearized trans-conductance operation of the bipolar transistor. He developed the BJT linear multiplier [14] (referred to as the Gilbert multiplier). Today this technique is still used in the design of high speed phase detectors, variable gain controlled amplifiers, RF mixers and modulators and precise linear multipliers (and the circuit topology has been even applied in MOS ICs).

Figure 2: Robert Widlar

Robert Widlar pioneered the monolithic integrated operational amplifier (1964: µA702, 1965: µA709, 1967: LM101 - much like the µA709, but with output short circuit protection and simplified frequency compensation. The µA741 was introduced by Fairchild in 1968, one year after Widlar resigned from Fairchild and joined National Semiconductor. The µA741 was similar to a LM101 except that it had a fully integrated compensation capacitor. Widlar also pioneered the monolithic band-gap reference [13], and the three pole voltage regulator. His name is remembered whenever a designer uses the commonly used high impedance current mirror called the Widlar current mirror [16]. Widlar had the insight in developing techniques that exploit the best attributes of the devices available in a bipolar integrated circuit process. He went as far as developing a circuit configuration that allowed the use of the low BV_{ceo} super gain (β) transistor in the input stage of operational amplifiers [12].

George Wilson pioneered current sources and operational amplifier design, and he developed circuits that exploited the benefits of both BJT and JFET transistors [15] when monolithically integrated together.

In 1969, A. Grebene and H. Camenzing of Signetics developed the first integrated monolithic Phase Locked Loop in bipolar process technology with a high level of integration [17]. It combined a phase detector, loop filter with an amplifier/buffer, and oscillator (loop filter and oscillator required external capacitors), bringing dramatic reduction in cost and availability to this highly versatile function. It was first used predominantly for FM demodulators, however it has since become pervasive in communications as well as in digital systems for timing.

ii) The "Field" becomes Established

Meanwhile with the increasing degree of transistor integration and the desire to design monolithic circuits at higher frequencies, more sophisticated transistor models and the means of managing the complex circuit analysis were needed by the designer. The ability to design these integrated circuits was becoming extremely complex and it became difficult to predict their performance parameters at that point. To solve this problem, in the late 1960s and early 1970s

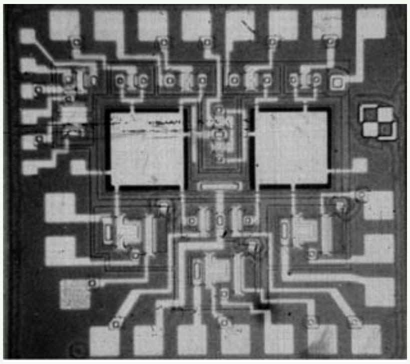


Figure 3: All-NMOS DAC for the Charge redistribution ADC

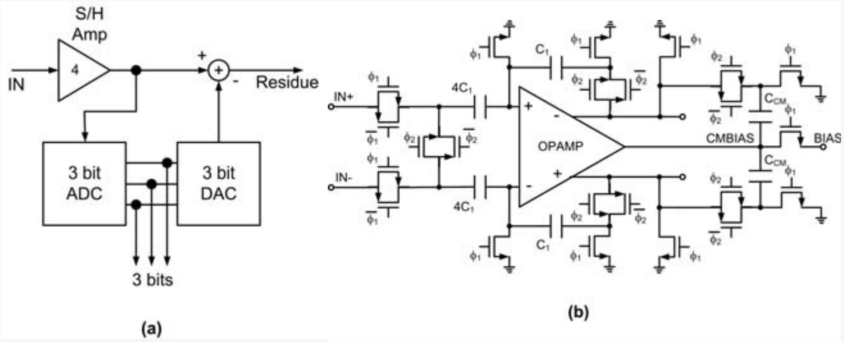


Figure 6: 5MHz 9b Pipeline ADC Circuits Diagram

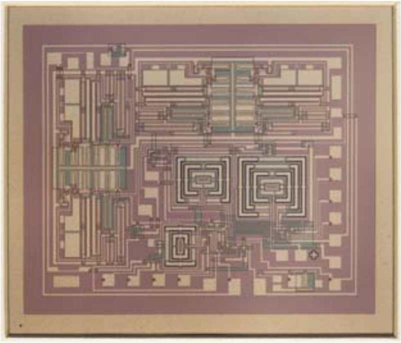


Figure 4: Fully integrated second order analog sampled data recursive filter – a four opamp switched-capacitor biquadratic filter. NMOS A1-gate process.

the Simulation Program with Integrated Circuit Emphasis (SPICE) was developed by the circuit researchers at UC Berkeley under the direction of Professor Don Pederson [18]. In 1972 the program was released into the public domain. SPICE became the standard simulator for IC design immediately and a whole CAD industry of circuit simulators grew out of it. Other universities and companies adopted this program making integrated circuit research and development more predictable and enhancing the understanding of the field.

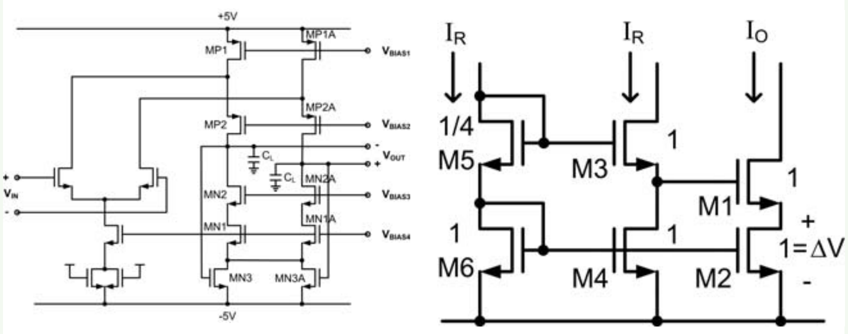


Figure 5: Fully Differential Folded Cascode OTA and wide swing cascode bias generation circuit.

With increasing performance and availability of digital circuitry for computation and signal processing there was a growing need for low cost Analog to Digital and Digital to Analog conversion circuits. The 1967 ISSCC paper by M. B. Rudin, R. O'Day, and R. Jenkins [19] describes the system level design of these circuits with IC building blocks and their level of integration. In 1970 Pastoriza, Krabbe, and Molinari of Analog Devices Inc., developed the first monolithic Digital to Analog Converter (DAC) that was designed using the replica biasing and constant-current-density operation of binary-weighted PNP bipolar transistor emitters for switched current sources [20]. This technique became the basis of the majority of future bipolar DACs and successive approximation (SAR) Analog to Digital Converters (ADC).

In the late 1960s and early 1970s integrated circuit process technology development moved its focus from BJT to MOSFET technology (with only four masks) in order to realize the potential of larger scale solid-state integrated memory and custom digital logic circuits. Analog circuit design knowledge was needed for these MOS integrated circuit memory chips to design the sensing, amplification and off-chip driver circuits that were required to achieve high speed access and large bit density. However MOS transistors had poor matching of their threshold voltage compared to bipolar transistors. In 1973, Poujois, Baylac, Barbier and Ittel from LETI in France used MOSFET linear transistors and switches to design a sample and hold low input offset voltage two-stage amplifier in an all-MOS process technology [21].

iii) The beginning of Analog MOS Integrated Circuits

In the mid 1970s the possibility of analog circuits being implemented with MOS technology became a reality. The idea that they could achieve lower cost and be integrated together with logic functions, started a major period of innovation for analog circuit design with MOS technology. At U. C. Berkeley the integrated circuits research group with Professors David Hodges, Paul Gray, Robert Meyer and Robert Broderson did pioneering work with their students and brought on the analog MOS integrated circuit era [22, 23, 24, 25, 26, 27, 28]. Their contribution enabled the large scale integration of analog circuits together with digital signal processing, logic and memory. The professors of the UC Berkeley IC group directed research that evolved into a number of analog integrated circuit and architecture accomplishments.

In 1974, Ph. D research student Ricardo Suarez-Gartner with Professors Paul Gray and David Hodges demonstrated a Successive Approximation Register (SAR) ADC

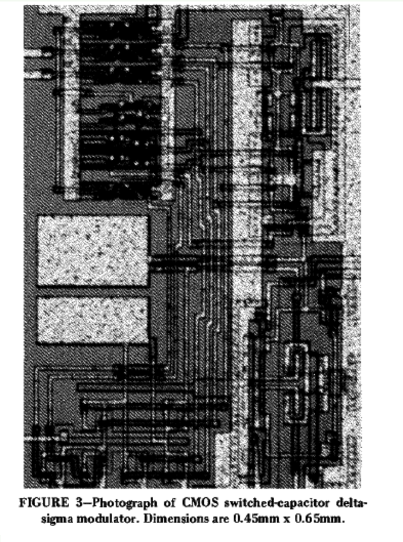


Figure 7: Photograph of the CMOS switched-capacitor Delta-Sigma modulator for oversampled ADC, 0.45mm x 0.65mm.

based on an All-MOS DAC using charge redistribution from a binary array of MOS capacitors and associated MOS switches [22]. This was because MOS technology had accurate well-matched capacitors (matched better than transistors) and good analog switches.

One of the earliest monolithic single chip ADCs was demonstrated with CMOS in 1976 using the dual slope auto zeroing architecture and a fully integrated CMOS opamp [23]. This ADC achieved 11bit accuracy. In the same year R. J. van de Plassche introduced the idea of dynamic element matching in DACs to achieve resolution beyond the intrinsic matching capability of the current sources without the use of trimming.

In 1976 Yannis Tsividis with Professor Paul Gray demonstrated an All-MOS internally compensated NMOS Operational Amplifier [25] that was insensitive to process variations, i.e. with current bias and transistor parameter tracking. In 1977 Ian Young (myself when a Ph.D student) with Professors David Hodges and Paul Gray demonstrated an All-MOS sampled-data second-order active filter using a precise clock reference [26], four operational amplifiers, analog switches and ratioed capacitors all fabricated on an NMOS integrated circuit. This analog sampled-data circuit technique was used to implement other filter topologies that were less sensitive to filter parameters, e.g. the L-C ladder filter. It became known as the switched-capacitor filter. Due to its discrete time sampled-data signal processing, the analog switched-capacitor filter's bandwidth and ripple only depended on the ratio of capacitors and the external reference clock frequency.

With the opportunity of applying switched-capacitor filters to the higher frequency communications applications, a high frequency opamp was needed to enable the sampling frequency to be increased. In 1984 Tat Choi, Ron Kaneshiro, and Professors Robert Broderson, and Paul Gray developed a wide bandwidth, high gain fully differential cascoded transconductance amplifier topology called the folded cascode amplifier [27]. Subsequently as MOS transistor scaling continued and supply voltages were reduced, this circuit became attractive for use at low supply voltages.

In 1985, A. G. F Dingwall and V. Zazzu demonstrated the first high speed, high resolution ADC (8MHz, 8b) that used sub-ranging to reduce capacitive loading and the number of comparators 8 fold over a full Flash ADC [28].

Research student Harry Lee and Professors David Hodges, and Paul Gray used a digitally controlled self-calibration architecture to realize a 12b, 12µs CMOS ADC [29] in 1984. The era of mixing digital circuits to improve analog IC performance was beginning.

iv) The emergence of the Mixed-Signal Analog ICs

With the increasing level of integration on IC chips, analog circuit researchers found ways of using more digital circuit techniques to improve the ADC accuracy. Oversampling Δ–Σ ADCs were first demonstrated in 1985 by U.C. Berkeley research students Mark Hauser, Paul Hurst, and Professor Robert Broderson [30]. This architecture applied signal processing noise shaping to an ADC that had just 1-bit conversion accuracy but sampled the input signal at rates 256 times higher than the normal 2X the bandwidth of the input signal, with negative feedback of high frequency quantization to exchange resolution accuracy in time for that in amplitude. This architecture provided a means of exploiting the continuously enhanced density and performance that digital MOS technology was providing with scaling, to ease the difficulty of implementing complex analog circuits within the scaled MOS technology.

Meanwhile researchers continued to pioneer ways of making high speed, high bandwidth ADCs, which were now called Nyquist ADCs because they had an input signal bandwidth up to their Nyquist sampling rate. In comparison the recently developed oversampled ADCs were only useful in low bandwidth applications due to their use of noise shaping through clock oversampling and filtering. Research student Stephen Lewis together with Paul Gray looked to MOS switched-capacitor circuit elements - operational amplifier, analog switches, ratioed MOS capacitors and a reference clock - to implement a low bit resolution ADC plus DAC with one multiply and subtract operation. In 1985 they were able to realize the high sampling rate Nyquist Pipeline ADC [31]. The pipeline term arises from the fact that there was a pipeline of 'n' bit resolution ADC stages. A digital circuit was designed to perform a conversion algorithm on the output bits from each stage into the overall high resolution output from the ADC.

In 1998 researchers R. Adams, K. Q. Nguyen, and K. Sweetland [32] at Analog Devices applied oversampled signal processing to DACs to enable higher resolution than the DAC elements alone provided. This was done by oversampling and shifting element-mismatch errors into the high frequency spectrum where it was easily filtered out.

v) Ubiquitous Analog + Digital For Communications – The Recent Years

As mentioned at the beginning of this article during the early years of the bipolar integrated circuit, RF circuits took advantage of monolithic integration. The field of narrowband RF integrated circuit development continued to progress after those early years. The benefits of lithography scaling and bipolar transistor device design were applied to f_t and f_{max} improvement and more transistor integration, enabling higher performance and lower cost communications and consumer electronics products. In the last fifteen years the field of RF integrated circuits – BiCMOS and, very recently, CMOS – has rapidly emerged, realizing optical network transceivers, and low cost wireless radio RF transceivers for Cellular and 802.11 wireless LAN applications.

With the introduction of SiGe heterojunction bipolar transistor (HBT) process technology, the f_t and f_{max} of the bipolar transistors were able to move to much higher frequencies (it had been held back for some years by the practical minimum on transistor base width). Thus bipolar circuits had a resurgence as they were able to move into much higher frequency applications such as 10Gb/s and 40Gb/s optical networks and the fully integrated cellular RF transceiver with low noise amplifiers, mixers and power amplifiers.

As has been the case for the digital IC technology, analog integrated circuits have enjoyed dramatic improvements in performance and functionality per unit cost for over four decades. This was a result not just of improvements and innovations in the process technology and its devices, but also as this article has tried to chronicle, was due to the contributions of many analog IC pioneers who innovated at the device, circuit, and system levels. Their combined contributions made possible the wide ranging applications of silicon integrated electronic devices in audio, wireless radio, video, digital micro-controllers, telecommunications, data communications and modems, 1/10/100/1000 M-bit Ethernet, disk drives, cell-phones, 802.11 wireless data networks, and multi-media entertainment.

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Acknowledgements: Paul Brokaw, and David Robertson for their work in writing the ISSCC 2003 Digest of Technical Papers, 40th and 50th ISSCC anniversary supplement articles respectively on the ISSCC history of the analog integrated circuit, from which I have referenced most of the key milestones.

About the Author

Ian Young is Senior Fellow and Director in Intel Corporation. He is responsible for directing Advanced Circuits and Technology Integration, including defining and developing future circuit directions and optimizing the manufacturing process technology for microprocessor and communications products.

Young joined Intel in 1983. Starting with the development of circuits for a 1Megabit DRAM, he led the design of three generations of SRAM products and manufacturing test vehicles, and developed the original Phase Locked Loop (PLL) based clocking circuit in a microprocessor while working on the 50MHz Intel486™ processor design. He subsequently developed the core PLL clocking circuit building blocks used in each generation of Intel microprocessors through the 0.13um 3.2 GHz Pentium 4. His work on six generations of PLL designs has been recognized as a contributing factor in improving microprocessor speed. Young has developed a number of optimization metrics for process technology development, including the transistor performance metric that provided a link between processor performance and basic transistor parameters, as well as back-end metal interconnect architecture. From 2001-2004 he worked on the circuit design and process development of 10Gb/s SONET Serdes transceiver circuits and wireless LAN RF front-end Radio transceiver circuits in a 90nm RF CMOS communications process. He is currently directing the development of high speed serial IO circuit technology in the 32nm logic technology and researching optical interconnects for the future products.

Born in Melbourne, Australia, Dr. Young received his bachelor's and master's degrees in Electrical Engineering from the University of Melbourne, Australia, in 1972 and 1975. He received his Ph.D. in Electrical Engineering from the University of California, Berkeley in 1978. Prior to Intel, Young worked on analog/digital integrated circuits for Telecommunications products at Mostek Corporation (United Technologies), and was an independent design consultant.

Young was a member of the Symposium on VLSI Circuits Technical Program Committee from 1991 to 1996, serving as the Program Committee Co-Chair/Chairman in 1995 and 1996, and the Symposium Co-Chair/Chairman in 1997/1998. He was a member of the International Solid-State Circuits Conference Technical Program Committee from 1992 to 2005, serving as the Digital subcommittee Chairman from 1997 through 2003, Technical Program Committee Vice-chair in 2004 and the Chair in 2005. He was Guest Editor for the April 1997, April 1996 and December 1994 issues of the IEEE Journal of Solid-State Circuits. He has been on the IEEE Solid-State Circuits Society AdCom since 2006.

Young is a Fellow of the IEEE. He holds 43 patents in integrated circuits and has authored or coauthored over 40 technical papers.

Abidi to Receive IEEE Donald O. Pederson Award at ISSCC 2008

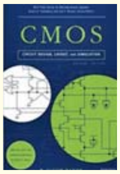
Katherine Olstein, SSCS Administrator, k.olstein@sscs.org

Professor Asad Abidi of UCLA has been selected as the recipient of the 2008 IEEE Donald O. Pederson Award in Solid-State Circuits. He will be honored for his "pioneering and sustained contributions in the development of RF-CMOS" at the next meeting of the ISSCC in February, 2008. Prof. Abidi was elected to the National Academy of Engineering (NAE) this spring. A full story about him will appear in the SSCS News of winter 2008.

Established in 1987, the IEEE Solid-State Circuits Technical Field Award was renamed in 2005 in memory of Donald O. Pederson of UC Berkeley. Pederson was a co-founder of the Solid-State Circuits Council, the predecessor of the current Society, and was involved in the early years of the International Solid-State Circuits Conference and the Journal of Solid-State Circuits (www.ieee.org/portal/pages/sscs/06Jan/Pederson-MDL.html).

Previous recipients of the Donald O. Pederson Award include Prof. Mark Horowitz of Stanford, in 2006 (www.ieee.org/portal/pages/sscs/05Nov/Horowitz.html) and Prof. Hugo De Man, Professor Emeritus at the Katholieke Universiteit, Leuven, Belgium, in 2007 (www.ieee.org/portal/pages/sscs/07Winter/DeMan.html). A full list of previous recipients may be found at http://sscs.org/awards/Fieldawards.htm.

R. Jakob Baker Receives Frederick Emmons Terman Award



Katherine Olstein, SSCS Administrator, k.olstein@sscs.org

The American Society for Engineering Education (ASEE) has selected R. Jakob Baker to receive the prestigious Frederick Emmons Terman Award for his book "CMOS: Circuit Design, Layout, and Simulation," Second Edition. This volume in the Wiley-IEEE Press Series on Microelectronic Systems has been a best seller at ISSCC for the past three years (www.ieee.org/portal/pages/sscs/07Spring/Books.html).

The Terman Award recognizes excellence in electrical and computer engineering textbooks by authors under the age of 40. Dr. Baker was formally honored at the ASEE Frontiers in Education Meeting co-sponsored by ASEE and the IEEE Computer and Education Societies this October in Milwaukee, WI (fie.engrng.pitt.edu/fie2007/). A fully story about him will appear in the SSCS News of winter 2008.

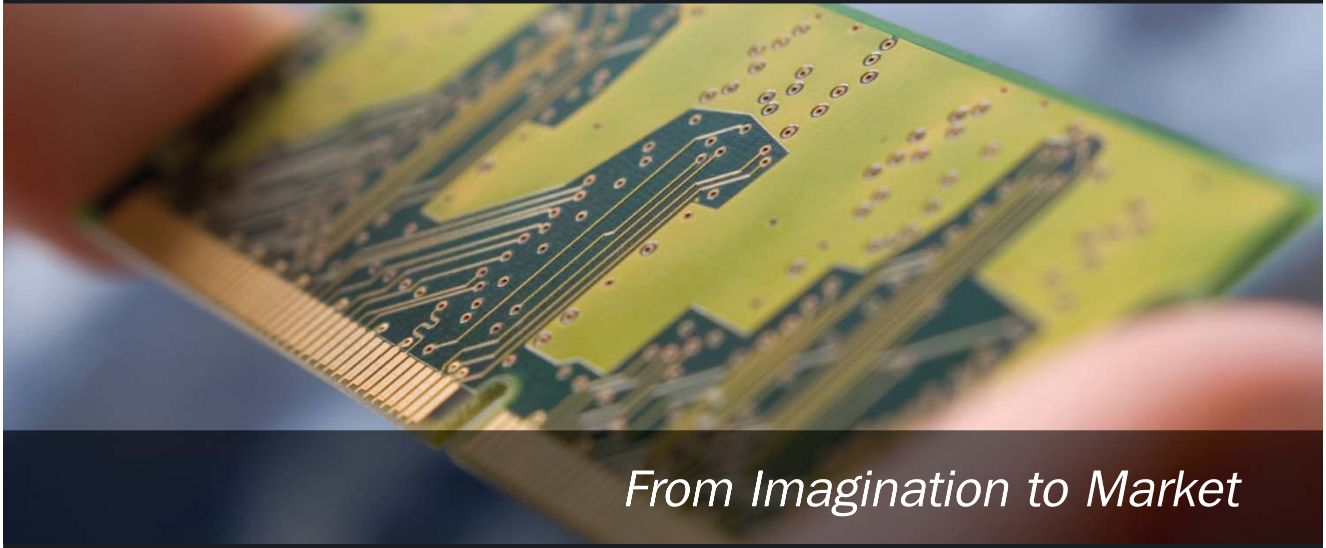
J. Kim and S. Shekhar Granted SSCS Predoctoral Fellowships for 2007-2008

Jintae Kim of UCLA and Sudip Shekhar of the University of Washington, Seattle have won Solid-State Circuits Society Predoctoral Fellowships for 2007 - 2008. The Society's predoctoral fellows are selected each year for "their considerable accomplishments to date and their great promise for future contributions to the field of solid- state circuits," said Prof. David Hodges of UC Berkeley, Chair of the Awards Committee.

The predoctoral fellowship provides a student stipend of $15,000, tuition and fees up to $8,000, and a grant of $2,000 to the department in which the recipient is registered. Applicants are required to have completed one year of graduate study, be in a Ph.D. program in the area of solid-state circuits, and belong to IEEE.

Jintae Kim (S'03) received the B.S. degree in electrical engineering from Seoul National University, Seoul, Korea in 1997. From 1997 to 2001, he was a design engineer at Xeline, Korea, where he worked on the design and implementation of digital baseband IC for power-line communication. While working at Xeline, he acquired two U.S. patents for new algorithms to adaptively find optimal data rate when multi-users are competing in the shared channel.

Since the fall of 2001, he has been a student in the department of electrical engineering, UCLA under the supervision of Prof. Chih-Kong Ken Yang. From the fall of 2001 to the spring of 2003, he was a teaching assistant in the department of electrical engineering for various undergraduate circuit courses such as analog electronic circuit (EE115A) and circuit analysis (EE10, EE110). In the summers of 2003 and 2004, he worked at Barcelona Design, Inc. as a summer intern.


From Imagination to Market

During this period, he made contributions on Barcelona's equation-based optimization engine for analog and digital circuit optimizations. This work, which was a primary part of his master's research, resulted in a presentation at the International Conference on Computer Aided Design (ICCAD), 2004. The paper focused on demonstrating an improved device modeling methodology for the equation-based circuit optimization.

Since March 2004, Mr. Kim has been working towards his Ph.D. degree at UCLA. Early in the Ph.D. program, he designed an innovative serial link transmitter circuit that combines a conventional transmitter with an integrated transformer booster. This circuit enables a true pre-emphasis equalization in the serial link transmitter. The idea was presented at the International Solid State Circuit Conference of 2006 and subsequently appeared in the JSSC of May, 2007.

Mr. Kim's current research interest is the design and optimization of CMOS mixed-signal circuits considering the multi-dimensional design tradeoff from device, circuit, and architecture perspectives. Preliminary results of this work will be presented at the International Conference on Computer Aided Design (ICCAD), 2007.

Mr. Kim received a Ministry of Information and Communication Fellowship in Korea in 2001 and a UCLA electrical engineering department fellowship for academic excellence in 2006.

Sudip Shekhar (S'00) received the B. Tech. degree with honors in electronics and communications engineering from the Indian Institute of Technology, Kharagpur in 2003. He received the M.S. degree in electrical engineering from the University of Washington, Seattle in 2005. His M.S. dissertation focused on bandwidth extension techniques for high-speed CMOS buffers and UWB low noise amplifiers. He is currently working toward the Ph.D. degree at the University of Washington on wideband phase locked-loops for polar transmitters.

In the summer and fall of 2005, he was an intern with the Advanced Components Division, Intel Corporation in Hillsboro, OR, where he worked on the modeling and design of serial links. During the summers of 2006 and 2007, he was an intern with the Circuits Research Lab at Intel Corporation, working on injection locking techniques and fast locking delay locked-loops. His current research interests include RF transceivers, frequency synthesizers and mixed-signal circuits for high-speed I/O interfaces.

Mr. Shekhar is a recipient of the Intel Foundation Ph.D. Fellowship for 2006–2008 and the Analog Devices Outstanding Student Designer Award for 2007. He placed second in the Analog Devices Inc. Circuit Design Contest in 2004. He has published over 20 IEEE conference and journal papers and two invited book chapters, and has submitted a patent application during his graduate work.

IEEE "GOLD" Program Designed for Members in their First Decade as Professionals

Bruce Hecht, SSCS Membership Chair, bruce.hecht@analog.com

The GOLD program is IEEE's outreach to "Graduates of the Last Decade." These members are recent graduates who are experiencing the exciting first decade of their professional careers. As you can tell by the choice of the word "Gold," with its connotation of a precious and valuable material, the young professionals in this group are highly valued by our technical community. One reason is the essential fresh perspective, as the new graduates apply their skills and enthusiasm to the open topics of the day.

The IEEE and its societies have long enjoyed success with IEEE student branches and membership at universities. However, once these members graduate and enter their work lives, not all continue their membership with IEEE. There are many reasons why we would like to change this situation: Our societies and the IEEE as an organization benefit from the ideas and enthusiasm of this cohort. In turn, young professionals expand their network of peers and their access to experienced mentors.

First launched at the 1996 Sections Congress, there are now 120 GOLD groups throughout the IEEE's 10 Regions. The current retention rate has risen to 61% of student members staying on with IEEE after graduation. With your help we can continue to expand the effectiveness of our GOLD program.

New graduates will find GOLD programs tailored to their interests

Over the last ten years, the GOLD program has grown and developed a variety of services, ranging from exposure to new technologies through participation in IEEE chapter meetings, conferences, and events. In addition, many GOLD groups organize social and professional events around local activities and attractions.

As an example of program ideas, the Region 1 GOLD groups gathered during a weekend last April to share experiences and ideas for successful events. Included on their list were subjects such as Guest Speakers for Financial Planning, Investment, Leadership development, and Career Advancement; convening GOLD competitions; and joint meetings with other groups such as student chapters, Women-in-Engineering, and local industrial visitors.

WANTED: IEEE Leaders to share their knowledge and experience with GOLD members
As an experienced practitioner in the field, you have valuable stories and knowledge to share. Volunteer to give your perspective. There are many avenues available. You could present a technical talk at a chapter meeting, or suggest a tutorial to help GOLD members "learn the ropes." With IEEE's latest approach to mentoring, you could find your match in establishing a personal connection with an up-and-coming engineering protégé.

Chapters are encouraged to promote activities for GOLD members
In seeking to grow chapter membership and recruit future volunteer leaders, a great place to focus is on newly minted graduates who are GOLD members. You may want to consider the opportunity for your chapter to encourage your new members to become active participants. Ideas which have worked well include: inviting participation from student branches and student members prior to graduation; providing welcome letters and hosting a graduation reception at the end of the school year; publishing articles in the IEEE Potentials Magazine on topics in your field of interest.

Links to explore: IEEE and GOLD Products and Services for Young Members
Information on the GOLD program, and benefits for GOLD members, a listing of GOLD groups around the world, the GOLDRush Newsletter, and further links for GOLD Resources are easy to find:.

- IEEE GOLD benefits:
  www.ieee.org/membership/congrats
- IEEE GOLD Events: www.ieee.org/gold
- IEEE.tv (internet-based broadcasting network, delivering special-interest programming about technology and engineering) – www.ieee.org/ieeetv
- IEEE Job Site, Career & Employment Resources - www.ieee.org/web/careers/home/index.html
- IEEE Center for Education & Training. - www.ieee.org/web/education/home/index.html

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SSCS Staff: O'Neill and Olstein Achieve Professional Milestones

The two staff members of the IEEE Solid-State Circuits Society recently achieved professional milestones.

O'Neill Earns Certified Association Executive Credential

Anne O'Neill, SSCS Executive Director, has earned the Certified Association Executive (CAE ™) credential, the highest professional credential in the association industry. Less than five percent of all association professionals have earned the CAE. O'Neill was recognized at the annual meeting of the American Society of Association Executives, the certifying organization, on 13 August, 2007.

To be designated as a Certified Association Executive, an applicant must have a minimum of three years in nonprofit organization management, complete a minimum of 75 hours of specialized professional development, pass a stringent examination in association management, and pledge to uphold a code of ethics.

As Executive Director of SSCS, O'Neill is responsible for managing the Society office, communications, and budget under the direction of the SSCS Administrative Committee. She became the first SSCS Executive Director in 1998 when the Society was formed.

After receiving a BS in Engineering from The College of New Jersey in 1985, O'Neill began her engineering career as a production Engineer for Microwave Semiconductor Corporation - a Seimens USA company. In 1991 she joined IEEE, working as a Standards Engineer for the IEEE 802 computer communications standards until 1996, and as an International Standards Engineer for the Power Engineering Society from 1996 to 1998.

Olstein Receives NYU Certificate in Journalism

Katherine Olstein, SSCS Administrator, completed a certificate program in journalism this spring at New York University's School of Continuing and Professional Studies. The Certificate in Journalism is awarded to students who complete four required courses and one 10-session elective or two five-session electives from the Journalism curriculum. The four required courses are: News Reporting, Feature Writing, Interviewing, and Legal and Ethical Issues in Journalism. Writing for Magazines was her selected elective.

Olstein manages, copyedits, and writes for the SSCS News and is responsible for supporting SSCS Chapter, Distinguished Lecturer and Membership activities, and the Society's Predoctoral Fellowship Program. According to Newsletter Editor Mary Lanzerotti, "Kathy led the upgrade of the Newsletter on the IEEE side using the expertise that she gained in her journalism classes at NYU. We are delighted that she was awarded the certificate and will continue to ensure that the SSCS News satisfies the highest standards in journalism."

Katherine joined SSCS in 2005 after careers in higher education and information technology. She holds a Ph.D. in Greek and Latin from Columbia University and is a member of Phi Beta Kappa.

Congratulations New Senior Members

21 Elected in April, May and June

Pietro Andreani	Denmark Section
Hamid Tony Bahramian	Coastal Los Angeles Section
Christian Bjork	Sweden Section
Sheng-Fuh Chang	Tainan Section
Marco Corsi	Dallas Section
Vincenzo Ditommaso	Oregon Section
Wolfgang Eberle	Benelux Section
Dimitrios Efstathiou	Central North Carolina Section
Payam Heydari	Orange County Section
Per Larsson-Edefors	Sweden Section
Sven Mattisson	Sweden Section
Joe Mcalexander	Dallas Section
Saeid Nooshabadi	New South Wales Section
Muralikumar Padaparambil	Mid-Hudson Section
Rahul Sarpeshkar	Boston Section
Jafar Savoj	Santa Clara Valley Section
Kenneth Tsui	Oregon Section
Gilson Wirth	South Brazil Section
Gonggui Xu	Dallas Section
Ji-Woon Yang	Central Texas Section
Regan Zane	Denver Section

Many benefits accompany IEEE Senior Member status:

- Professional recognition for technical and professional excellence
- Fine wood and bronze engraved Senior Member plaque to proudly display
- Up to $25 gift certificate toward one new Society membership
- Letter of commendation to your employer, upon the request of the newly elected Senior Member
- Announcement of elevation in Section/Society and/or local newsletters, newspapers and notices
- Eligibility to hold executive IEEE volunteer positions
- Eligibility to be Reference for Senior Member applicants
- Invitation to be panelist for reviewing Senior Member applications

To qualify for Senior Member elevation, a candidate must be an engineer, scientist, educator, technical executive, or originator in IEEE-designated fields. The candidate must have been in professional practice for at least ten years, and have shown significant performance over a period of at least five of those years. Three references are required to accompany the application.

For more information, or to apply for Senior Membership, please see the IEEE Senior Member Program website: www.ieee.org/organizations/rab/md/smprogram.html.

TOOLS:
How to Write Readable Reports and Winning Proposals

Part 4: Internal Proposals That Move Decision Makers

Peter and Cheryl Reimold, www.allaboutcommunication.com

People with great ideas for their organizations are often shocked to find those ideas rejected by management. They come to see management as unimaginative, unresponsive, or blinkered, but the real problem may be their own inability to write a persuasive proposal. Here we show you how to avoid common traps and to construct an internal proposal that stirs up decision makers.

Some Myths and Truths About Internal Proposals

Take an honest look at your beliefs about internal proposals. Do they fit more with the following myths than with the truth?

Myth #1: It's easier to get money for technical projects from my own management than it is to sell an external customer on a project. In truth, most managers who control the money are looking for solutions to major headaches. Unless you show them a burning problem, they're not going to spend a penny. The only sense in which internal proposals may be easier than external ones is that their format is often less complex.

Myth #2: Internal management appreciates creative projects or approaches. Researchers, project engineers, and technical professionals in general like to experiment with new ideas and therefore present the creativity of a project as a selling point. However, people who control the money (and are held accountable for it) usually prefer certainty: "If I spend $x, I'll get $y back within z months."

Myth #3: If I point out a problem the organization is facing, management will be eager to get it solved. In truth, decision makers are conservative; they will cling to the status quo as long as it seems safe and profitable. If you point out a problem, they may deny it, blame you or somebody else, or wait for it to go away— anything but fund your idea. The key is to show, in logical, financial terms, that the status quo is not safe and profitable.

Myth #4: If I show that a pressing problem exists and offer a cost effective solution, management will act. Chances are, management will still not move. Why? Because there are better investments for the company's limited money. It's just like the stock market: Many stocks may promise to satisfy your need to grow your savings, but you'll probably pick those that offer the biggest (though still safe) return in the shortest time. To persuade management to invest in your solution, you must present an attractive breakeven point after which your solution will save or make money.

An Effective Approach to Internal Proposals

The following five-step approach can give your proposals a good chance, because it is built on the truth about management's attitudes.

1. Define the problem to be solved.

What exactly is it? How much is it costing us? (Advice: Go for big problems that are causing a lot of pain; solving those will build your credibility and reputation.) When and where does it occur? (Advice: Think big. Does the same, or a similar, problem occur in several areas of the organization beside the one you initially considered?) Why is it occurring? If we don't solve the problem, how much will it cost us over the next year or several years?

2. Present an effective solution.

Briefly describe several possible solutions. (Advice: State the pros and cons of each objectively. This demonstrates that you have thought about the problem and are not offering your first half-baked idea.) Then recommend one idea as the preferred course of action. Finally, explain your plan of action by describing (1) the specific steps to be taken, (2) who will be involved, (3) what resources will be needed (both human and technical), and (4) when the plan will be implemented (include a time line or Gantt chart if the project is long or complex).

3. Present cost information.

This should include detailed budgets for the specific steps to be taken, people involved (internal/external consultants, support personnel, etc.), and technology required (equipment and services).

4. Project financial results.

Contrast the cost of solving the problem with the cost of not solving the problem. When will the organization begin to profit from this proposal? (Advice: Resist the temptation to inflate your projections. It is better to be seen as conservative than as overly optimistic.)

5. Ask for the order.

Close by asking for permission to start the project. (Advice: Use this as an opportunity to repeat the main benefits of implementing your solution.)

Cheryl and Peter Reimold have been teaching communication skills to engineers, scientists, and business people for 20 years. Their firm, PERC Communications (+1 914 725 1024, perccom@aol.com), offers businesses consulting and writing services, as well as customized in-house courses on writing, presentation skills, and on-the-job communication skills. Visit their Web site at http://www.allaboutcommunication.com.

The Blossoming of IC Design and Business in Asia

3rd Asian Solid-State Circuits Conference, 12-14 November, 2007, Jeju, Korea

Nicky Lu, A-SSCC 2007 Technical Program Committee Chair, pr@etron.com

The third Asian Solid-State Circuits Conference will be held from 12-14 November in Jeju, Korea at the Ramada Plaza Hotel on the island's beautiful seashore. The conference is fully sponsored by the IEEE Solid-State Circuits Society.

The A-SSCC is held every year in a rapidly growing region, such as in Korea (2007), China (2006), and Taiwan (2005). The conference provides unique opportunities for IC design experts and technology and business leaders to get together in Asia and to exchange ideas and information.

The theme of this year's conference is "The Blossoming of IC Design and Business in Asia."

From 1996 to 2006, Asia's IC sales increased by 10% in compound annual growth rate (CAGR); the CAGR of Asia's production value was 6% during that time. In 2006, IC sales in Asia reached about US $135 billion -- approximately 65% of the worldwide IC market. The production value of the worldwide IC industry in 2006 was about US $216 billion, with US $88 billion, or 41%, created by Asia. Since this high growth rate in the IC business in Asia is expected to continue in 2007, research and development in IC circuit design has been blossoming, as evidenced by the increasing number of papers submitted from Asia to the A-SSCC.

Submissions Represent 21 Countries

A-SSCC 2007 received 345 paper submissions, of which 111 will be selected for presentation. Therefore, the paper quality is exceptional and the presentations are expected to be very stimulating. The paper submission distribution is as follows: Korea 108, Taiwan 60, China 53, Japan 38, US 23, Iran 19, Hong Kong 9, India 7, Belgium 5, Canada 4, Malaysia 3, France 3, Germany 3, Austria 2, Spain 2, Australia 1, Bangladesh 1, Egypt 1, Singapore 1, Thailand 1, and Tunisia 1. The

CONFERENCES

TPC consists of a balanced mix of experts from both industry and academia. Thus, the technical program will cover the interests of all attendees from most of all IC product segments.

There will be four plenary talks presented by distinguished leaders in the IC industry.

Dr. Heegook Lee

Dr. Satoru Ito

Dr. Jackson Hu

Prof. Willy Sansen

The first speaker, Dr. Heegook Lee, President and CTO of LG Electronics Inc. (Korea), will give a speech entitled "The Strategic Considerations for Digital-TV System-on-Chip Products."

The second speaker, Dr. Satoru Ito, Chairman of Renesas Technology (Japan), will talk on "Convergence and Divergence in Parallel for the Ubiquitous Era."

The third speaker, Dr. Jackson Hu, Chairman and CEO of UMC (Taiwan), will speak on "Recent Business Models and Technology Trends and Their Impact on the Semiconductor Industry."

The last speaker, Prof. Willy Sansen of K.U. Leuven (Belgium), will give a talk entitled "Analog Design Challenges in Nanometer CMOS Technologies."

Four Tutorials and Two Panels

Tutorials on 12 November will cover advanced data converter design, silicon mm-wave IC design, advanced leakage reduction techniques, and low energy CMOS systems for body sensor network and ubiquitous healthcare. Also, two panel discussions on SoC or SiP and display driver ICs are planned for 13 November.

Popular Industry Program

In addition, the A-SSCC will hold a very unique and popular event called the "Industry Program," in which speakers will present cutting-edge product chips not only in a detailed chip or circuit description, but also through demonstrations and evaluation results to show how customers have improved their performance by using the chips.

On 12 November, Professor Hoi-Jun Yoo will host the Student Design Contest Program, where the best student papers will be demonstrated.

Some of the technical papers selected from the A-SSCC will be printed in a special edition of JSSC after being reviewed, and the best three Student Design Contest papers will be presented at the ISSCC 2008.

For more detailed information, please visit the following Web site: www.a-sscc.org

I look forward to seeing you in November on the picturesque island of Jeju, and hope that you will enjoy an excellent meeting and warm hospitality at the conference.

CHAPTERS

New SSC Chapter Formed in Western Australia

Associate Professor Adam Osseiran, Edith Cowan University, Perth, Australia,
a.osseiran@ecu.edu.au

Engineering and R&D Activity Boom in the Region

When I came to Western Australia from Europe five years ago, I saw that the region was poised for a promising future with numerous innovation possibilities.

- Western Australia is a young and vibrant part of the world; although it is more renowned for its flourishing resource industries, there are many activities and much potential in engineering research and development.
- Western Australia has four universities with a strong emphasis on engineering (Curtin University of Technology (CUT), Edith Cowan University (ECU), Murdoch University (MU) and the University of Western Australia (UWA)). Each has its strength in engineering topics, and inter-collaboration between researchers from different universities and with engineers from industry is common.

These resources and activities are attracting thousands of new residents to the region each month. This rush in return necessitates strengthening the existing basis of technology development to sustain its booming resource-based economy.

Therefore, it made sense to set up a Solid-State Circuits Society Chapter to gather members from the region and federate them around shared technical interests while promoting IEEE and SSCS, too.

How the Western Australia Chapter was Formed

I invited the IEEE Distinguished Lecturer Professor, Vojin Oklobdzija from UC Davis to give a series of talks in Perth in November 2006 (see SSCS News, winter 2007, vol.12, No.1). During these seminars, Prof Oklobdzija encouraged me to establish a SSCS chapter.

I contacted the Section Chair, Dr Douglas Chai, circulated the petition, collected signatures and forward them to the SSCS team in Piscataway. Then everything went very fast. On 11 July a new chapter in Western Australia was born. In time, I aim for the Western Australian Chapter to become a solid foundation for members to use as an innovation platform.

Western Australian Chapter Mission

The new Chapter is a joint association between three Sections: Solid State Circuits (SSCS), Electron Devices (EDS) and Laser and Electro-Optics (LEOS). Many activities in this region are indeed covered by these three Societies, but the objective is eventually to split the Chapters into two or three as the number of members grows and activity increases.

As the founder of the Western Australia Chapter, I will endeavour to:

- invite distinguished researchers/lectures to Western Australia;
- maintain a list of members and invite new members to join;
- set up a website for the Chapter;
- organise IEEE SSCS conferences and symposia;
- hold meetings and seminars for members.

However, our first action item will be to ensure that SSCS plays a significant role in Western Australia so that the links within the Western Australian engineering community grow stronger.

About the Author

Adam Osseiran (M'92-SM'06) obtained the B.Sc. degree in 1981 and the M.Sc. in 1982 from the University Joseph Fourier in Grenoble-France. He obtained the Ph.D. in 1986 from the INPG, National Polytechnic Institute of Technology in Grenoble, France.

Adam is currently Associate Professor at Edith Cowan University in Perth, and the Director of the Australian National Networked TeleTest Facility, a Major National Research Facility project. He has held positions as Professor, Consultant, Sales and Technical Director, Senior Research Fellow and instructor to many engineers on microelectronics design and design for test in both the academic and industrial arenas.

He was Chair of the Working Group of the IEEE Std 1149.4 Mixed-Signal Test Bus 2000-2005; Vice Chair, Test Technology Technical Council (Asia) of the Computer Society; General Chair of the IEEE IMSTW 2002; General Chair of the IEEE DELTA 2004; General Chair of the VLSI-SOC 2005; Vice General Chair of IEEE IDT 2006; Program Chair of several Conferences and member of several Conference Steering and Program Committees. Adam Osseiran was the invited editor of the Microelectronics Journal Special edition in 2002.

Nizhny Novgorod Confers M. S. Dissertation Awards

SSCS/EDS Chapter Subsidies Underwrite 2007 Program

Yuri Belov, Chair, SSCS-Nizhny Novgorod, belov@nirfi.sci-nnov.ru

Prof. Belov congratulates Ms. A. V. Manina, a co-winner of the 2007 State Technical University of Nizhny Novgorod best M.S. dissertation award.

Prof. Belov with outstanding Nizhny Novgorod M.S. recipients of 2007, Mr. A. Belinsky (at left) and dissertation award winner Mr. D. V. Metel'kov (at right).

The State Technical University of Nizhny Novgorod presented dissertation awards in June to two masters' degree recipients belonging to the SSCS-Nizhny Novgorod chapter. Ms. A. V. Manina was recognized for "CAD development of two-channel on-board telemetry control unit with FPGA components," and Mr. D.V. Metel'kov for "Sensor for measurement of gas-liquid flow density."

M.S. candidates at the State Technical University of Nizhny Novgorod are required to submit their work to one of several State Attestation Commissions every year at the beginning of June. Each Commission typically considers 10-15 submissions, rating them and conducting interviews. This year, the Commission on Radioengineering for Communication and TV presented SSCS-Nizhny's award winners with two books -- Leont'ev's "Complete PC Encyclopedia" (BHV St. Petersburg, 2007) and E. Finkelstein, "Auto CAD 2007 and Auto CAD LT 2007 Bible" (Wiley, Inc. 2007).

IEEE SSCS/EDS chapter subsidies financed the 2007 Nizhny Novgorod MS dissertation award program.

Summer Workshop on SDR in Radio Equipment Sponsored by SSCS-Estonia

Peeter Ellervee, Chair, SSCS-Estonia, lrv@cc.ttu.ee

Since 2001, the joint IEEE SP001/CAS004/SSC037 Chapter of the IEEE Estonia Section has organized annual two-day workshops at the end of August for IEEE members to meet and discuss various topics – organizational, industrial, educational, etc. It should be noted that the workshops have always been open to other IEEE members and non-members and are always on the same days – August 19-20 – when summer vacations have ended (or are just ending) and the academic year in universities has not yet started.

Every year, there have been presentations both from industry and academia about very different topics. Some examples from industry: "30 years of ASIC in Estonia" (2001), "Modern Railway Communication System GSM-R" (2002), "Development of outsourcing in electronics industry" (2003), "Modern naval communication and Cybernetica" (2005), "SDR in radio equipment" (2007). A lot of discussions have been about how to educate engineers. In addition, there have been presentations about issues that, at first glance, may seem to be unrelated to electronics, e.g., "Robot fish for environmental measurements of Baltic Sea" (2004), "History of electric guitars" (2006), "With GPS at Elbrus" (2007). Now and then there have been presenters from outside Estonia – Daniel Foty in 2002 (MOS modeling) and Paolo S. R. Diniz in 2004 (Multicarrier Communication Systems).

Some participants at the SSCS- Estonia summer workshop at Sagadi Manor (2002).

In the first three years, the workshop was held at Sagadi Manor – an old but renovated manor complex on the northern coast of Estonia. In 2004, it was decided to have the workshop at different places to allow attendees to see different locations and to study some interesting historical facts. For instance, in 2005 the workshop was held at Janeda Manor where writer H. G. Wells had stayed as a guest of the owner in the summer of 1934. In 2004 and 2006, the workshop was held at Waide Motel in southern Estonia. This year the workshop will take place at Roosta Holiday Village on the north-west coast of the country.

The number of participants has varied depending on the location – one can say that the further from Tallinn, the capital, the smaller the number. It should be noted that the small size of the Chapter (23 IEEE members) limits the number of participants, although the number of participating IEEE members has been rather stable – mostly 13 or 14. The total number of participants has been between 20 and 39.

Due to the establishment of the Estonia Section in 2006, this year's workshop was organized with the cooperation of three chapters. One of the notable results was an increase in participation – 19 IEEE members were present, three of whom were students. The total number of participants was 26 (30% up from the lows of the last two years) and nine were from industry.

The presentation topics this year ranged from using electronics in medicine to using GPS in mountains, to guiding the teaching/learning process. The presentations that provoked interesting discussions were:

- "With GPS at Elbrus Peak" (Kalle Tamnmemäe, Tallinn University of Technology / IT College);
- "Lab-on-the-Chip" (Mart Min, TUT);
- "Dynamics of study process – regularities, control, estimations" (Vello Kukk, TUT);
- "SDR in radio equipment" (Toomas Ruuben, TUT);
- "Introduction to Digital Audio Workstation" (Rein Sabolotny, NSC Estonia).

SSCS Extra Chapter Subsidy Funds Short Course on Digital RF Design in Taiwan

IEEE SSCS Taipei Chapter

Dr. Chih-Ming Hung presented a lecture on "Digital RF Processor (DRPTM) Strategy and Technology of TI's Wireless SoC" at National Chiao-Tung University, Hsinchu, Taiwan in July.

After Dr. Hung's lecture at National Taiwan University, Taipei, Taiwan. (Center of front row: Dr. Chih-Ming Hung; the 4th person from the right: Prof. Shen-Iuan Liu, Taipei Chapter Chair).

The approach of digital RF design has recently generated much interest, for it capitalizes the benefit of CMOS process scaling. In light of its technical merits and potential applications, the Taipei Chapter organized a two-day short course on the topic of digital RF design entitled "Digital RF Processor (DRPTM) Strategy and Technology of TI's Wireless SoC." The invited speaker was Dr. Chih-Ming Hung, who is a senior technical staff member and RF design manager at Texas Instruments (TI).

Approximately 60 participants attended the lecture in Hsinchu on 3 July, and 50 gathered to hear it at National Taiwan University, Taipei, the next day. About two-thirds of the attendees are students and university faculty from academia, indicating this topic has drawn lots of attention in the academic research community.

The course began with the definition and fundamentals of digital RF design. Dr. Hung then went on to talk about the realizations of digital PLL, digital transmitters, and digital receivers in detail. He described the design methodology and presented several examples. The intensive use of logic gates and DSP in RF/analog designs has raised the complexity and difficulty level in circuit simulation. Dr. Hung also discussed this important issue and suggested that co-simulation with software may be considered. In the last part of his lecture, Dr. Hung shared many of his design experiences with the audience. Practical design aspects, such as ESD, package and PCB design, and production testing were also covered.

Dr. Hung, who has many years of practical IC development and research experience, brought a good mix of design knowledge to the lecture. His short course was well-received by the attendees, and many considered its content a great value to their research and work.

The Taipei Chapter greatly appreciates the partial financial support from the IEEE Solid-State Circuits Society in organizing this event.

Sansen Elected SSCS President

Boser Elected SSCS Vice-President

At its September meeting, the Society's Administrative Committee elected Willy Sansen to serve as President beginning 1 January 2008. Bernhard Boser was elected to serve as Vice-President beside Sansen. After two years, the Vice-President is typically elected President by the AdCom.

Sansen will be the first non-US based officer of the Society, whose membership comprises equal numbers of US and non-US based residents. The President and Vice-President must have been previously elected to AdCom positions.

Willy Sansen received the MSc degree in Electrical Engineering from the Katholieke Universiteit Leuven in 1967 and the Ph.D. degree in Electronics from the UC Berkeley in 1972.

In 1972 he was appointed by the National Fund of Scientific Research (Belgium) at the ESAT laboratory of the K.U.Leuven, where he has been a full professor since 1980. During the period 1984-1990 he was the head of the Electrical Engineering Department. Since 1984 he has headed the ESAT-MICAS laboratory on analog design, which counts about sixty members and which is mainly active in research projects with industry. He is a fellow of the IEEE and is a member of several boards of directors.

He has been a visiting professor at a number of Universities and companies: Stanford University in 1978, the EPFL, Lausanne in 1981, the University of Pennsylvania in 1985, the T.H. Ulm in 1994, and Infineon, Villach in 2004.

Prof. Sansen is a member of several journal editorial and conference program committees. He is cofounder and organizer of the workshops on Advances in Analog Circuit Design (AACD) in Europe. He is a member of the executive and program committees of the ISSCC. He was program chair of the ISSCC-2002 conference. He is now in charge of the educational activities of the ISSCC and its Long-Range Planning Committee.

He has been involved in design automation and in numerous analog integrated circuit designs for telecommunications, consumer electronics, medical applications and sensors. He has been supervisor of over 55 Ph.D. theses in these fields. He has authored and coauthored fifteen books, including the PPT-based book on "Analog Design Essentials." He has published more than 580 papers in international journals and conference proceedings.

Prof. Bernhard E. Boser received the Diploma in Electrical Engineering from the Swiss Federal Institute of Technology in 1984 and the M.S. and Ph.D. from Stanford University in 1985 and 1988. In 1988 he became a Member of the Technical Staff of the Adaptive Systems Department at AT&T Bell Laboratories. In 1992 he joined the faculty of the Department of Electrical Engineering and Computer Sciences at UC Berkeley, where he also serves as a Director of the Berkeley Sensor & Actuator Center.

Dr. Boser's research is in the area of analog and mixed signal circuits, with special emphasis on analog-digital interface circuits and micromechanical sensors and actuators. He has served on the program committees of the International Solid-State Circuits Conference, the Transducers Conference, the VLSI Symposium, and the Sensor and Actuator Workshop. He was the Editor of the IEEE Journal of Solid-State Circuits and is currently the Chair of the Publications Committee of the IEEE Solid-State Circuits Society.

Dr. Boser is a Fellow of the IEEE. He is the Chief Scientist of SiTime, a fabless semiconductor company he co-founded in 2004. In 2005/06 he was a visiting professor at the Institute of Micro- and Nanosystems at the Swiss Federal Institute of Technology in Zurich.

SSCS Bylaws Change to Permit Online Petition Candidates

Last year IEEE updated its bylaws for petition candidates. In line with the changes, IEEE developed new software to enable rapid online authentication of member support for petition candidates. Once the rules and software were in place, the process was rolled out to all Society elections. This year, SSCS AdCom voted to revise its process for petition candidates to be in keeping with IEEE rule updates. Additional updates to the SSCS Bylaws include changes to the definition of "quorum" and the appointment of AdCom ad hoc committees. The AdCom dropped the decade-old section of the Bylaws that defined the process for SSCS to transition from a Council to Society. Higher level IEEE bodies have reviewed and approved these bylaw changes, which will take effect as soon as the membership has been notified of them by publication in the Society's News.

Preparing the Slate of Candidates for SSCS AdCom

In the typical process to prepare for elections, a nominating committee for an IEEE or Society body evaluates its future needs and recruits members to run on a slate of contested candidates. Interested members sometimes approach a nominating committee with their own suggestions or even self-nominate. After a nominating committee announces its slate, a petition process is available for additional candidates. The SSCS process ensures that the nominating slate is announced in the summer news issue. Then time is set aside for the petition process to complete so that additional candidates may qualify to be on the slate. An online petition, if requested, is set up by IEEE Corporate, but paper petitions are still allowed. The election takes place in the fall. The summer 2007 news issue included a description of the process for anyone who chose to nominate and advance a candidate by the petition process.
www.ieee.org/portal/pages/sscs/07Summer/AdCom.html

IEEE Bylaw I-308.16 defines the number of signatures needed for a petition candidate: 2% of the eligible voting members of the body. The original decade-old petition process in the SSCS Bylaws required fewer signatures and was done in parallel with the nominating committee, rather than as an alternative action after the announcement of the nominating committee's slate. The new process was required to be used for the 2007 candidate slate to be in keeping with IEEE bylaws which supersede the Society's.

Changes to SSCS Bylaws sscs.org/AdCom/bylaws.htm

3.0 ADMINISTRATIVE COMMITTEE (ADCOM)

Article V, Section 1, of the Constitution provides that the Administrative Committee (herein after referred to as the AdCom) shall consist of 15 elected members-at-large plus ex-officio members. **As stated in** ~~Bylaw~~ Section 7.2 **the SSCS will follow IEEE bylaws in the definition of a quorum**. ~~provides that a quorum shall be ten members having full voting privileges~~. However, adoption of a bylaw or amendment to a bylaw, shall be governed by the provisions of Article IX, Section 2 of the Society Constitution.

4.1 Nominations Committee

~~The President shall appoint a Nominations Committee by December 1 of each year, which shall consist of a Chair and four or more members of the Society, not more than half of which may be sitting members of AdCom~~.**The SSCS will follow** IEEE Bylaw I-308.1 **to form the nominations committee.**

4.2 Nominations

The Nominations Committee Chair shall call for nominations from the Society membership in an issue of a Society publication ~~going~~ **available** to all members by the end of ~~February~~ **January** of the year of the election. The announcement will include procedures for submission of nominations by petition. **Nominations from the Society membership must be received by the Society Executive Director by the end of February of the year of the election.** ~~The Nominations Committee Chair shall in time for the ballots to be mailed by September 15th provide names of the nominees and biographical sketches to the IEEE Technical Activities Department for preparation, mailing, and tallying of ballots. A slate~~ **By the end of April, the Nominations Committee Chair shall collaborate with the Nominations Committee to determine its slate of candidates.** ~~A slate~~ **The** number of candidates must be at least 1.5 times the number of vacancies to be filled must be supplied.

4.4 Petition Candidates

A petition nominating a Society member meeting the eligibility requirements and supported by ~~the identifiable signatures of at least 10 voting members of the Society~~ **required number of Society members through a petition process defined by** IEEE Bylaw I-308.16 **and** IEEE Policy 13.7.3.c shall automatically place that member's name on the slate of nominees, provided **a statement declaring the interest to submit** such a petition is received by the Society Executive Director by August 1 and the petition **is completed with the required support and** received by the Nominations Committee Chair no later than ~~May~~ **September 1**. Such petitions must be submitted with the knowledge and agreement of the nominee.

7.2 Quorum

~~Ten members of the AdCom who have full voting privileges shall constitute a quorum, except as provided otherwise herein.~~ **The SSCS will follow** IEEE Bylaw I-300.5 **in the definition of a quorum.** Each member of the AdCom shall have only one vote irrespective of the number of AdCom positions with vote currently held, and can be counted only once for the purposes of a quorum.

12.0 AD HOC COMMITTEES

Special or ad hoc committees may be created by the ~~AdCom~~ **President with the advice and consent of the Administrative Committee.** For each such case, the ~~AdCom~~ **President** shall specify the number of members the committee shall have, how the members are to be selected, and the terms of the members if other than for the life of the committee. Special or ad hoc committees shall be dissolved automatically after two years unless the ~~AdCom~~ **President** sets an expiration date. Chairs of such ad hoc committees shall be ex-officio members of the AdCom without vote.

All of Section 16 on the topic Transition from Council to Society will be deleted.

New Publications Available to SSCS Members in 2008

As the result of SSCS membership in IEEE Councils, Society members will be eligible for discount subscriptions to two additional publications, a new publication package, and one complimentary magazine in 2008:

IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems
A monthly print, electronic, or print and electronic publication by the IEEE Council on Electronic Design Automation, an inter-society group comprised of AP, CAS, C, ED, MTT and SSC.
PER139-PRT (Air freight addition: $112) $34
PER139-ELE $26
PER139-EPC $39

IEEE Journal of Selected Topics in Applied Earth Observations and Remote Sensing (J-STARS)
A quarterly print publication with free electronic access for one year produced by the Geoscience and Remote Sensing Society and IEEE Committee on Earth Observations, to debut in March 2008.
PER215PRT $30

Technology Management Package
IEEE Transactions on Engineering Management (print and electronic)
IEEE Engineering Management Review (print and electronic abstracts)
Newsletter
A quarterly collection offered by the new IEEE Technology Management Council, including AES, BT, CAS, COM, C, ED, IE, LEO, RL, SP, SMC, SSC and VT.
MEMO14 (Air freight addition: $148) $30

The Nanotechnology Magazine, a new quarterly publication of the Nanotechnology Council, will be mailed to SSCS members at no cost.

Renew your IEEE membership for 2008 on line.

CEDA Sponsors IC Routing Contest at ISPD

IEEE CEDA cosponsored the International Symposium on Physical Design (ISPD), organized by ACM and held on 18-21 March 2007.

An IC global routing contest at the symposium showcased new directions for research in IC routing algorithms. Two sets of benchmarks were released, corresponding to 2D and 3D routing instances, and teams were invited to produce global-routing solutions for them.

"The purpose of the contest is to guide researchers toward most urgent challenges in the EDA industry and also to map out state-of-the-art solutions," said ISPD 2007 chair Patrick Madden, associate professor at the State University of New York at Binghamton. Routers were compared on the basis of the number of routing violations (overflows) and total routing-wire length. David Pan, ISPD 2007 program chair and professor at the University of Texas at Austin, noted that there's still some controversy over the methods used to compare routers. "The ISPD community is still trying to define a good metric," Pan said.

Eleven teams from academic and research institutes participated in the ISPD contest. A prize was awarded for the entry that achieved the best overall results in each category. In addition, CEDA sponsored a prize for the best results achieved by an openly available router.

The winning entry in the 2D category was Fairly Good Router (FGR), written by Jarrod Roy, a graduate student at the University of Michigan, Ann Arbor. "We plan to open-source it to boost research in routing and help improve commercial EDA tools," said Igor Markov, associate professor at the University of Michigan, Ann Arbor.

The winner of the 3D category was Maize Route, written by Michael Moffitt, also a graduate student at the University of Michigan, Ann Arbor. "High-quality and publicly available global routers will be very helpful for CAD research," explained Lou Scheffer, Cadence Design Systems Fellow and ISPD 2006 chair. "Also, existing global routers should make it easier to build an academic detailed router— perhaps our contest for next year."

CEDA Distinguished Speaker Series

The Council's Distinguished Speaker Series will feature in-depth presentations of the best works in EDA over the past year, as demonstrated by their reception at CEDA-sponsored conferences, such as the International Conference on Computer Aided Design (ICCAD) and the Design Automation Conference (DAC), and by their coverage in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. Each presentation will take place before an audience of experts, followed by a discussion. Videos of the events will be posted on CEDA's Web site (www.ieee-ceda.org). Michael Orshansky, Assistant Professor at the University of Texas at Austin and winner of the 2006 IEEE/ACM William J. McCalla ICCAD Best Paper Award, presented the fourth seminar in this series, entitled "Joint Design-Time and Post-Silicon Minimization of Parametric Yield Loss Using Adjustable Robust Optimization" at ICCAD 2006 in Santa Clara, California.

DAC: An Exciting Event

Steven P. Levitan, General Chair of 44th DAC

The Design Automation Conference (www.dac.com) took place on 4-8 June 2007 in San Diego. Celebrating its forty-fourth year with information especially about new technologies in key areas such as multicore processing and advanced manufacturing, the program covered a broad range of topics in design practice, tools, and methodology. In more than 50 technical sessions divided into 10 tracks, 161 papers selected by a diverse committee of electronic design experts covered the latest research.

Hot topics focused on both the top and the bottom of the design process, including system-level design and electronic system level (ESL) design, power analysis and low-power design, verification, and DFM. In a special session, eight short papers on “Wild and Crazy Ideas (WACI)” offered path-breaking perspectives on early stage development. The program also included eight special sessions, seven full-day tutorials, eight panels, and 18 pavilion panels. Several hands-on tutorials were available, with companies demonstrating the use of their DFM tools or design flows. There was also a day-long seminar for management teams worldwide, where leading experts could discuss innovation.

The three keynotes offered a diverse look at the field of design:

Oh-Hyun Kwon, president of the System LSI Division of Samsung Semiconductor Business, offered “A Perspective of the Future Semiconductor Industry: Challenges and Solutions.”

Jan M. Rabaey, the Donald O. Pederson Distinguished Professor in the Department of Electrical Engineering and Computer Sciences at the University of California at Berkeley, presented “Design without Borders—A Tribute to the Legacy of A. Richard Newton.”

Oh-Hyun Kwon

Jan M. Rabaey

Lawrence D. Burns

Lawrence D. Burns, vice president of R&D and Strategic Planning for General Motors, discussed “Designing a New Automotive DNA” to highlight the conference’s automotive theme, which continued with a series of events throughout the week.

Finally, of course, there was the yearly highlight of the Exhibition and Suite area, where attendees could see close to 250 of the leading and emerging EDA, silicon, and IP providers. Overall, DAC 2007 was a week filled with exciting and informative technical sessions.

CEDA Currents is a publication of the IEEE Council on Electronic Design Automation. Please send contributions to Kartikeya Mayaram (karti@eecs.oregonstate.edu) or Preeti Ranjan Panda (panda@cse.iitd.ac.in), or Anand Raghunthan (anand@nec-labs.com).

CrossRef Pilots Plagiarism Detection Service

Six Academic Publishers to Allow Full-Text Indexing

IEEE, a founding and active member of CrossRef, is participating in the launch of a new plagiarism detection service. CrossRef, the association behind publishing's preeminent shared digital infrastructure, has entered into an agreement with iParadigms (www.iparadigms.com/), the company that runs Turnitin and iThenticate, to develop a system that allows scholarly and professional publishers to verify the originality of submitted and published works. The service, when it is launched, will be called "CrossCheck." Six leading academic publishers have agreed to allow their full-text content to be indexed for the pilot, and to test the service along several measures.

According to Ed Pentz, CrossRef's Executive Director, “We’re quite excited about the launch of the CrossCheck pilot. For the first time we are applying the principles of publisher collaboration beyond reference linking. CrossRef is in a unique position to help create a comprehensive database of published academic content because of its broad membership. CrossCheck will be a valuable service for our publishers enabling them to verify the originality of content. But the real beneficiaries of the service will be researchers and scholars who want trustworthy online content. On the technology side, iParadigms is the leading provider of the technology that we need.”

Besides IEEE, the other five participating publishers are: the Association for Computing Machinery (www.acm.org/), BMJ Publishing Group Ltd. (bmjgroup.bmj.com/), Elsevier (www.elsevier.com), Taylor & Francis (www.taylorandfrancisgroup.com/), and Wiley-Blackwell (www.wiley.com).

John Barrie Ph.D., President and CEO of iParadigms, adds: “We are honored to be working with some of the most prestigious academic publishers in the world to create a service designed to improve the quality and integrity of STM research. CrossCheck is the next logical evolution of the technology behind Turnitin -- a service that has already become part of how secondary and higher education work.”

Headquartered in Oakland, CA, iParadigms, LLC (www.iparadigms.com) is the leading provider of web-based solutions to check documents for originality and plagiarism. The company’s products include Turnitin, an internet service used by tens of millions of students and faculty for the digital assessment of academic work, and iThenticate, an internet service which enables companies to determine originality and check documents for misappropriation.

CrossRef (www.crossref.org) is a non-profit membership association founded and directed by publishers. Its mission is to enable easy identification and use of trustworthy electronic content by promoting the cooperative development and application of a sustainable infrastructure. IEEE participates with CrossRef as the official DOI® link registration agency for scholarly and professional publications. It operates a cross-publisher citation linking system that allows a researcher to click on a reference citation on one publisher’s platform and link directly to the cited content on another publisher’s platform, subject to the target publisher’s access control practices. For a demonstration, try this DOI in your Google search window and access the Journal’s most frequently downloaded article this year.

IEEE Mentoring Connection™ Program Seeks Partners to Advise Young Professionals

The IEEE Solid-State Circuits Society has many young professional members. Many of them would appreciate the opportunity to have an "online" mentor to guide them in their career planning and professional development.

The IEEE Mentoring Connection™ program enables each enrollee to select a mentoring partner online from a list of individuals who have volunteered to serve as mentors. After a mentor is identified as a potential match, he or she is contacted and asked to begin establishing a relationship.

Gary Hinkle, a mentor in the program, says "Helping young engineers develop in their careers is very rewarding. Working with some of these individuals has proven to be quite a challenge because of the diversity among those seeking mentors. I'm glad to be contributing to this program."

Mentor participation in the IEEE Mentoring Connection Program™ is open to all IEEE members above the grade of Student Member. Interested members can visit www.ieee.org/web/membership/mentoring/index.html for information on the roles and responsibilities of each mentoring partner, including additional program information and an FAQ page. Potential mentors are asked to review the time and effort commitment to the program necessary to ensure a successful mentoring partnership.

To access the IEEE Mentoring Connection site, please go to www.mentoringconnection.com and use the Group ID "IEEE2006" to enter. Once you enter the site, you will need to set your own user id and password.

If you have any questions, please contact Cathy Downer, Regional Activities, at c.downer@ieee.org.

Letters to the Editor

Continued from page 2

the first one, provides much needed clarifications, and most notably includes the original 'law' formula as presented by Amdahl 4 decades ago!

Congratulations on covering the 40th anniversary of Amdahl's law in such a brilliant way!

Sincerely,
Professor Vladimir Getov
Visiting Scientist, Performance and Architecture Lab, Los Alamos National Laboratory, New Mexico, USA
Research Director, Harrow School of Computer Science
University of Westminster, London, UK

Corrections

In Volume 12, number 3 (summer 2007), page 9, bottom of the left column, in Computer Architecture and Amdahl's Law by Gene Amdahl, the claim about invalidating Amdahl's Law in 1988 came from a team at Sandia National Laboratories, and not Los Alamos. The correct text should read: "Several years later I was informed of a proof that Amdahl's Law was invalidated by someone at Sandia National Laboratories, where a number of computers interconnected as an N-cube by communication lines, but with each computer also connected to I/O devices for loading the operating system, initial data, and results."

On page 20 of the same issue, in the second sentence of the diagram explanation note by Justin Rattner, the percentage figures for the sequential and the system coordination parts of the workload were interchanged. The correct version of this sentence should read: "Assuming a fixed sized problem, Amdahl speculated that most programs would require at least 10% of the computation to be sequential (only one instruction executing at a time), with overhead due to interprocessor coordination averaging 25%."

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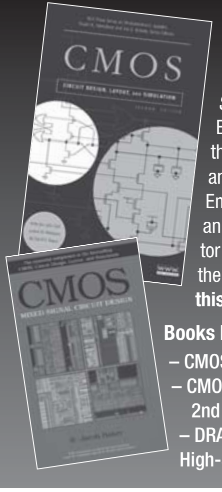


R. Jacob Baker is the 2007 winner of the Frederick Emmons Terman Award for his book *CMOS: Circuit Design, Layout, and Simulation, Second Edition.* Established in 1969 by the Electrical and Computer Engineering Division of the American Society of Engineering Education and sponsored by Hewlett-Packard, the Frederick Emmons Terman Award is bestowed annually upon an outstanding young electrical engineering educator in recognition of the educator's contributions to the profession. **Congratulations to Dr. Baker on this incredible achievement!**

Books by Dr. Baker:

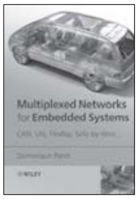
– CMOS, Mixed-Signal Circuit Design
– CMOS: Circuit Design, Layout, and Simulation, 2nd Edition
– DRAM Circuit Design: Fundamentals and High-Speed Topics *(due to publish Nov 2007)*

DRAM Circuit Design
Fundamentals and High-Speed Topics
Brent Keith, R. Jacob Baker, Brian Johnson, Feng Lin
978-0-470-18475-2 • November 2007 • Cloth • List: ~~$105.00~~ • Special: $84.00
Wiley-IEEE Press

This easy-to-read book covers the transistor-level design of DRAM building blocks, including architecture and the array, voltage regulators and pumps, and peripheral circuits. *DRAM Circuit Design* presents both standard and high-speed implementations in a balanced approach to help IC designers prepare for the future, in which DRAM will be embedded in logic devices for complete systems on a chip.

Advanced FPGA Design
Architecture, Implementation, and Optimization
Steve Kilts
978-0-470-05437-6 • June 2007 • Cloth
List: ~~$99.95~~ • Special: $79.96 • Wiley-IEEE Press

Addressing advanced issues of FPGA (Field-Programmable Gate Array) design and implementation, this book accelerates the learning process for engineers and computer scientists. With an emphasis on real-world design and a logical, practical approach, it walks readers through specific challenges and significantly reduces the learning curve. Designed to enhance and supplement hands-on experience, this real-world reference is ideal for engineers and computer scientists who want to take their FPGA skills to the next level and for use as a hands-on reference.



Multiplexed Networks for Embedded Systems
CAN, LIN, FlexRay, Safe-by-Wire…
Dominique Paret, Roderick Riesco MA
978-0-470-03416-3 • July 2007 • Cloth
List: ~~$150.00~~ • Special: $120.00

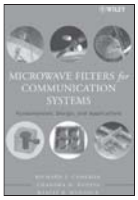
A valuable guide to embedded systems for a range of applications, *Multiplexed Networks for Embedded Systems: CAN, LIN, FlexRay, Safe-by-Wire…* is essential reading for electronics engineers and researchers developing electronics for the automotive industry. It is also useful for practising aerospace engineers and other practitioners interested in the application of network technologies, and advanced students taking courses on automotive and embedded system design.

High-Speed VLSI Interconnections, 2nd Edition
Ashok K. Goel
978-0-471-78046-5 • September 2007 • Cloth
List: ~~$145.00~~ • Special: $116.00 • Wiley-IEEE Press

The second edition of *High-Speed VLSI Interconnections* focuses on the emerging topics of optical interconnection and nanotechnology. New to this editions are section on nanotechnology circuit interconnects which include discussions of nanowires, nanotubes and wireless interconnection technologies for nanoscale circuits; sections on Parasitic Inductances and Optical Interconnections; accompanying FTP site will contain the appendices from the end of the chapters; complete and comprehensive coverage of VLSI interconnection for microelectronics programs.

Lead-Free Electronics
iNEMI Projects Lead to Successful Manufacturing
Edwin Bradley, Carol A. Handwerker, Jasbir Bath, Richard D. Parker, Ronald W. Gedney
978-0-471-44887-7 • August 2007 • Cloth
List: ~~$94.95~~ • Special: $75.96 • Wiley-IEEE Press

Reflecting the results of a two-year study, *Lead-Free Electronics* provides full coverage of the issues surrounding the implementation of Pb-free solder into electronic board assembly. This book is extremely timely–most electronic manufacturers are going to change over to Pb free soldering by 2006 to meet new European laws. All manufacturers around the globe are going to be affected by this change. The text provides specific results from the thirty company NEMI project activities. It contains integrated and fully documented book chapters with references to existing published work in the area. These serve as tremendous resources for engineers and companies faced with making the switch to Pb-free solder assembly.



Microwave Filters for Communication Systems
Fundamentals, Design and Applications
Richard J. Cameron, Raafat Mansour, Chandra M. Kudsia
978-0-471-45022-1 • July 2007 • Cloth
List: ~~$135.00~~ • Special: $108.00

There have been significant advances in the synthesis and physical realization of microwave filter networks, but until now, no book has provided a coherent and readable description of system requirements and constraints, fundamental considerations in theory and design, up-to-date synthesis techniques, or EM-based design tools. *Microwave Filters for Communication Systems* fills the need for such a book, providing comprehensive coverage of microwave filter design and applications for communication systems.

Phase-Lock Basics, 2nd Edition
William F. Egan
978-0-470-11800-9 • September 2007 • Cloth
List: ~~$99.95~~ • Special: $79.96 • Wiley-IEEE Press

This book is a broad-based, hands-on text, designed to be both easy to understand and easy to customize. When used with MATLAB simulation software, the book becomes a virtual laboratory for working professionals who want to improve their understanding of the design process and apply it to the demands of specific situations. Extensive new simulations include MATLAB scripts that enable the reader to duplicate and expand these experiments. This second edition begins with a large body of new statistical data obtained from simulations and uses available experimental data for confirmation of the simulation results. It then progresses to analysis and approximations whose limits of applicability are evident from the previously presented simulations.

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Contact: Ms. Kathy MacLennan
kathy@mpassociates.com

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vlsidat.itri.org.tw
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Hsinchu, Taiwan
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Contact: Ms. Stacey C.P. Hsieh
stacey@itri.org.tw

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kevin@mpassociates.com

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lloydsl@ieee.org

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Palo Alto, CA, USA
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www.islped.org/ http://www.islped.org/
Aug 2008
Contact: Diana Marculescu,
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ESSCIRC/ESSDERC 2008 - 38th European Solid State Circuits/DeviceResearch Conferences
www.esscirc2007.org
15 Sep - 19 Sep 2008
Edinburgh, Scotland
Contact: Bill Redman-White, ESSCIRC Chair
bill.redman-white@nxp.com

2008 IEEE Integrated Circuit Ultra-Wide Band ICUWB
www.icuwb2007.org
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chiamichael@i2r.a-star.edu.sg

2008 IEEE Bipolar/BiCMOS Circuits and Technology Meeting - BCTM
www.ieee-bctm.org
Contact: Ms. Janice Jopke
ccs@mn.rr.com

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