



Volume 11
Number 2
May 2006

SOLID-STATE CIRCUITS

IEEE Solid-State Circuits Society Quarterly Newsletter

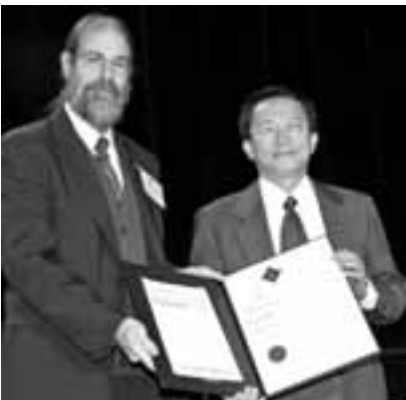


Frank Chang Recognized for Modern Cell Phone Technology and WLAN Systems

Mau-Chung Frank Chang Receives 2006 IEEE David Sarnoff Award

Dr. Mau-Chung Frank Chang received the 2006 IEEE David Sarnoff Award in a ceremony during the Plenary Session of ISSCC 2006 on 6 February, 2006. Dr. Chang was honored for the development of heterostructure bipolar transistors (HBT) power amplifiers leading to their commercialization in wireless communications.

“Dr. Chang is regarded as the driving force behind the development and commercialization of GaAs-based heterostructure bipolar transistors” said



Dr. Michael Lightner, 2006 IEEE President and IEEE Board of Directors representative at the ceremony. “He took



what was once considered theoretical technology and enabled reliable, readi-

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Gabor Temes Honored for Analog Signal Processing Fundamentals

Gabor C. Temes Receives 2006 IEEE Gustav Robert Kirchoff Award

In a ceremony during the Plenary Session of ISSCC 2006, Dr. Gabor C. Temes received the 2006 IEEE Gustav Robert Kirchoff Award for his fundamental contributions to analog-signal-processing techniques. This IEEE Technical Field

Award recognizes outstanding contributions to the fundamentals of any aspect of electronic circuits and systems that have long-term significance or impact.

An IEEE Life Fellow and Professor or

Continued on page 3



Frank Chang Article, Continued from page 1

ly-manufactured commercial devices critical to the broadband, linear, efficient and low-cost power amplifiers in most of today's cellular telephones and wireless local area networks (WLANs)" he said.

Dr. Chang "pioneered the development and technology transfer of the GaAs HBT while a staff member at the Rockwell Science Center in Thousand Oaks, California. He investigated and resolved gain degradation problems that had branded the transistor technology as unreliable and difficult to fabricate under high-current operation conditions," said Dr. Lightner. "Dr. Chang developed the emitter ledge formation process and implemented effective monitoring methods to manufacture highly reliable GaAs HBTs and power amplifiers. Today, about 80 percent of cellular tele-

phones and all WLAN systems use the GaAs HBT technology developed by Dr. Chang for power amplification in transmitters," he said.

Dr. Chang received a B.S. in physics from National Taiwan University in 1972, and a Ph.D. in Electrical Engineering from National Chiao-Tung University, Taiwan, ROC in 1979. He is currently a full Professor at the Electrical Engineering Department and Director of the High Speed Electronics Laboratory at UCLA. He is a Fellow of the IEEE and a co-editor of the IEEE Transactions on Electron Devices. Dr. Chang was also a guest editor for the IEEE Journal of Solid-State Circuits in 1991 and 1992 and for the Journal of High Speed Electronics and Systems in 1994.

Before joining UCLA, he was the Assistant Director of the High Speed

Electronics Laboratory at the Rockwell Science Center (1983-1997). During that period of time, he developed and transferred the AlGaAs/GaAs HBT technology from the research laboratory to the production line (Conexant Systems). The HBT production has now grown into a multi-billion dollar business worldwide.

Dr. Chang's research work has been mostly in the development of high-speed semiconductor devices and integrated circuits for mixed signal communication and sensor system applications. He was the principal investigator at Rockwell to lead the US-DARPA ADC and DAC development for direct conversion transceiver (DCT) and digital radar receivers (DRR) systems. He was the inventor of the multi-I/O reconfigurable RF/wireless interconnects based on FDMA/CDMA multiple access algorithms for inter- and intra-ULSI communications. His research group has demonstrated the world's first source synchronous CDMA bus interface with reconfigurable multichip access capability. He also led the first demonstration of a 2Gsps 6bit ADC in CMOS, a 1Gsps 11bit THA in SiGe and a dual mode (CDMA/AMPS) power amplifier in SiGe for wireless handset applications.

He has authored over 200 technical papers and 10 book chapters, edited 1 book, and hold 17 U.S. patents. He was honored with Rockwell's Leonardo Da Vinci (Engineer of the Year) award in 1992, the National Chiao-Tung University's Distinguished Alumni Award in 1997, and National Tsing-Hua University's Distinguished Alumni Award in 2002. He was named an IEEE Fellow in 1996 for his contributions in ultra-high speed HBT integrated circuit development. ■

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For questions regarding Society business, contact the SSCS Executive Office.

Contributions for the May 2006 issue of the e-News must be received by 15 May 2006 at the SSCS Executive Office.

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Gabor Temes Article, Continued from page 1

Engineering at Oregon State University, Dr. Temes has published prolifically on analog and digital signal processing and mixed-signal integrated electronics, “progressing from classical network theory to active filter synthesis to monolithic filter and data converter design,” said Dr. Michael Lightner, 2006 IEEE President and IEEE Board of Directors representative at the ceremony. “Without his work on analog-to-digital converters, DSL and cable-modem Internet connections would be much slower than they now are, and the data density of hard disk drives would also be lower than that in today’s systems,” he said.

“Dr. Temes’ research on filter design, optimization methods and low-sensitivity filter structures has significantly helped the explosive growth of analog signal processing in MOS integrated circuit technologies during the last 30 years.” He may truly be considered “one of the ‘fathers’ of the field of modern analog and mixed-signal circuits – a field of extraordinary industrial importance in the modern world.”

Dr. Temes received his undergraduate education at the Technical University and Eotvos University in Budapest, Hungary, from 1948 to 1956, and his Ph.D. in Electrical Engineering from University of Ottawa, Canada in 1961. He received an honorary doctorate from the Technical University of Budapest in 1991.

In addition to his appointment at Oregon State, Dr. Temes has held academic positions at the Technical University of Budapest, at Stanford University and at UCLA, and worked in industry at Northern Electric R&D Laboratories (now Bell-Northern Research), as well as at Ampex Corp. He has served as Department Head at both UCLA and Oregon State University.

A Life Fellow of the IEEE, Dr. Temes served as Associate Editor of the Journal of the Franklin Institute, Editor of the IEEE Transactions on Circuit Theory, and Vice President of the IEEE Circuits and Systems Society (CAS). In 1968 and 1981, he was co-winner of the CAS Darlington Award, and in 1984 received the Centennial Medal of the IEEE. He received the Andrew Chi Prize Award of the IEEE Instrumentation and Measurement Society in 1985, the IEEE Circuits and Systems Society Education Award in 1987 and the Technical Achievement Award in 1998, and the IEEE Millennium Medal as well as the IEEE CAS Golden Jubilee Medal in 2000.

Co-editor and co-author of “Modern Filter Theory and Design” (Wiley, 1973) and “Oversampling Delta-Sigma Data Converters” (IEEE Press, 1997), and co-author of “Introduction to Circuit Synthesis and Design” (McGraw-Hill, 1977), “Analog MOS Integrated Circuits for Signal Processing” (Wiley, 1986), Dr. Temes has published approximately 300 papers in engineering journals and conference proceedings and contributed to several other edited volumes. ●

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PEOPLE

24 SSCS Members Elevated to IEEE Fellow in Class of 2006

7 SSCS Nominees Attain Highest IEEE Membership Grade

The IEEE Board of Directors selected 24 members of SSCS, including 7 evaluated by the Society, for elevation to the rank of IEEE Fellow. There are a total of 271 Fellows in the Class of 2006. No more than one-tenth of one percent of the Institute membership may be elevated to Fellow in a given year. The distinction recognizes extraordinary contributions to one or more fields of IEEE interest.

Dr. Michael Lightner, IEEE President and Board of Directors representative at ISSCC 2006, congratulated five Fellows evaluated by SSCS and Dr. Naresh Shanbhag, who was evaluated by the Circuits and Systems Society and chose to receive his plaque at ISSCC. Dr. James (Brock) Barton and Dr. David Su were unable to attend.



Dr. Bhupendra Ahuja



Dr. Tohru Furuyama



Dr. William Krenik



Dr. Tadahi Kuroda



Prof. Naresh Shanbhag



Prof. Richard Spencer

The 7 IEEE Fellows of 2006 evaluated by SSCS are:

- Dr. Bhupendra Ahuja
- Dr. James (Brock) Barton
- Dr. Tohru Furuyama
- Dr. William Krenik
- Prof. Tadahi Kuroda
- Prof. Richard Spencer
- Dr. David Su

The 17 SSCS-member IEEE Fellows of 2006 evaluated by other societies are:

- Prof. Andreas Andreou
- Prof. Steve Chung
- Dr. Hector De Los Santos
- Prof. Paul Franzon
- Prof. Ramesh Harjani
- Prof. Qin (Alex) Huang
- Prof. Andre Ivanov
- Prof. Bin-Da Liu
- Dr. Frederick Raab
- Dr. Resve Saleh
- Prof. Gianluca Setti
- Prof. Naresh Shanbhag

- Prof. Yu-Chong Tai
- Dr. Tsuneo Tokumitsu
- Dr. Huei Wang
- Dr. Katsuyoshi Washio
- Dr. Burnell West



Dr. Bhupendra Ahuja
Intersil Corporation
for contributions to design of mixed signal complimentary metal oxide semiconductor (CMOS) integrated circuits for telecommunications and computer communications systems.

Bhupendra K. Ahuja received his B.Tech. degree from Indian Institute of Technology, Kanpur, India, in 1973 and his MS and PhD degrees in Electronics Engineering from Carleton University, Ottawa, Canada, in 1976, and 1978.

During his career at AT&T Bell Laboratories (1978 to 1980), he led the first CMOS implementation of single-chip

CODEC with Switched-Capacitor filters. This product was manufactured in very large volume, eventually finding its way into majority of Line-Card of the 80's. From 1980 to 1992, he worked at Intel Corporation developing more complex Telecom IC's and later on the first Pentium design.

One of his well known contributions that bears his name is a novel frequency compensation technique for CMOS operational amplifiers. It removes the limitations of Miller-Compensation, achieves wider bandwidth and better power supply rejection. This technique, widely known as the "Ahuja Compensation," was published in JSSC in 1983.

From 1992 to 2002, he worked at several small companies and startups developing low power, high speed mixed analog chips for PC graphics controllers, ADSL line drivers, Digital Camera and SONET transceivers. Since 2003, he has

worked at Intersil Corp. as Director of Engineering on Precision Analog products where he is leading the development of Ultra Low Power Precision Floating Gate Voltage Reference products. Dr. Ahuja has published numerous technical papers and holds many patents in the area of CMOS Analog IC designs.



Dr. James (Brock) Barton

Texas Instruments
for contributions to the design of digital signal processing integrated circuits.

Brock Barton is a Texas Instruments Fellow, in TI's DSP Systems/Silicon Development organization. He received the B.S. and B.A. degrees in physics and mathematics, respectively, from the University of Texas, Austin, in 1966. He received the Ph.D. in solid-state physics from the Massachusetts Institute of Technology in 1971. He joined TI in 1972 and has worked in TI's Equipment Group, Central Research Laboratories, Semiconductor Group, Semiconductor Process and Design Center, and DSP Solutions R&D Center, before moving to DSP Development. He was responsible for the design of TI's first standard cell library. He has worked on a number of different programs, including CCD imager and memory design and development, and CMOS calculator chip product engineering, prior to helping create TI's ASIC technology. He was responsible for fuzzy logic R&D and 1V DSP chip design in the DSPS R&D Center. More recently, he led the TI 65nm High Performance SRAM Power Management Team, and serves on the TI Technology Roadmap Team. He is currently working in the Advanced Architecture and Chip Technology group, on silicon technology-related issues related to design with new process flows. He was Co-Chairman of the Technical Program Committee for the 1996 IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED'96), and Co-General Chairman of ISLPED'97. He is on the Executive Committee for ISLPED, 1996-present. He is the TI representative to the MARCO C2S2 (Center for Circuit and Systems Solutions), 2003-present. He was Vice Chairman, IEEE

Solid-State Circuits Society, Dallas Chapter, 2000-01.



Dr. Tohru Furuyama
Toshiba Corporation
for contributions to high speed dynamic random access memory (RAM) design and technologies.

Tohru Furuyama received the B.S. degree in physics from the University of Tokyo, Tokyo, Japan, in 1975, the M.S. degree in electrical engineering from Cornell University, Ithaca, NY, in 1984, and the Ph.D. degree in information science from the University of Tokyo in 1988.

Dr. Furuyama led several commodity DRAM and Rambus DRAM developments and the embedded DRAM (eDRAM) project for graphics applications at the Semiconductor Device Engineering Laboratory, Toshiba Corp. He also worked on research of new circuit technologies including sense amplifiers and on studies of reliability issues, such as particle induced soft errors, hot carrier related problems, and wafer level burn-in technologies. From 1994 to 1996, he was the 64Mb DRAM design manager for the Toshiba/IBM/Siemens trilateral joint DRAM development project at Burlington, VT. He was then a senior manager at the System LSI Engineering Laboratory, Toshiba Corp, where he was responsible for the developments of Toshiba's original "Media embedded Processor" (MeP), MPEG-4 codec LSI's for mobile applications that utilized the eDRAM technology he had established as a project leader. Since 2002, he has been a general manager of the SoC Research & Development Center, Semiconductor Company, Toshiba Corp., where he has been supervising the wide range of R&D activities: advanced CMOS technologies, NAND flash memories, embedded memories, novel memories, embedded processors, various digital media related SoC, and software developments.



Dr. William Krenik
Wireless Terminals
Business Unit
Garland, TX
for contributions to integrated circuits and technology for wireless products.

Bill Krenik received a BEE degree from the University of Minnesota in 1984, an MSEE degree from Southern Methodist University in 1987, and a Ph.D. in Electrical Engineering from the University of Texas at Dallas in 1993. Bill holds 38 U.S. patents with several more pending, he has published numerous technical papers and speaks regularly at industry and technical conferences. He is a registered professional engineer in Texas.

Since 1984, he has been with Texas Instruments in Dallas in a variety of management and technical roles. He is presently the Wireless Advanced Architectures Manager with responsibility for development of advanced wireless technology. Bill's team assesses new technology, participates in standards activity, develops key technology for use in future products, and supports new product activity in emerging market spaces. His research interests include communications technology, cognitive radio, software defined radio, analog/RF IC design, and wireless handset technology. Prior to his present role, Bill held general management positions over TI's RFIC and hard disk drive analog IC businesses.



Prof. Tadahiro Kuroda
Keio University,
Yokohama,
Kanagawa, Japan
for contributions to low-power and high-speed very large scale integrated (VLSI) design.

Tadahiro Kuroda (M'88-SM'00-F'06) received the Ph.D. degree in EE from the University of Tokyo in 1999. In 1982, he joined Toshiba Corporation, where he designed CMOS SRAMs, gate arrays and standard cells. From 1988 to 1990, he was a Visiting Scholar with the University of California, Berkeley, where he conducted research in the field of VLSI CAD. In 1990, he was back to Toshiba, and engaged in the research and development of BiCMOS ASIC's, ECL gate arrays, high-speed CMOS LSI's for telecommunications, and low-power CMOS LSI's for multimedia and mobile applications. He invented a Variable Threshold-voltage CMOS (VTCMOS) technology to control V_{TH} through sub-

strate bias, and applied it to a DCT core processor and a gate-array in 1995. He also developed a Variable Supply-voltage scheme using an embedded DC-DC converter, and employed it to a micro-processor core and an MPEG-4 chip for the first time in the world in 1997. In 2000, he moved to the Keio University, and he has been a professor since 2002. His research interests include low-power, high-speed CMOS design for wireless and wireline communications, human computer interactions, and ubiquitous electronics. He has published more than 200 technical publications including 50 invited papers, 18 books/chapters, and filed more than 100 patents. He served as a conference chair for the Symp. on VLSI Circuits, a vice chair for ASP-DAC, TPC chair for the Symp. on VLSI Circuits, the invited talk program chair for A-SSCC, sub-committee chairs for ICCAD and SSDM, and program committee member for Symp. on VLSI Circuits, CICC, DAC, ASP-DAC, ISLPED, SSDM, ISQED, and other international conferences.



Prof. Naresh Shanbhag
University of Illinois
for development of a communication-centric design paradigm for low power systems on a chip.

Naresh R. Shanbhag received his Ph.D. degree in Electrical Engineering from the University of Minnesota in 1993. He worked at AT&T Bell Laboratories at Murray Hill from 1993 to 1995, where he was the lead chip architect for AT&T's 51.84 Mb/s transceiver chips over twisted-pair wiring for Asynchronous Transfer Mode (ATM)-LAN and very high-speed digital subscriber line (VDSL) chip-sets. Since August 1995, he has been with the Department of Electrical and Computer Engineering and the Coordinated Science Laboratory at the University of Illinois, where he is a Professor. His research interests are in the design of integrated circuits and systems for broadband communications, including lowpower/high-performance VLSI architectures for error-control coding equalization, as well as digital inte-

grated circuit design. He has numerous publications in this area and holds three US patents. He is also a co-author of the research monograph "Pipelined Adaptive Digital Filters" published by Kluwer Academic Publishers in 1994.

Dr. Shanbhag received the 2001 IEEE Transactions on VLSI Best Paper Award, the 1999 IEEE Leon K. Kirchmayer Best Paper Award, the 1999 Xerox Faculty Award, the Distinguished Lecturership from the IEEE Circuits and Systems Society in 1997, the National Science Foundation CAREER Award in 1996, and the 1994 Darlington Best Paper Award from the IEEE Circuits and Systems Society. From 1997-1999 and from 1999-2002, he served as an Associate Editor for the IEEE Transaction on Circuits and Systems: Part II and the IEEE Transactions on VLSI respectively. He has served on the technical program committees of various conferences.



Prof. Richard Spencer
University of California, Davis
for contributions to integrated circuits for digital communication and magnetic recording.

Richard R. Spencer received the B.S.E.E. degree from San Jose State University in 1978 and the M.S. and Ph.D. degrees in Electrical Engineering from Stanford University in 1982 and 1987, respectively.

Prof. Spencer has worked at Aydin Energy Division designing circuits for the IF section of microwave transceivers and at Memorex Corporation designing disc drive read/write electronics and an integrated circuit process monitor chip and test system. At Stanford his research concentrated on circuit design for integrated sensors. He joined the Department of Electrical and Computer Engineering at UC Davis in 1986. His research focuses on analog circuit design for RF and baseband communication. He is the primary author of *Introduction to Electronic Circuit Design*, Prentice Hall, 2003.

Professor Spencer held the Child Family Professor of Engineering endowed chair from 1999 to 2005. He

has received the UCD-IEEE Outstanding Undergraduate Teaching Award four times. He was Vice Chair for Undergraduate Studies from July 1, 2000 to June 30, 2003. He was a co-organizer of the IEEE Solid-State Circuits & Technology Committee Workshop on Integrated Sensors in 1988, and has been a session chair for the International Solid-State Circuits Conference and the Symposium on VLSI Circuits. He was a guest co-editor of the IEEE Journal of Solid-State Circuits in December 1992. He was a member of the Program Committee for the ISSCC from 1987-1993 and was the chair of the Sensors, Imagers, and Displays subcommittee from 1995-1997. He has been an editor and Executive Committee Member of the ISSCC since 2004.



Dr. David Su
Atheros Communications Corporation
for contributions to design of analog and mixed-signal integrated circuits for communications systems.

David K. Su was born in Kuching, Malaysia, in 1961. He received the B.S and M.E. degrees in Electrical Engineering from the University of Tennessee, Knoxville, in 1982 and 1985 and the Ph.D. degree in Electrical Engineering at Stanford University, Stanford, CA, in 1994. From 1985 to 1989, he worked as an IC design engineer at Hewlett-Packard Company in Corvallis, Oregon and Singapore where he designed full-custom and semi-custom application-specific integrated circuits. From 1989 to 1994, he was a Research Assistant with the Center for Integrated Systems, Stanford University. From 1994 to 1999, he was a Member of Technical Staff with the High Speed Electronics Department of Hewlett Packard Laboratories, Palo Alto, CA, where he designed CMOS analog, RF, and mixed-signal ICs for wireless communications. Since February 1999, he has been with Atheros Communications, Sunnyvale CA, where he is the Senior Director of Analog/RF Design, engaging in the design and development of integrated CMOS sys-

tems-on-a-chip for wireless communications. He has also been with Stanford University since 1997, where he is a consulting Associate Professor. His research interests include the design of RF, analog, mixed-signal, and data conversion circuits.

Dr. Su is a technical program subcommittee member of the ISSCC and an associate editor of the IEEE Journal of Solid-State Circuits. He was a co-recipient of the IEEE Journal of Solid-State Circuits 2002 Best Paper Award and the 2004 ISSCC Beatrice Winner Editorial Award.

SSCS Members – 2006 Fellows evaluated by other Societies are:

Prof. Andreas Andreou
Johns Hopkins University
for contributions to energy efficient sensory microsystems.

Prof. Steve Chung
National Chiao Tung University
for contributions to reliability in ultra-thin-oxide complimentary metal oxide semiconductor (CMOS) devices.

Dr. Hector De Los Santos
NanoMEMS Research, LLC
for contributions to radio frequency (RF) and microwave micro electromechanical systems (MEMS) devices and applications.

Prof. Paul Franzon
North Carolina State University
for contributions to chip-package codesign.

Prof. Ramesh Harjani
University of Minnesota
for contributions to the design and computer aided design (CAD) of analog and radio frequency circuits.

Prof. Qin (Alex) Huang
North Carolina State University
for contributions to emitter turn-off thyristor technology and its applications.

Prof. Andre Ivanov
University of British Columbia
for contributions to intellectual property (IP) for system on a chip (SoC) testing.

Prof. Bin-Da Liu
National Cheng Kung University
for contributions to very large scaled integrated (VLSI) processors for neural networks and video signal processing.

Dr. Frederick Raab
Green Mountain Radio Research Co.
for contributions to modeling and design of high-efficiency power amplifiers and radio transmitters.

Dr. Resve Saleh
University of British Columbia
for contributions to mixed-signal integrated circuit simulation and design verification.

Prof. Gianluca Setti
University of Ferrara
for contributions to application of nonlinear dynamics to communications, signal processing, and information technology.

Prof. Yu-Chong Tai
California Institute of Technology
for contributions to integrated nano/micro-electro-mechanical systems (MEMS) and nano/micro-fluidics for Lab-on-a-Chip applications.

Dr. Tsuneo Tokumitsu
Eudyna Devices (formerly Fujitsu Quantum Devices Ltd.)
for contributions to uniplanar and 3-dimensional monolithic microwave integrated circuits (MMICs).

Dr. Huei Wang
National Taiwan University
for contributions to broadband and millimeter-wave monolithic millimeter-wave integrated circuits (MMICs) and radio frequency integrated circuits (RFICs).

Dr. Katsuyoshi Washio
Central Research Laboratory, Hitachi, Ltd.
for contributions to high-speed silicon and silicon germanium bipolar/Bi complimentary metal oxide semiconductors (CMOS) device and circuit technologies.

Dr. Burnell West
Credence Systems Corporation
for contributions to high-performance automatic test equipment. ■

Congratulations New Senior Members

17 Elected in February

Diego Barrettino	Hawaii Section	Marco Maccarrone	Italy Section
Jose De La Rosa	Spain Section	Denis Masliah	France Section
Antoni Fertner	Sweden Section	Andrew Mason	Southeastern Michigan Section
Wesley Gee	Central Georgia Section	Robert Montgomery	Philadelphia Section
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Baher Haroun	Dallas Section	Michael Oshima	Santa Clara Valley Section
W. Matthew Hogan	Oregon Section	Mark Santoro	Santa Clara Valley Section
Chulwoo Kim	Seoul Section	Zhenhai Shao	Singapore Section
Torsten Lehmann	New South Wales Section		

TECHNICAL LITERATURE

Nguyen and Kitching Receive Jack Raper Award at ISSCC 2006



From left: Tim Tredwell, ISSCC Executive Chair, John Kitching and Clark T. C. Nguyen.

Clark T. C. Nguyen (DARPA, Arlington, VA and University of Michigan) and John Kitching (NIST, Boulder, CO) received the Jack Raper Award for Outstanding Technology Directions Paper at ISSCC 2006 for their ISSCC 2005 article “Towards Chip-Scale Atomic Clocks.”

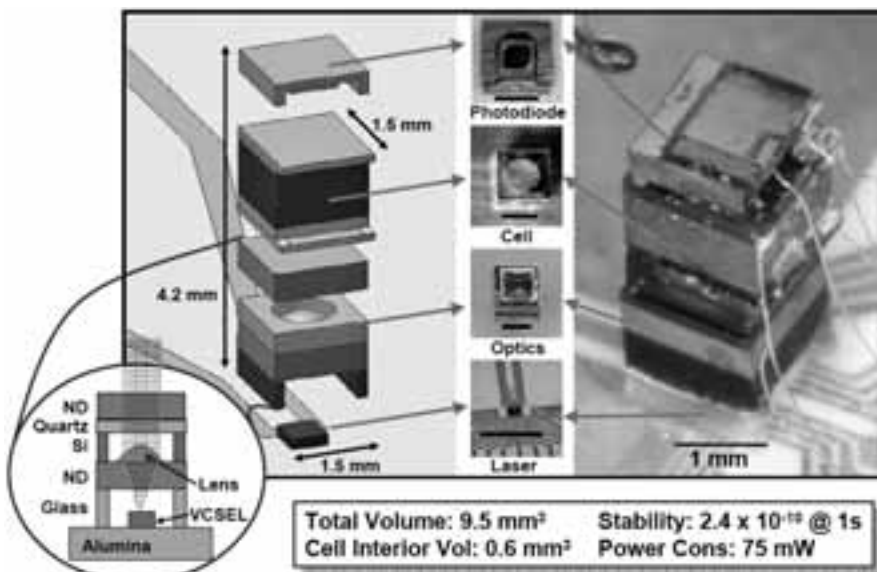
Summary: Atomic clocks have the potential to greatly enhance the timing, and ultimate performance, of many electronic systems, such as parallel A/D converters, spread-spectrum communications and GPS receivers. However, their size and power consumption have been prohibitively large for use in man-portable applications.

This paper demonstrates a miniature physics package, shown to the right, for a chip-scale atomic clock that includes a tiny micromachined cesium (Cs) atomic vapor cell, an 852nm VCSEL, a photodiode detector, polarizing and focusing optics, heater elements to maintain Cs atoms in a vapor state, and a micromechanical suspension system that thermally isolates the vapor cell/heater structure to allow elevated temperatures with low-power consumption. The system is implemented in a

MEMS-enabled size less than 10mm³, which is more than 700x smaller in volume than the smallest atomic clock physics package in production, shrinking atomic clocks from their present-day table-top sizes down to only 1 cubic centimeter. When one shrinks the atomic cell to less than 10mm³, using the MEMS technology, the amount of power needed to keep the atoms in a vapor state can be reduced to less

than 10mW in a properly designed thermal control system. In effect, the smaller the mechanical structure, the less power is needed to heat up to a given temperature. The physics package described in the paper consumes 75mW of power, which is 100x better than the present lowest power production atomic clock, but still not low enough to meet the 30mW Chip-Scale Atomic Clock (CSAC) total clock power goal (which implies a ceiling of ~10m W for the physics package alone).

The accomplishments described in this paper are a direct result of funding under the Defense Advanced Research Projects Agency’s CSAC program, which Nguyen ran for the past 3.5 years. This program specifically aims to take advantage of the enormous miniaturization and thermal isolation opportunities afforded by MEMS technology to achieve an atomic clock that occupies a volume less than 1 cubic centimeter and consumes less than 30 mW total, all while retaining an Allan deviation better than 10⁻¹¹ at one hour, which is on par with much larger existing atomic clocks. To date, approximately one year after the paper was given, an atomic clock physics package has been



MEMS technology is used for a chip-scale atomic clock with thermal isolation that uses 30 mW.

achieved that consumes only 5mW to achieve the needed Cs vapor temperature, and complete atomic clocks have been demonstrated that measure less than 10 cm³, consume less than 150 mW of total power, and attain better than 5e⁻¹¹ Allan deviation at 100 seconds. The program is now in its third phase, which is expected to culminate with devices that actually meet the goals of the CSAC program.

Interestingly, the main barrier to achieving the power goals of CSAC's atomic clocks is no longer heating of the physics package, but actually now is the equally important power drains by the electronics for the microwave oscillator and for environmental control. These are also discussed in the paper.

Prof. Clark T.-C. Nguyen received the B.S., M.S., and Ph.D. degrees from the University of California at Berkeley in 1989, 1991, and 1994, respectively, all in Electrical Engineering and Computer Sciences. In 1995, he joined the faculty of the Department of Electrical Engineering and Computer Science at the University of Michigan, Ann Arbor, to which he has very recently returned after a 3.5 year leave in Washington, DC, where he served as the MEMS Program Manager in the Microsystems Technology Office (MTO) of DARPA. His technical interests at Michigan focus upon micro electromechanical systems (MEMS) and include integrated vibrating micromechanical signal processors and sensors, merged circuit/microme-

chanical technologies, RF communication architectures, and integrated circuit design and technology. Prof. Nguyen and his students at Michigan have garnered numerous Best Paper Awards at prestigious conferences, including the 1998 and 2003 IEEE Int. Electron Devices Meetings, the 2004 IEEE Ultrasonics Symposium, the 2004 DARPA Tech Conference, the 2004 IEEE Custom Integrated Circuits Conference, the 2005 IEEE ISSCC, and the 2005 IEEE Frequency Control Symposium.

In 2001, Prof. Nguyen founded Discera, Inc., a company aimed at commercializing communication products based upon MEMS technology, with an initial focus on the vibrating micromechanical resonators pioneered by his research in past years. He served as Vice President and Acting Chief Technology Officer (CTO) of Discera from 2001 to mid-2002.

In mid-2002, Prof. Nguyen went on leave from the University of Michigan to join the Microsystems Technology Office (MTO) of DARPA in Arlington, Virginia, where he served as a Program Manager in MEMS technology. At DARPA, from mid-2002 through 2005, Prof. Nguyen created and managed a diverse set of programs that included Microelectromechanical Systems (MEMS), Micro Power Generation (MPG), Chip-Scale Atomic Clock (CSAC), MEMS Exchange (MX), Harsh Environment Robust Micromechanical Technology (HERMIT), Micro Gas Analyzers (MGA), Radio Isotope

Micropower Sources (RIMS), RF MEMS Improvement (RFMIP), Navigation-Grade Integrated Micro Gyroscopes (NGIMG), and Micro Cryogenic Coolers (MCC).

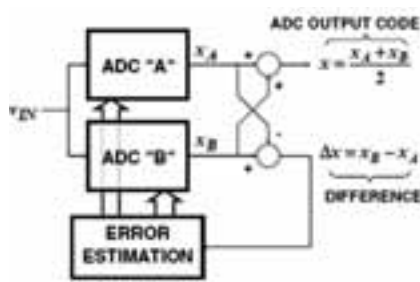
Dr. John Kitching received his BSc. in physics from McGill University in 1990. He went on to obtain a MSc. And Ph.D. in Applied Physics from the California Institute of Technology in 1992 and 1995, respectively. His thesis topic was an investigation of amplitude and frequency noise properties of semiconductor lasers subjected to optical feedback. From 1995 to 2003, he was with JILA/The University of Colorado and also held a guest-researcher appointment in the Time and Frequency Division at the National Institute of Standards and Technology, NIST. Since 2003, he has been a physicist in the Time and Frequency Division at NIST. His research interests include atomic clocks and frequency standards, quantum interference effects in atomic systems, and applications of semiconductor lasers to problems in atomic physics and frequency control. Most recently, he and his team pioneered the development of microfabricated atomic devices for use as frequency references, magnetometers and other sensors.

He has received several awards including the 2005 EFTF European Young Scientist Award and the Department of Commerce Silver Medal. He has published over 40 papers in refereed journals, has given numerous invited talks and has been awarded two patents. ●

McNeill, Coln and Larivee Receive Lewis Winner Outstanding Paper Award at ISSCC 2006

John McNeill, Worcester Polytechnic Institute, mcneill@ece.wpi.edu

John McNeill, Associate Professor of Electrical and Computer Engineering at Worcester Polytechnic Institute (WPI) and Michael Coln and Brian Larivee of Analog Devices (ADI) received the Lewis Winner Award at the 2006 ISSCC for their 2005 ISSCC paper "A split-ADC architecture for deterministic digital background calibration of a 16b 1 MS/s ADC."



Architecture uses FPGA for digital calibration algorithm for ADC.

Chip Summary

The "split-ADC" architecture enables the use of a deterministic digital calibration procedure that operates continuously in the background and requires fewer than 10,000 conversions to complete calibration. This architecture, demonstrated in a 16b, 1 MS/s algorithmic ADC, is shown in the figure to the left. The analog sub-system of the ADC was implemented in 0.25 μm CMOS, con-



From left, Tim Tredwell, ISSCC Executive Chair, Brian Larivee, Dr. Michael Coln, Dr. John McNeill.

sumes 105 mW, and has a die size of 1.2 X 1.4 mm².

Dynamics of the Project

Although this project started in the summer of 2002, McNeill's relationship with Analog Devices began a decade earlier. As a PhD student at Boston University from 1991-1994, he worked with Larry DeVito's PLL group to develop a theoretical framework for understanding jitter in ring oscillators and guiding design to meet specific noise requirements; this work was published in the *Journal of Solid-State Circuits* in 1997 (dx.doi.org/10.1109/4.585289).

When McNeill's turn for a sabbatical leave from WPI came up in the 2002-3 academic year, he contacted DeVito and asked if he knew of any good problems to work on at ADI. At the same time, Mike Coln in ADI's Precision Nyquist Converter Group was looking for a "breakthrough" in ADC design: an innovative architecture that would explicitly take advantage of CMOS scaling by relaxing requirements on analog circuitry and moving as much complexity as possible into the digital domain. Work-

ing in Coln's group at ADI, McNeill completed the top-level architecture design in the fall of 2002; circuit design and layout were completed by the fall of 2003. As McNeill returned to his teaching and research duties at WPI in 2003, Brian Larivee carried out the process of integrating the analog test chip with the FPGA implementing the digital calibration algorithm. The test and evaluation process was completed in time to submit the paper for ISSCC in September 2004.

The collaborative relationship between WPI and Analog Devices is continuing in research toward applying the split ADC concept to other types of ADCs. In addition to funding from ADI for this work, McNeill was also awarded a grant from NSF in 2005 to support further research.

John McNeill joined the ECE faculty at WPI in 1994. Since 1998, he has been director of the Center for Analog and Mixed Signal Integrated Circuit Design at WPI, (<http://ece.wpi.edu/analog/center.html>), a consortium of industry sponsors supporting undergraduate projects and graduate research in the area of analog and mixed sig-

nal integrated circuit design. In 1999 he received the WPI Trustees' Award for Outstanding Teaching. He received an A.B. from Dartmouth College in 1983, an M.S. from the University of Rochester in 1991, and a Ph.D. from Boston University in 1994. From 1983 to 1990 he worked in industry in the design of high speed, high resolution analog-to-digital converters and low noise interface electronics used in high speed, wide dynamic range imaging systems.

Mike Coln joined Analog Devices in 1988, after earning a PhD from MIT. Since then, he has been involved in design, leadership, and mentoring roles, contributing to all areas of precision data converter development within the company. A holder of 12 patents, Coln was the chief architect of ADI's PulSAR® analog-to-digital-converter (ADC) family, which overcame perceived architectural barriers then boxing-in the specifications of speed, resolution, power consumption, and size of successive-approximation converters. The PulSAR self-calibrating architecture was the first to enable 16-bit ADCs to reach throughput of 1 Msps (million samples per second), and it resulted in the first SAR ADC to reach 18-bit resolution. In 2005, Coln was named an Analog Devices Fellow, the highest level of achievement for a technical contributor at Analog Devices, Inc..

Brian Larivee has been working for Analog Devices since 2003 as a design engineer for the Precision Nyquist Converters group. He received the BSEE and MSEE degrees from the University of Michigan in May 2002 and December 2002, respectively. His development interests are in the areas of Nyquist-rate converter design and low-power analog integrated circuit design techniques. ●

JSSC CD to Change to DVD: The End of an Era

CD of JSSC, 20th Issue Will Be The Last

The annual CD containing the previous two years of the *Journal of Solid-State Circuits* articles will be issued in June 2006 and mailed to subscribers. It provides 2004 and 2005 Journal articles in pdf format. For those who didn't subscribe to the CD, a separate purchase can be entered through the IEEE Store. shop.ieee.org/ieeestore/product.aspx?p

product_no=JD3755D The member price is \$150.

The CD will be replaced by the SCS Archival DVD. Since 2001, SCS has issued a complete archival DVD, which includes all the articles of the IEEE *Journal of Solid-State Circuits* from the first issue through 2005, plus complete digests from four conferences: Three are complete from their beginnings through

2005 (ISSCC, Custom Integrated Circuits Conference and the Symposium on VLSI Circuits), while the Proceedings of European Solid-State Circuits Conference (ESSIRC) covers 1997 through 2005. All are full-text searchable with ASTAware search engine provided on the disk.

Starting in 2007, the DVD will replace the annual CD update and can be obtained beginning with the 2007

member renewal cycle. Purchasing the DVD as a subscription during renewal will result in receiving it as soon as the product is manufactured in early February.

The JSSC is the best archive of technology advances in integrated circuits,

with original research and expanded articles based on outstanding presentations from premier conferences. Once again in 2005 the Journal tops the list of most downloaded articles out of 193 technical publications in Xplore. JSSC has been readers' top choice since Xplore

began keeping download counts four years ago. 38% more JSSC articles are downloaded than the next most popular journal. More than 10 times the number of JSSC articles are downloaded than for each of 137 other transactions and magazines hosted online by IEEE. ●

ISSCC 2006 Panel on Classic Circuits

An ISSCC 2006 Evening Panel

Un-Ku Moon and K. Nagaraj, SSSC AdCom Members, moon@ece.orst.edu, nagaraj@ti.com

In a packed standing room only session, moderator Bill Redman-White opened the "Present (and Future) Classic Circuits with Less than 25 Transistors" evening panel by asking the question "what makes a real classic circuit?" While the audience quietly mulled over their own favorites and possibilities, the number 25 was quickly forgotten by the panel members.

Barrie Gilbert pulled out probably the most interesting item. He provided the silver lining by not only presenting the best circuit of the evening (below, left), but also by making it colorful and humorous with the KERMIT terminology. Who would remember what it stood for, other than it had to do with something KERMITan? We certainly enjoyed being reminded of the power of what just a few bipolar transistors can do.

Tom Lee was funny and entertaining as always and presented "the Rodney

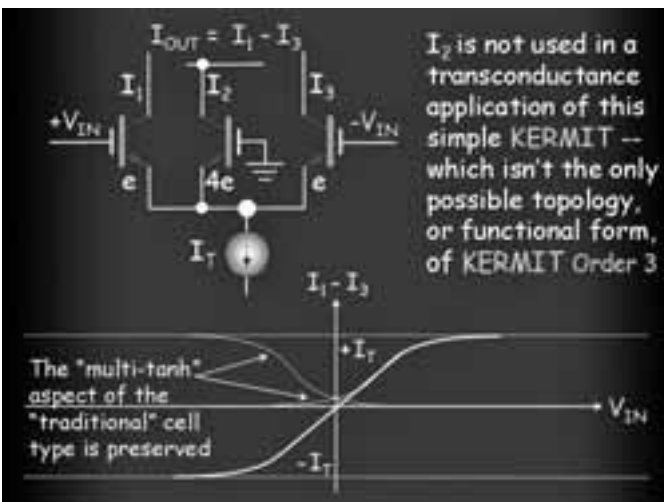
Dangerfield of circuits" (biasing: they never get any respect), which we felt was the second best circuit in the evening panel.

Other panelists presented Class AB output stage (Klaas Bult), linear V-I converter (Takahiro Miki), "infinite gain" via positive feedback stages (Bob Dobkin), and companding integrator (Yannis Tsiividis, shown below, right). We went to the panel looking for gems, and ended up a little disappointed, wondering why no one talked about something as basic and powerful as a two stage amplifier or a folded cascode amplifier.

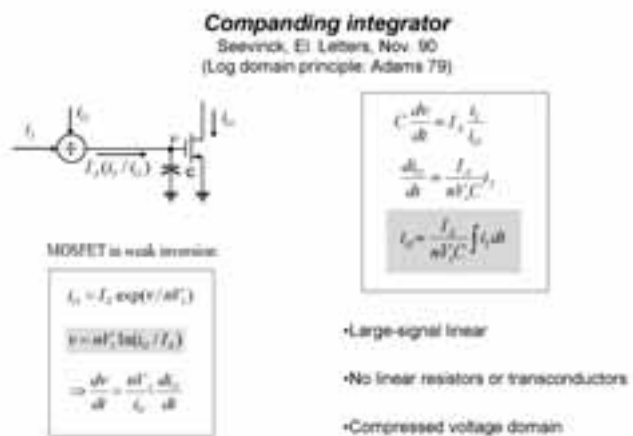
Then the evening panel kicked into a second round of what effectively ended up being a contest of "circuits with as few transistors as possible". Perhaps we should thank Scott Wurcer for launching this contest with a single JFET-resistor combination constant current source. These lighter moments of the second round are what the audience is likely to

remember and have enjoyed the most. Barrie Gilbert's talking about what one can do with just a single diode later led to Yannis Tsiividis poking fun at Barrie Gilbert's one diode circuit also needing a supply, a current source, and switches. His tongue in cheek accusation of Barrie Gilbert's one diode circuit needing a switched-capacitor signal processing system for it to work was clearly enjoyed by the audience as well as Barrie Gilbert. Yannis Tsiividis's own truly single transistor amplifier based on MOS channel parasitic RC was fun, but obviously not practical.

The element of controversy that can make for a spicy panel was missing, but the friendly competition of single-transistor circuits and routine teasing among the panel members made up for what otherwise may have been an ordinary session. The audience was entertained and will certainly remember that one application-free single transistor amplifier. ●



Best circuit of the evening, presented by Barrie Gilbert.



Companding integrator, presented by Yannis Tsiividis.

CHAPTERS

Special Chapter Events

SSCS Extra Subsidies Support Meetings in Central Texas and Taipei

SSCS chapters are eligible for extra subsidies to support events such as workshops and mini-conferences that are not financed by the annual Chapter Subsidy. In 2006, these two IC events are being supported, as well as the IEEE Siberian Section Congress to take place at the end of July:

Austin Conference on Integrated Systems & Circuits

Inaugural Meeting on 17-19 May 2006
By Mike Seningen, CTS CAS/SSC Joint Chair

Austin, the Silicon Hills of the USA, is a hotbed of electronic design, with most of the world's major companies situated in or around the immediate area. The Austin Conference on Integrated Circuits promises to bring together people with a mutual interest in presenting, learning, and debating the hot issues facing the semiconductor industry in a forum for the dissemination of technical information and the advances in electronic technology at chip, board and system levels, covering design, CAD methodology, and test. The meeting is sponsored by the UT Electrical Computer Engineering Department and the Austin Technical Council.

Jeffrey Scott, who co-founded Silicon Laboratories in August 1996 and served as Vice President of Engineering and as a Director from the company's inception to 2003, will deliver the keynote address. Mr. Scott holds a B.S. in electrical engineering from Lehigh University and an M.S. in electrical engineering from the Massachusetts Institute of Technology. Possible titles for his keynote are: "Where Will Chips be Designed in 2010" or "How is Semiconductor spelled in Chinese?"

More information may be found at the conference website: www.acisc.org.

Short Course on High-speed Link Design

By The IEEE SSCS Taipei Chapter

With the Extra Chapter Subsidy from the IEEE Solid-State Circuits Society, the Taipei Chapter successfully organized a two-day short course event in February, 2006 entitled "Efficient High-speed Link Designs: Challenges, Solutions, and Future Directions." The invited speaker was Prof. Gu-Yeon Wei of the Electrical Engineering Department, Harvard University.

The short course consisted of two one-day lectures held in Hsinchu and Taipei on February 23 and 24, respectively. This course attracted approxi-

mately 60 attendees in Hsinchu, and 50 attendees in Taipei.

Hsinchu is the epicenter of Taiwan's semiconductor industry, with many IC design companies established in the Hsinchu Science Park. As a result, professional engineers were the majority at the Hsinchu lecture. Some attendees from central Taiwan even drove more than two hours to attend the course. The audience at the Taipei lecture came from various Universities and research institutes.

Both lectures started at 10 o'clock in the morning and ended at 4:30 PM, with a lunch break at noon. After an introductory overview of the high-speed link design fundamentals, Prof. Wei went on to talk about the challenges of efficient high-speed link designs. In particular, he focused on the design methodologies of equalization and adaptation, and described several circuit and system architectures to address these design challenges. In the last part of his lecture, Prof. Wei shared his views on future research trends in high-speed link design. The engineers and students who raised questions about high-speed link design in the Q&A sessions at the end obtained insightful feedback from the speaker. This short course was well-received. Many attendees considered its content valuable to their research and work. ●



Photo taken after the lecture in National Taiwan University, Taipei. From left to right: Prof. Tsung-Hsien Lin, Prof. Gu-Yeon Wei, Prof. Shen-luan Liu (Chair of the IEEE SSCS Taipei Chapter), Prof. Hen-Wai Tsao, and Prof. Yi-Jan Chen.



Prof. Wei lecturing at National Chiao-Tung University, Hsinchu.

Rebirth of the Benelux Chapter

Chandrakasan Speaks on Design of Ultra-Low Power Systems

Jan Craninckx, Chapter Chair, jan.craninckx@imec.be

On March 24th, the SSCS Benelux chapter invited Prof. Anantha Chandrakasan to speak about the ultra-low power systems work by his group in the Microsystems Technology Lab at the Massachusetts Institute of Technology. His talk covered a lot of exciting results obtained with sub-threshold operation of digital circuits that dramatically reduce the power dissipation of digital integrated circuits. Also, system-level techniques for power reduction with fine-grain power gating and ultra-dynamic voltage scaling were shown, as well as a 3-D integration technique for FPGAs that increases the connection density and hence its power.

Abstract:

Energy efficiency is a key design consideration in wireless systems. Energy efficient system design requires systematic optimization at all levels of the design abstraction ranging from process technology and logic design to architectures, algorithms and networking. The energy expended per operation continues to improve as the power supply voltages are scaled. Sub-threshold circuit design provides a major opportunity to dramatically reduce the power dissipation of digital integrated cir-

uits. The opportunities and challenges associated with sub-threshold design will be presented. Idle-mode power (i.e., leakage) must also be carefully managed in sub-90nm CMOS and will require the use of techniques such as fine-grain power gating and ultra-dynamic voltage scaling. 3-D integration also presents an interesting opportunity for power savings - the potential power savings of this technology will be presented for a 3-D FPGA circuit. Specific examples of power management in integrated circuits will be presented, focusing on wireless sensor networks and impulse based ultra-wideband communications as drivers.

Prof. Chandrakasan is an SSCS Distinguished Lecturer. His biography may be found in the SSCS News of March 2006 www.ieee.org/portal/pages/sscs/06Mar/DL_Program.html.

This event was the first held by the new chapter chair, Jan Craninckx (IMEC, Belgium). "I want to thank the previous chair, Raf Roovers (Philips, the Netherlands), for the work he has done in the past, and we appreciate the fact that he will stay active in the future to help us revitalize the chapter. The Benelux area has always been very successful in solid-state circuits. There are

very good universities (KU Leuven, TU Delft, TU Eindhoven, TU Twente, etc.) that provide an excellent education for new electrical engineers and obtain very high quality research results from their PhD students, which are presented every year at all major conferences (ISSCC, ESSCIRC, CICC, etc.). The inter-university research institute IMEC, with its new 300mm fab, is a world-class technology research organization with major achievements in advanced digital and analog design. Amongst the large number of companies present in the area, AMI Semiconductor in Belgium and of course Philips in the Netherlands are the best known."

Invitation to Volunteer

Since so many excellent engineers work in Benelux, the SSCS Benelux chapter looks forward to becoming a vibrant forum where people meet each other and exchange ideas. Having volunteers on the team from a broad background, including Belgium and the Netherlands, industry and academics, will allow us to achieve this goal. The chapter extends an invitation to all who would like to help. People interested can contact me at "Craninckx Jan" jan.craninckx@imec.be ●



Dr. Chandrakasan addressing the SSCS Benelux chapter on 24 March, 2006.



From left, Hugo Deman (KUL/IMEC), Prof. Chandrakasan, Jan Craninckx

CONFERENCES

2006 Symposium on VLSI Circuits to Emphasize Seven Design Areas

Meeting in Hawaii on 15-17 June Will Overlap the VLSI Technology Symposium

The 2006 Symposium on VLSI Circuits, meeting on 15-17 June, 2006 at the Hilton Hawaiian Village in Honolulu, Hawaii and the VLSI Technology Symposium, at the same hotel on 13-15 June, enable technologists and circuit and system designers from around the world to interact and exchange ideas. The close affiliation of these two conferences, a tradition since 1987, gives attendees "a unique opportunity to span the entire VLSI discipline," says Bruce Gieseke, 2006 Symposium Chair. "The Symposium is full of rich and exciting papers."

After two full-day tutorial courses on 14 June, this year's Circuits Symposium program will focus on seven topic areas:

Wireless Communication

Five sessions on RF integrated circuits for wireless communications will include Cellular, WLAN, UWB, Satellite/Mobile Broadcasting and Radar applications. The presentations will cover a broad range of wireless system chip and building block designs, ranging in operation frequency from 400 to 800 MHz in the case of a DVB-H tuner all the way to 182GHz in the case of a millimeter wave Schottky diode detector. Circuit design techniques using both low-voltage standard CMOS technologies and high performance SiGe BiCMOS technologies will be discussed.

Opportunities and challenges for RF integrated circuit designs continue to arise as new technologies and wireless standards emerge. Sharp Corporation will present a direct conversion DVB-H Tuner operating from 400 to 800 MHz, with 184mW power consumption, realized in a 0.5 μ m SiGe BiCMOS technology. The IC includes a distortion compensated variable-gain low-noise amplifier and an offset cancellation loop for the base-band section. Several contributions explore the realization of millime-

ter wave integrated circuits in CMOS technology. Researchers from the University of Florida will present a 24GHz transmitter with on-chip antenna and a 182GHz Schottky diode detector. A team from National Taiwan University will discuss a 40GHz voltage-controlled oscillator and a 50GHz distributed amplifier. The University of California at Los Angeles will contribute a 60GHz CMOS receiver.

In addition to the emerging applications, advances continue for cellular, WLAN, UWB connectivity and for RF building blocks. Columbia University will present a 0.5V 900MHz CMOS receiver that demonstrates the critical RF front-end blocks operating from an ultra-low supply voltage. The University of California at Berkeley will discuss an EDGE RF transmitter using Cartesian feedback implemented in CMOS which overcomes some of the obstacles towards a true single chip phone realization. Intel Corporation will present a multi-band discrete-time receiver implemented in a 90nm digital CMOS process. The UWB session includes both MB-OFDM and pulse-based RF transceiver designs. Finally, recent advances in oscillator and divider designs will also be presented at the symposium.

Data Converters and Analog Techniques

The ever-increasing importance of data converters is reflected by this year's Symposium program, which will start with a data converter short course and a plenary talk on the future roles of data converters, followed by four sessions in the areas of Nyquist ADCs, over-sampled ADCs, and data converter techniques for embedded systems.

A 500MS/s 5b ADC is one of the first ADCs in 65nm to be presented by researchers from MIT, which describes a

technique to reduce switching energy for embedded UWB systems. Also the trend continues towards wide bandwidth in over-sampled ADCs. There will be a full session on delta sigma ADCs where Hughes Research Labs will present a 1.4GHz IF band-pass modulator at a 4GHz sample rate.

1V (and below) analog design continues to be an area of active interest and significant advancement in recent years. An example of such work will be presented by Columbia University featuring a 0.5V track-and-hold circuit achieving 60dB SNDR. On the ADC front, researchers from Shizuoka University will present 1V 10-b 100MS/s ADC with only 30mW power. The ADC features a low-power class-AB amplifier to achieve low steady-state current implemented in 90nm CMOS.

Other analog program includes paper sessions on image sensors and real-world interfaces. CMOS image sensors will have a dedicated session this year where Micron will present the world's largest single die CMOS image sensor yielding 4Kx4K pixels of 16 million pixels.

Multi-Gbps Interfaces

The demand for increased bandwidth has resulted in the development of high speed interfaces capable of driving data across long cables and channels as well as short-haul links for memory-CPU communication in computers. Four technical sessions address issues ranging from clock generation techniques to equalization circuit design approaches and channel effects.

As the drive to higher data rates continues, equalization techniques are becoming prevalent to combat channel loss and inter-symbol interference at high frequencies. UCLA and IBM show a low power (5 mW at 6 Gbps) receiver for short-haul applications. A soft decision feedback equalization technique is

used instead of the conventional hard-decision (data slicer based on edge-triggered flip-flop) architecture to relax the critical path, thus saving power.

Researchers from National Taiwan University present a 38.5GHz clock generator that enables high speed transceiver design. RMS jitter of 0.24ps at 38GHz is achieved with 52 mW power consumption.

Performance and power of 1.6 to 9.6 Gbps server, desktop, and mobile I/O lines in a 1.2 V 90nm CMOS process is analyzed in a paper by Intel. They show that a novel combination of voltage-mode driver (equalized or un-equalized) and RX equalizer delivers the lowest power (12.1mW/Gbps at 7.2Gbps), offering a low power option for short distance links.

Digital Circuit Techniques

As logic technology is moving towards 65 nm and below, on-die variations in the electrical characteristics of transistors and interconnect are presenting difficult challenges to circuit designers.

This year's contributions in the area of digital circuits focus on

- in-situ die monitoring for process and supply and process variations, and
- power and leakage management techniques applied to a range of entertainment, multimedia and communications processors.

An in-situ measurement scheme for mapping supply-noise is described which measures 69 mV local supply noise with 5 ns time resolution in a 3G cellular phone processor from Hitachi.

Many papers describe the use of parallel processors for attaining high computational throughput. The circuits and design methodology of the massively parallel processor from Renesas is based on a matrix architecture, which enhances

the performance of multiply-accumulate operations up to 30 GOPS/W.

A paper from Keio University demonstrates low system power from application specific architecture optimization. By using a hardware accelerator coupled with a programmable processor core, a real-time face detection core is achieved in 0.79mm² Si using 0.13um CMOS technology. It can detect 8 faces per frame at 30 fps, while consuming merely 29mW at 1.2 V supply voltage.

SRAM for Ultra-deep submicron technologies

Nine papers on next generation SRAMs from industry and academia will address critical issues related to SRAM cell stability and architectural features at 65 nm and beyond.

Two key papers are from IBM and Intel. The IBM paper describes a 32Mb SRAM designed for 65 and 45 nm technologies. It features read-and-write-assist circuit techniques that expand the operating voltage range and improve manufacturability across technology platforms. Intel's paper describes a 16-way set associated, single-port 16MB cache for the dual-core Xeon processor using a 0.624 um² cell in a 65 nm 8-metal layer technology. Sleep transistors are used in the SRAM array. Techniques to protect the cache from latent defects and infant mortality failures will be discussed.

Non-Volatile Memory Architecture and Circuits

This year's non-volatile memory session will cover two new flash memory architectures as well as two new emerging technologies, including a 500 MHz SOC MRAM by NEC Corporation and a new CBRAM by Infineon Corporation. What is a CBRAM? Come to the VLSI Sympo-

sium memory session and learn about this new technology, as well other papers. To further scale the NOR flash array, Sharp Corporation will discuss its new contactless virtual ground array architecture with an interesting 32 cell stack string.

Spansion will provide details about their 1.8V 90nm 1Gb OrNAND flash memory solution to the growing removable and embedded data market. This paper discusses their product and memory architecture that was squeezed into 81 mm². Their paper will also discuss how this 2 bit/cell MirrorBit memory is able to achieve near regular NAND write rates of 3 to 11 MB/S.

Who says non-volatile memories are slow? NEC Corporation will present their MRAM of capable of 500MHz and higher on a 130nm CMOS/240nm MRAM SOC process. They will introduce two new MRAM cell architectures able to achieved this very high speed performance as well as lower write current.

Evolving DRAM technologies

For SOC (System-On-a-Chip) applications, minimum operational voltage is becoming very critical for DRAM's. All four DRAM papers will report new circuit techniques and technologies to meet low operating voltage requirements.

Renesas will report a high performance TwinCell RAM technology in SOI process at 90nm.

Toshiba will report the first ever 6F² 128 Mb single transistor gain cell-based high density RAM in SOI, which provides a bit yield of 99% and reduced power.

IBM will report a 3T DRAM cell with a gated diode for enhanced speed and data retention time.

Further information can be found on the Symposium web site: www.vlsisymposium.org/index.html. •

RFIC Symposium to Launch Microwave Week, 11-13 June, 2006

Luciano Boggione, RFIC 2006 TPC Co-Chair, l.boggione@ieee.org

The RFIC (Radio Frequency Integrated Circuits) Symposium is renowned as the foremost IEEE technical conference dedicated to the lat-

est innovations in RFIC development of wireless and wire line communication ICs. It is co-sponsored by SSCS.

This year's RFIC Symposium, on 11-



13 June at the Moscone Convention Center in San Francisco, will launch Microwave Week 2006, the largest world-wide RF/Microwave enclave of the

year. The IEEE MTT-S International Microwave Symposium (IMS) will coincide with RFIC, from 11-16 June, along with the 67th Automatic RF Techniques Group (ARFTG) Conference, whose specialty is measurements, on 16 June. More than 1000 papers will be presented in all.

Plenary Session on Wireless and Mobile Communications ICs and Systems

A plenary session on Sunday evening will kick off the formal technical program. This year, three distinguished speakers will share their views on the future of wireless and mobile communications ICs and systems: Mr. Stefan Wolff, Vice President RF-Engines at Infineon Technologies, Mr. Kent Heath, Director, Cellular Operations, Radio Products Division, at Freescale Semiconductor, and Dr. Arogyaswami Paulraj, Founder and Chief Technology Officer at Beceem Communications and Professor, Stanford University.

Plenary 1: "RF-Modems the Real Application for RF CMOS"



Stefan Wolff

As Vice President of Infineon Technologies, Stefan Wolff oversees the company's Cellular RF Engine business unit and has been involved in its RFIC business since the early nineties. After beginning his career at the Robert Bosch group as a RF engineer for Mobile Phones, he joined Siemens Semiconductor, where he was responsible for the marketing of RF ICs. Prior to joining Infineon, Mr. Wolff headed the San Diego RF design centre of Siemens Mobile Phones.

Abstract: Over the last decade, wireless connectivity has become an integral and essential part of our lives. The plain mobile phone of the early nineties has evolved into the mobile multimedia terminal as consumers demand cell phones that provide a comprehensive set of advanced features enabling voice, data and video services. Handset manufacturers have to accommodate their products to fast-changing market requirements. The semiconductor supplier has to provide a cost effective and flexible platform that enables handset manufacturers to differentiate their products quickly

while maintaining a low-cost development effort.

The vast majority of today's cell phones require at least a multiband radio. In the near future, multimode multiband 2G and 3G operation will be a part of main stream products including wireless LAN, Bluetooth®, GPS and DVB-H as well. Infineon Technologies has focused its RF expertise on providing the next wave of highly integrated, high performance and easy to use RF CMOS radio subsystems. Infineon Technologies demonstrates the maturity of RF CMOS with respect to RF performance by producing e.g. a six-band WCDMA / UMTS transceiver; the RF CMOS capability enabled the world's first single chip cell phone: EGold-Radio. RF-modems will be the next leap in integration. These RF-SoCs will simplify the handset development process by separating radio hardware and the protocol stack from the application layer.

Plenary 2: "Architectural Implications of Multimode, Multiband Cellular Radios"



Kent Heath

Kent Heath joined Freescale Semiconductor in March, 2004 as director of the Analog Cellular IC business unit, where he is responsible for power management and user interface ICs, RF transceivers, power amplifiers, RF subsystems and DVB-H components targeted for the cellular handset market. Prior to joining Freescale, he was senior director of strategy and business development for the RF Solutions Division at Skyworks Semiconductor. From 1997-2000, he was director of Motorola Semiconductor's Wireless Subscriber Systems Group (WSSG, Japan) after previous engineering management positions at Xerox, Genisco Technology, and LectroMagnetics Inc. Mr. Heath is a BSEE and MBA graduate of Southern Methodist University in Dallas. He belongs to the Semiconductor Industry Association in Japan (SIAJ) and the Society of Mechanical Engineers (SME), and has been an active member of the IEEE for over 20 years.

Abstract: This talk explains how combinations of System-on-Chip(SoC)-

and System-in-Package(SiP)-level integration may be employed to meet the accelerating cost and size reduction needs of OEMs and carriers. These technologies exemplify trends toward high levels of integration and multiple radio technologies in a single RF lineup.

Solutions to the challenge of integrating multiple radio technologies in a single RF chip range from elaborate III-V technologies to SiGe-based methodologies, BiCMOS nodes and RFCMOS-based solutions. Some of these technologies are single-chip solutions, while others are combinational approaches using various platforms for SiP-level integration. This talk addresses the various approaches available and the potential implications to the mobile communications industry.

Plenary 3: "Multiple Antenna Technology in Mobile Broadband - New Challenges for RF Designers"



Dr. Arogyaswami Paulraj

Dr. Arogyaswami Paulraj supervises the Stanford University Smart Antennas Research Group, working on applications

of space-time wireless communications. The many key fundamentals he has developed have drawn research attention to this new field. Dr. Paulraj has won several awards for his engineering and research contributions, most recently the IEEE SP Society Technical Achievement Award 2003. He is the author of over 300 research papers and a textbook on wireless communications. He also holds 24 patents. Dr. Paulraj is a Fellow of the IEEE and a Member of the Indian National Academy of Engineering.

Abstract: Multiple antenna wireless has emerged as a key technology that significantly improves coverage and throughput. Multiple input - multiple output (MIMO) is a configuration that uses multiple antennas at both ends of the link. This talk on MIMO in mobile broadband begins with a survey of mobile broadband applications, markets and standards with special reference to multiple antenna technology. It describes the typical design of a next generation mobile broadband system that uses MIMO-OFDMA and highlight design

areas that are impacted by MIMO and quantifies the performance enhancement offered by multiple antennas in mobile broadband. Finally, it describes the RF design challenges related to multiple antennas at both terminals and base stations, and addresses mutual coupling and its impact on RF performance, transmit-receive RF calibration necessary for the transmitter to learn the channel, RF power drain and power management achieved by controlling the number of active RF chains, and PAPR reduction. A survey of emerging multiple antenna RF products concludes the talk.

Sunday Evening Reception

The RFIC reception begins immediately after the plenary, making Sunday evening a highlight of both technical

activities and social festivities. This highly attended, enjoyable social event allows attendees to meet with old friends, discuss the latest events in the RFIC field and interact with professionals in the wireless community.

Technical Program

The RFIC technical program starts on Sunday with tutorials and workshops focused on RF technology, design and systems, and continues on Monday and Tuesday with paper presentations, panel sessions and an interactive forum.

The panel sessions at lunch time are always captivating. On Monday, one distinguished group of panelists will discuss the subject "4G: Do We Really Need 1 Gbits/s?" and another distinguished set of panelists will debate "SoC vs. SiP:

Dollars & Sense" on Tuesday.

The interactive forum on Tuesday afternoon is an excellent opportunity for attendees to meet authors face to face to discuss their presentations in detail.

If you are not sure about investing time and money to attend the RFIC, ask any professional or academic: They will confirm to you that this is the conference to attend in the area of RF integrated circuits. See you in San Francisco, June 11th, 2006!

For more information, see the RFIC website, www.rfic2006.org, the IEEE MTT-S International Microwave Symposium (IMS) website www.ims2006.org/ims2006_tech-program.htm, and the 67th Automatic RF Techniques Group (ARFTG) Conference website, (www.arftg.org/#Upcoming%20Events). •

DAC Receives Record 1,007 Submissions

43rd Conference to Meet in San Francisco, 24-28 July 2006

The Design Automation Conference received 864 technical paper proposals, 13 tutorial proposals, 78 panel submissions and 52 student contest designs for its 43rd annual meeting at the Moscone Center in San Francisco, according to a press release this January. DAC is the premier forum for the electronics industry's "hottest trends," it said, with attendance regularly exceeding 10,000 developers, designers, researchers, managers and engineers from leading electronics companies and universities around the world.

"Hot Areas" are System-Level Design, DFM and Power

System-level design, Design-for-Manufacturability (DFM), and power are the "hot areas" in this year's submission pool, said Ellen Sentovich, DAC General Chair, due to the fact that consumer electronics and computer applications continue to drive the industry, along with "still-increasing time-to-market pressures that imply the need for advances in designing faster, denser chips, for reducing power consumption, and for taping out quickly."



System-Level Progress

Discussions about the best tools that allow designers to work at a level above RTL will speak to questions about

- resolving language/standards controversies
- unifying disparate, often complementary approaches
- emergence of a global vision.

DFM

Papers on integrated flows and enablers that bridge the gap between design and manufacture for the cost-effective continuation of Moore's Law beyond the 65 nm. node will point to collaboration among the electronic

design automation (EDA) and semiconductor industries and suppliers.

Power Challenges

The increasing use of dynamic analysis and tools for tackling all levels of design, from voltage blocks at the architectural level to leakage control for high-speed parts, will be important developments to watch at the conference.

Beyond the Die Integration Packaging

"In the last few years," said Grant Martin and Sachin Sapatnekar, co-chairs of this year's TPC, "we have seen a growing need for advanced design technologies to solve problems at the package, hybrid, board, and whole-system levels" and "a growing response" to this need with "new tools and methods, including co-design approaches between all levels of design integration." As a result, the DAC program will include "beyond-the-die" integration packaging -- chip-package co-design, system-in-package (SIP), new integration techniques, such as 3D and stacked designs, and everything in the design area that goes beyond the die-design, simulation, physical layout, and analysis and optimization at the package, hybrid board, backplane, rack and whole-system levels.

Theme Day to Focus on Entertainment, Games and Multimedia

Wednesday's program on 26 July will address "the growing convergence of entertainments platforms for gaming and the digital home, the continued role of graphics processors as key EDA industry drivers and San Francisco's hotbed of software and content development," said Ms. Sentovich.

Start-Up Exhibitors

Start-up companies will represent new developments in analog, verification, system-level IC design, and DFM.

Annual Student Design Contest

Jointly sponsored by the Design Automation Conference (DAC) and the International Solid State Circuits Conference (ISSCC), the prestigious DAC Student Design Contest has been co-chaired for several years by Bill Bowhill, Senior Principal Engineer, Intel Massachusetts, and Alan Mantooth, Professor of Electrical Engineering at the University of Arkansas. The total prize money this year is expected to be close to \$15,000, shared between the first, second and third place winners. They will receive travel assistance to attend the meeting, where their winning submissions will be displayed as posters at the DAC Univer-

sity Booth on the exhibit floor. They will also have the opportunity to present their work at a special poster session at ISSCC 2007. "The DAC/ISSCC Student Design Contest is unique in the industry for the opportunities it offers to its winners and sponsors," said Mantooth. "The contest provides competition between graduate and undergraduate students at universities and colleges worldwide, while also giving them a chance to demonstrate their experience to sponsor company representatives who serve as judges."

More information about DAC 2006 may be found at the conference website: www.dac.com. •

SSCS Sponsors 2nd Annual Organic Microelectronics Workshop

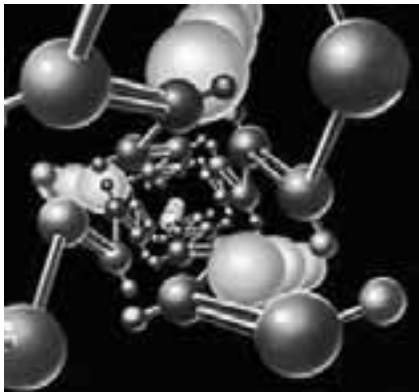
23 Invited Papers Focus on TFT Circuits and Printing, Photovoltaics and OLED/TFT for Displays

Ed Chandross (eachandross@bell-labs.com), Ananth Dodabalapur (ananth@mer.utexas.edu) & Shelby Nelson (shelby.nelson@kodak.com), Technical Chairs

The second annual Organic Microelectronics Workshop will take place in downtown Toronto on 9-12 July, 2006. It is an unusual interdisciplinary conference, established by the American Chemical Society (ACS), the IEEE Components Packaging and Manufacturing Technology Society (CPMT) and the Materials Research Society to bring the communities into lively discussion across boundaries. Invited speakers are from around the globe, and represent both industrial and academic communities, with heavy representation from companies trying to develop commercially attractive devices.

Organic microelectronics, a topic of great interest for over a decade, comprises both fundamental properties and applications for technology. The Workshop emphasizes applications for technology. This year's papers will span theoretical, materials, interface analysis, device fabrication, and commercialization issues.

The five-session technical program will focus on organic transistors, LEDs, and photovoltaics. Posters will be presented after the Monday and Tuesday afternoon sessions.



TFT Circuits	Monday, 10 July, a.m.
TFT – Printing	Monday, 10 July, p.m.
Materials	Tuesday, 11 July, a.m.
Photovoltaics	Tuesday, 11 July, p.m.
OLED/TFT for Displays	Wednesday, 12 July, a.m. and p.m.

TFT Circuits and Printing

Two of the sessions making up a full day are devoted to thin film transistor circuits and printing. Applications here include backplanes for displays that may be based on electrophoretic or liquid crystal technology. Organic based RFIDs are an attractive possibility. RFID technology is becoming

widespread and many are interested in low cost "chips" that can be cheaply printed on various packaging materials.

Materials

The development of new materials is a critical aspect. Included are both small molecule materials and various polymers. The latter may be useful for their semiconductor properties or as emissive materials in organic light emitting displays (OLEDs). Displays are covered for both aspects in addition to the discussion of materials.

Photovoltaics

Low cost photovoltaics are under investigation, especially for portable electronics via solution deposition processes and they are discussed in one session.

Finally, a few talks are intended to raise "real world" issues, and perhaps stir controversy, by addressing competing technologies. Ample time is set aside for discussion and posters are invited. There are no evening sessions so that attendees can enjoy the attractions of Toronto.

More information may be found at the Workshop website: www.organicmicroelectronics.org. •

2006 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM) in Maastricht, the Netherlands, 8-10 October

Nobel Prize Winner Dr. Zhores Alferov to Deliver Keynote Address

John Long, BCTM General Chair, j.r.@ewi.tudelft.nl

You want to be at the IEEE Bipolar/BiCMOS Circuits and Technology Meeting 2006 (BCTM) if you're interested in leading edge processes, devices, and circuits used in state-of-the-art telecom and power control systems. Bipolar/BiCMOS technologies, particularly SiGe HBT BiCMOS, play a key role in these systems.

We are extremely fortunate this year to have the 2000 Nobel Prize winner in Physics, Dr. Zhores Alferov (photo, left) as our keynote speaker. Dr. Alferov received the Nobel prize for "Developing Semiconductor Heterostructures Used In



High-Speed And Optoelectronics." Don't miss this opportunity to hear Dr. Zhores describe his historic contribution to semiconductor devices and technology in the keynote address.

The conference begins with a short course on Sunday, October 8, followed by two full days of contributed and invited papers. Exhibitors offering key technologies relevant to the BCTM community will be present for the entire conference. The annual Workshop on Compact Device Modeling for RF/Microwave Applications organized by TU-Delft follows the conference on Wednesday.

The 2006 BCTM short course is dedicated to on-chip Passive Component technologies and features three renowned experts.

Achim Burghartz from IMS Stuttgart will present an overview of RF passives on silicon.

G.P. Li from UC Irvine will address MEMS for wireless and biomedical applications.

Yuri Tretiakov from RFMD will present passive device design, modeling and measurement (including packaging effects).

The invited papers include a full morning session on Emerging Technologies, featuring the latest in new and speculative devices and materials.

See you in Maastricht this Fall! ●

SSCS Digital Archive DVD Set



This archive, on a pair of DVDs, includes all the articles of the *IEEE Journal of Solid-State Circuits* from the first issue through 2005 in pdf, plus four conferences:

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- VLSI Symposium on circuits 1988 to 2005
- CICC Custom Integrated Circuits Conference 1988 to 2005
- ESSCIRC European Solid-State Circuits Conference 1997 to 2005

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SSCS SPONSORED MEETINGS

2006 Symposium on VLSI Circuits

www.vlssymposium.org

15–17 June, 2006

Honolulu, Hawaii

Paper deadline: passed

Contact: Phyllis Mahoney, vlss@vlssymposium.org

or Business Center for Academic Societies, Japan, vlssymp@bcasj.or.jp

2006 (CICC) Custom Integrated Circuits Conference

www.ieee-cicc.org

10–13 September, 2006

San Jose, CA, USA

Paper deadline: passed

Contact: Melissa Widerkehr, cicc@bis.com

2006 (A-SSCC) Asia Solid-State Circuits Conference

www.a-sscc.org

13–15 November, 2006

Hangzhou, Zhejiang Province, China

Paper deadline: 5 June 2006

Contact: zbibua@tsinghua.edu.cn

2007 (ISSCC) International Solid-State Circuits Conference

www.isscc.org

11–15 February, 2006

San Francisco Marriott Hotel,

San Francisco, CA, USA

Paper deadline: 15 September 2006

Contact: Courtesy Associates, ISSCC@courtesyassoc.com

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2006 Radio Frequency Integrated Circuits Symposium

www.rfic2006.org

11–13 June, 2006

San Francisco, CA, USA

Paper deadline: passed

2006 Symposium on VLSI Technology

www.vlssymposium.org

13–15 June, 2006

Honolulu, Hawaii

Paper deadline: passed

2006 Design Automation Conference

www.dac.com

24–28 July, 2006

San Francisco, CA, USA

Paper deadline: passed

2006 European Solid-State Circuits Conference

www.esscirc2006.org/

18–22 September, 2006

Montreux, Switzerland

Paper deadline: passed

2006 International Symposium on Low-Power Electronic Devices

www.islped.org

4–6 October, 2006

Tegernsee, Germany

Paper deadline: passed

2006 Bipolar/BiCMOS Circuits and Technology Meeting

www.ieee-bctm.org

9–10 October, 2006

Maastricht, Netherlands

Paper deadline: passed

2006 International Conference on Computer Aided Design

www.iccad.com/future.html

5–9 November, 2006

San Jose, CA, USA

Paper deadline: passed

2006 Compound Semiconductor IC Conference

www.csics.org/

12–15 November, 2006

San Antonio TX

Paper deadline: 15 May 2006

2007 International Conference on VLSI Design

www.vlsiconference.com/

3–7 January, 2007

Bangalore, India

Paper deadline: TBD

2007 Design, Automation and Test in Europe

www.date-conference.com/conference/next.htm

16–20 April, 2007

Acropolis, Nice, France

Paper deadline: TBD

IEEE SOLID-STATE CIRCUITS SOCIETY NEWSLETTER is published three times per year, January, May, and September by the Solid-State Circuits Society of The Institute of Electrical and Electronics Engineers, Inc. Headquarters: 3 Park Avenue, 17th Floor, New York, NY 10016-5997. \$1 per member per year (included in society fee) for each member of the Solid-State Circuits Society. This newsletter is printed in the U.S.A. **Postmaster:** Send address changes to IEEE Solid-State Circuits Society Newsletter, IEEE, 445 Hoes Lane, Piscataway, NJ 08854. ©2006 IEEE. Permission to copy without fee all or part of any material without a copyright notice is granted provided that the copies are not made or distributed for direct commercial advantage and the title of publication and its date appear on each copy. To copy material with a copyright notice requires specific permission. Please direct all inquiries or requests to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. Tel: +1 732 562 3966.

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