CICC Celebrates 25 Years of Innovation, Education, and Communication

The Custom Integrated Circuits Conference (CICC), a premier conference for information on leading-edge analog and digital circuits, celebrates its 25th year, 21–24 September in San Jose, California. CICC is dedicated to IC development, showcasing original first-published technical work and innovative circuit techniques tackling practical problems.

CICC has evolved with the industry to cover a broad spectrum of technical topics and offers attendees a total educational experience including paper presentations, exhibits, panels, tutorials, and interesting networking events. This year the program consists of in-depth educational sessions, advanced technical sessions (including new sessions on emerging technology), panel discussions, technical/commercial exhibits, exhibitor preview sessions, and networking opportunities.

Bob Lucky Leads Off the Technical Program

CICC is very proud to announce the keynote speaker for 2003, Dr. Robert W. Lucky, author of the bimonthly “Reflections” column in IEEE Spectrum magazine. Dr. Lucky, an IEEE Fellow, is well known for his groundbreaking work in adaptive equalization at AT&T Bell Labs. He has served as the Executive Director of the Communication Sciences Research Division at Bell Labs and as Chair of the Scientific Advisory Board.

50 Years of ISSCC History

Back in 1954, the organizers of what would become the International Solid-State Circuits Conference did not know they were founding an international conference, or even an annual event. The only international presence at the first conference consisted of one attendee each from Canada and Japan. That perspective changed rapidly over the first few years. The first overseas papers appeared in 1958. In 1960, after experimenting with almost-yearly title changes, the organizers settled on the present “International” title of the conference.

Gordon Moore informed attendees of the 50th Anniversary ISSCC that “No Exponent is Forever,” reminding IC designers of the challenges ahead. The Plenary Session filled the San Francisco Ballroom in February 2003. See page 5 for a look at an overflow crowd from 1960 and more details about the history of ISSCC.

Continued on page 2

Continued on page 4
for the United States Air Force. Dr. Lucky also has received numerous honorary doctorates and industry awards, including the Marconi Award for his contribution to data communications. Dr. Lucky’s discussion of technology in the midst of telecom turmoil will provide a lively opening to the CICC technical program, Monday, 22 September.

Lunch Talk on Robots
During lunch on Tuesday, 23 September, Dr. Tsugio Makimoto of Sony Corporation will present a historical review of robots, highlighting the critical role played by chip technology. Dr. Makimoto also will share the story of Sony’s entertainment robots, including a dog-like robot, AIBO, and a biped humanoid robot. This promises to be a fascinating and educational experience.

Panel Discussions
Three spirited panel discussions on Tuesday, 23 September, will feature experts sure to offer strong opinions on the following topics:

Outsourcing! From Fabrication to Packaging, and Now Design—Will the U.S. Semiconductor Industry Survive Overseas Outsourcing?
The semiconductor industry witnessed a dramatic rise in the number of fabless companies in the 1990s. Company business models were based on access to IC manufacturing processes at foundries such as TSMC and Chartered Semiconductor, and on access to assembly plants in South-East Asia. As the cost of building fabs became an ever-increasing percentage of corporate revenues, even traditional IC companies started to outsource part of their manufacturing and assembly to the same foundries. This trend shows no sign of slowing down as both assembly and even design are being outsourced to overseas companies. Panelists will discuss these trends and the serious consequences for the future of the IC industry in the U.S.

Panelists:
Ed Ross, President, TSMC, USA
Jim Clifford, Senior Vice President, Qualcomm
Representative from WiPro
Brian Fitzgerald, CEO, ChipWrights
AnnLee Saxenian, U.C. Berkeley
Representative from Motorola

Are Analog Device Models Really That Bad or Are They Just a Convenient Excuse?
The poor accuracy of transistor models is a constant complaint of circuit designers. Why has research to improve transistor model equations done little to alleviate these complaints? Is the pace of technology change too fast for stable models to emerge? Is it the nature of our industry to constantly push past the limit so that this problem will never go away? Or, are the models just an easy excuse for missed deadlines and product specs?

Panelists:
Pieter Vorenkamp, Broadcom
Yannis Tsividis, Columbia University
Dan Foty, Gilgamesh Associates
Colin McAndrew, Motorola
Ali Niknejad, Co-director BSIM Project, U.C. Berkeley
Yu-Tai Chia, Department Manager of Spice Modeling, TSCM
Weidong Liu, President, TSMC, USA

Convenient Excuse?

The introduction of 130-nm technology was anything but “seamless.” Furthermore, the technology delivers less performance than expected and the future doesn’t look promising. For example, performance benefits of the next process generation are questionable. Leakage power, ignored by

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For detailed contact information, see the Society Web page: www.scs.org

For questions regarding Society business, contact the SSCS Executive Office.

Contributions for the October 2003 issue of the newsletter must be received by 1 August 2003 at the SSCS Executive Office.

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designers for so long, will limit future designs. Adding to the pain are exploding mask costs. What can product developers expect from technology suppliers in the future to satisfy consumers’ needs?

Panelists:
Dan Lenoski, Vice President Engineering, Cisco Systems

Erich Goetting, Vice President, Advanced Product Group, Xilinx, Inc.
Jack Sun, Senior Director, Logic Technology R&D, TSMC
Simon Yang, Vice President, Logic Technology Development and Manufacturing, SMIC
Scott Crowder, Foundry Technology Development, IBM Microelectronics

**CICC Educational Sessions—Sunday, 21 September**

The conference starts with three full-day educational sessions on Sunday, 21 September. These sessions are taught by practicing experts who work at the leading edge of their fields. The topics for these sessions are:

- **Advanced RF: From Devices to Systems**
  - RFIC Receiver Circuits—J. Long
  - Key Issues in Transmitter Blocks—E. McCune
  - From RF Systems to Silicon—A. Abidi

- **Advanced Data Converter Design and Test Techniques**
  - Introduction to Data Converters—Speaker to be announced
  - Continuous-Time ADCs—K. Philips
  - Device Mismatch for Data Converter Design—P. Drennan
  - Practical Aspects of Nyquist-Rate Switched-Capacitor ADCs—D. Nain

- **High-Performance and Low-Voltage Design Challenges and Techniques**
  - Low-Power Circuit Design in SOI Technology—A. Marshall
  - High-Performance and Leakage-Tolerant Circuit Technologies—R. Krishnamurthy
  - Emerging Memory Technologies—S. Natarajan
  - Low-Power Circuit Technologies—K. Roy

- **Hands on for SOC/Mixed-Signal/RF: Design, Verification, and Test**
  - SOC and ASIC Functional Verification Methods—A. Nordstrom
  - Modeling and Simulation Issues in Phased-Locked Systems—B. Razavi
  - RF Integrated Circuit Design Using Parasitic-Aware Optimization Methods—D. Allstot
  - Test Cores for On-Chip Measurements—G. Roberts

**Exhibits**

Monday afternoon the exhibitor preview sessions kick off the opening of the Exhibits Hall. Here many of our exhibitors will present overviews of new products and services. As always, our exhibits will include displays and demonstrations by semiconductor manufacturers, software tool suppliers, design service houses, and leading electronics industry publications providing the latest technical information on new integrated-circuit design products. The Exhibit Hall also will be the site for Monday’s Exhibitors’ Reception and Tuesday evening’s Happy Hour, opportunities for attendees to network with their colleagues and the exhibitors.

**Additional Information**

The conference will take place at the Double Tree Hotel in San Jose, California. The complete advance program and registration form can be downloaded from the CICC Web site at [www.ieee-cicc.org](http://www.ieee-cicc.org). For additional information and general inquiries about the CICC, please contact the Conference Manager, Melissa Widerkehr, CICC, 16220 South Frederick Avenue, Suite 312, Gaithersburg, MD 20877; Tel: (301) 527-0900/101; or email: cicc@his.com.

**CICC Technical Session Topics**

The technical sessions include invited and tutorial papers by leading experts from industry and academia.

- **Analog Filters**
- **SOC Design, Methodology, and Infrastructure**
- **Programmable Logic: New Roads to Low Cost**
- **Timing Recovery**
- **Modeling for RF Design**
- **Oversampled Data Converters**
- **Next Generation RF Technologies**
- **Application-Specific Signal Processors**
- **Nano Devices and Other Alternatives to CMOS Scaling**
- **Advanced MOSFET Modeling**
- **DSP for Communications**
- **Building Blocks for Broadband Communications**
- **Directions in Process and Integration Design and Modeling Challenges**
- **Emerging Memory Circuits and Technology**
- **Nyquist Converter Techniques**
- **Transmitters and Receivers for Wireless Systems**
- **Custom Design and Applications**
- **Bioelectronic Systems**
- **Interconnect Schemes for Multi-GHz RF**
- **RF and Microwave Generation Techniques**
- **Broadband Wired Communication Systems**
- **Towards Testing in the 90-Nanometer Era**
- **Low-Power Circuits and Techniques**
- **SOC Design Challenges and Tradeoffs**
- **Analog Techniques**
- **Noise Modeling**
Converting regional birth into international breadth was more difficult. As late as 1961, four northeast-region American companies (BTL, GE, IBM, and RCA) contributed over 50% of all conference papers. The first overseas Program Committee members appeared in 1960. These were, of necessity, “corresponding” members. Much of the industrialized world was still recovering from the aftermath of World War II. Overseas travel was expensive and, therefore, a major hurdle to conference participation. Military-sponsored research was still a major source of solid-state funding. The Office of Naval Research provided travel for overseas speakers through the Military Air-Transport Service. The other armed services soon joined this support, and the practice continued into the 1970s.

By 1965 the number of overseas Program Committee members had increased to eight, and by 1968 the number and quality of overseas papers was on a par with those from North America. Throughout the 1960s overseas members contributed primarily by soliciting submitted papers (with written commentary), which were mailed to the U.S. Program Committee.

In 1970 the overseas membership was greatly expanded and began meeting separately in both Europe and Japan under the leadership of Jan van Vessem and Takuo Sugano, respectively. Selected members were dispatched to the final Program Committee meeting in Philadelphia with the results of these deliberations. The Executive Committee was expanded to include the overseas chairs.

Today, there are 32 members of the European Program Committee and 34 members of the Far-East Program Committee, not counting liaison members. Overseas members participate in all aspects of the conference organization and technical program selection. Approximately one-half of all ISSCC papers presented originate from outside North America. Some papers have authors on multiple continents. The “I” in “ISSCC” is real!

**Evolution of the Technical Program and the Program Committee**

The original Program Committee was formed by recruits drawn from the Circuit-Theory Group 4.10 Committee. The Program Committee soon adopted the practice of rotating membership, so that each year 30% would “retire” and be replaced by “new” members. In the formative years the Program Committee would reorganize itself yearly into new subcommittees to grapple with an ever-changing menu of new paper topics. In an era unconstrained by the demands of integration, a broad spectrum of technologies found their way into the “solid-state tent.” A few of these technologies, like tunnel diodes, had very short lifetimes.

In 1968 the Program Subcommittee evolved: Digital, Analog (Linear), Microwave, and “Other.” The rather nondescript “Other” referred to a brave band of committee members prepared to review one-of-a-kind papers. By the mid-1960s the enormous economic power of circuit integration had marginalized many competing solid-state technologies, particularly magnetics, as well as semiconductor devices requiring unique diffusion profiles. Solid-state came to mean solid-state integrated semiconductor circuits. This four-subcommittee organization of the Program Committee would remain stable for the next fifteen years.

The last year of the Microwave Subcommittee was 1984. Microwave technology had largely remained in discrete circuits or low-level integration. The Microwave program had become a conference within a conference, exhibiting little overlap with wider attendee interest. Thereafter, Microwave was dropped from the program. Diversification in integrated circuit application rapidly filled the void.

By 1987 Digital had split into separate Digital and Memory Subcommittees, and a Signal-Processing Subcommittee had joined the Program Committee roster. “Other” was given the more genteel title of “General,” eliminating some rather bad insider jokes.

In 1992 the proliferation of subcommittee disciplines resumed, with the launching of the Emerging Technologies Subcommittee. This was the first subcommittee specifically chartered to seek out solid-state applications that had not already found a home in ISSCC. Both the subcommittee title and its charter were eventually expanded to Technology Directions. Papers reviewed by this subcommittee have become one of the most highly ranked features of the conference.

The 42 top contributing authors over the years of the ISSCC were named to the Author Honor Roll at the 50th Anniversary Plenary in 2003. Shown here, as plaques were presented to the top 10 contributing authors, are: Masakazu Yamashina, Behzad Razavi, Michel Steyaert, Asad Abidi, Mark Horowitz, Bruce Wooley, Robert W. Brodersen, David Hodges, Paul Grey, and James Meindl.
Through the 1990s an explosion in communications papers added to the list of separate subcommittee disciplines. A steady growth in submitted papers throughout the late 1990s and early 21st century has kept each new subcommittee’s paper review schedule fully loaded. The 2003 subcommittees consist of Analog; Digital; Imagers, Displays, and MEMs; Memory; Signal Processing; Technology Directions; Wireless and RF Communications; and Wireline Communications. The committees reviewed 450 submitted papers to bring you the 2003 program.

The Move from Philadelphia
ISSCC was founded in Philadelphia by the University of Pennsylvania and the local chapters of the IRE and the AIEE (forerunners of the IEEE). In the formative years, ISSCC garnered broad support from established electronics firms in the American northeast. Many of these firms were within easy driving distance of the conference’s home on the campus of the University of Pennsylvania.

However, by the mid-1960s the center of semiconductor development in the United States was shifting west, and the international nature of the conference was coming into much sharper focus. Western attendees gradually became more vocal about moving the conference to San Francisco. Unsurprisingly, the founders preferred their Philadelphia home. They had a surprisingly effective, if somewhat perverse-sounding, argument. “When an engineer says he wants to attend a conference in Philadelphia in February, management knows he is sincere.” Strong conference attendance, even in weak economic years, seemed to validate this view.

A campaign by western attendees, orchestrated by David Hodges, convinced the sponsors to try San Francisco in 1978. The first year, California attendance was large and the response was gratifying. The conference then continued to alternate coasts, with New York soon substituting for Philadelphia. After a decade of consistently stronger attendance in California, the conference made San Francisco its permanent home in 1990.

The Role of the Executive Committee
ISSCC is the single largest financial entity within the oversight of the IEEE Solid-State Circuits Society. Although it is strictly a non-profit organization, financial sobriety requires that it be run like a business.

From the very beginning, the operations of the Executive Committee were made entirely separate from those of the Program Committee. The organizational philosophy was to keep the Program Committee firmly focused on the quality of the program without the distraction of concerns about conference operations or financial balance. This separation, which was somewhat innovative at the time, has now become common industry practice. In the beginning, this ‘business’ committee was called the “National Committee,” a name reflecting the regional origins of the conference. The name was changed to “Executive” once the conference firmly gained its international stature.

The Executive Committee’s structure has changed considerably over the years. From the early years through 1980, the post of Conference (and Executive Committee) Chair usually was filled by the previous year’s Program Chair. In roughly these same years, continuity-of-business acu-
men was provided by the Treasurer Bob Mayer, Digest Editor Lew Winner, Local Arrangements Chair Henry Sparks, and the Chair of the Sponsors Committee Murlin Corrington. All four of these people had been continuously active in the leadership of the conference from the formative years. Other posts, such as Secretary and International Arrangements, rotated more often. In the 1980s all four of these pioneers would retire or die.

Starting in 1980, the term of Executive Chair was extended to multiple years (typically five to eight). Since 1980 there have been just four chairs: Jack Raper, David Pricer, John Trnka, and Tim Tredwell. All four would oversee significant changes in the conference.

The Lew Winner Years

Lewis Winner began his career as a technical writer and New York City radio commentator. In 1956 he was recruited to help edit what was then called the “Technical Addendum to the Program Booklet.” This would eventually become the Digest of Technical Papers, but initially looked more like today’s “Visual Supplement.” He and Editorial Chair, Jack Raper, assisted by Lew’s wife, Beatrice, maintained a standard of excellence for decades. Over the next three decades, the fortunes of Lew and the ISSCC would become progressively more intertwined. In retrospect, it is difficult to say which influenced the other the most.

Lew’s early association with ISSCC was tenuous. He didn’t even put his name on the first Digest. Formal arrangements stipulated that he would be paid, but only if the conference showed a surplus. His title was Public Relations, which he kept to the end—well beyond the point where it was anywhere near descriptive of his duties.

By the mid-1970s Lew was effectively the general manager of the conference. As many of the pioneers retired in the 1980s, he assumed some of their duties. He worked Herculean hours for a modest fee. His ability to resist sleep deprivation was storied. For fifty weeks a year, his life WAS the ISSCC. Then for two weeks each year, he took a hotel room in Fort Lauderdale, sat on the beach, and compiled the conference statistics. That was Lew’s vacation! As noted in his 1988 obituary, in his later years he came to enjoy playing the role of the curmudgeon, demanding excellence from anyone associated with the conference, and delivering scorn in the event it wasn’t immediately forthcoming.

W. David Pricer
Consultant

Originally published as “ISSCC — The Later Years” in the ISSCC 2003 Digest of Technical Papers, this article will be continued in the October issue of the newsletter.

ISSCC Museum

Imagine that a group of SSCS experts have identified 70 outstanding articles in the history of Solid-State Circuits, have summarized the articles, and are showcasing them free of charge on a virtual museum. It is a museum of 70 ideas that spans over 50 years of solid-state circuits history.

“I definitely recommend visiting the museum to all my students taking Solid-State Circuits at the University of Toronto. I plan to bring the museum to my class, discussing one or two articles at the beginning of each lecture. A critical walk through the last 50 years of ideas can inspire and contribute to the next 50 years of ideas.” Visit the ISSCC Museum at sscss.org/isscc50.

Ali Sheikholeslami
Museum Coordinator
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Virtual Museum Launches New Microwave Exhibit

The IEEE Virtual Museum (VM) has launched a new exhibit, “Microwaves: From Your Kitchen to the Edges of the Universe.” The exhibit highlights the ways microwave technology impacts daily life and, like all VM exhibits, explains how the technology works and fits into historical and social contexts. “Microwaves” was sponsored by, and largely written by, the IEEE Microwave Theory and Techniques Society. Visit the museum at www.ieee.org/museum.
A JSSC Classic Paper:
All-MOS Charge-Redistribution A/D Conversion Technique

This sixth most frequently cited JSSC article by Jim McCreary and Paul Gray at UC Berkeley, appeared in December 1975. McCreary recalls the background impact and legacy.

More top cited JSSC articles are listed at sscs.org/jssc/topcites.htm

Background
To say that 1975 was a period of change for analog integrated circuits would be an understatement. For all that happened then and all that followed in the industry, I have felt lucky to be involved. However, the project came about not as the result of luck but as the first leg of well-guided strategy by several professors at the University of California, Berkeley (UCB), to make “MOS analog” a reality. In particular the guidance that I received from Professors Paul Gray and Dave Hodges was invaluable to the success of the project. I will always be indebted to them. Looking back, the concept of the paper seems obvious today, but at the time this was uncharted territory full of unknowns and the fear that if feasibility could not be demonstrated, I would be a graduate student forever.

During that period analog products were dominated by bipolar technology with laser-trimmed thin-film resistors for quantizing current—a mature, accurate, and dominant technology. However, this was not cost-effective for products requiring large digital circuits. In contrast, MOS technology provided high-density, low-cost digital circuits but relatively mediocre 8-bit accurate analog circuits. The strategy at Berkeley was to eliminate this barrier starting with new techniques for MOS data converters. Fortunately, I was able to be a part of this effort.

The Data Converter Challenge
The feasibility of creating MOS current sources that could compete with bipolar was discarded from the beginning and a new approach of working with charge was considered to be more attractive. Working with charge was intriguing because the high impedance of the MOS gate would hold charge with minimal loss. Precision charge quantizers needed for data conversion had not been developed and the viability of such a technique required overcoming a variety of perils including: dielectric absorption, temperature coefficient, voltage coefficient, parasitic capacitance, switch feed-through, and matching requirements.

The Charge-Redistribution A/D Converter Project
A novel circuit was developed and fabricated in the UCB semiconductor lab in NMOS technology. The particular test chip was a 10-bit quantizer and comparator that comprised the key blocks of a 10-bit A/D converter. Numerous problems were encountered that resulted in a redesign of the capacitor array to improve matching. Process and instrumentation improvements provided data that led to identification of the sources of error and what would be required to further reduce these. Ten-bit accuracy was achieved.

ISSCC Presentation and JSSC Paper
The project was presented at the 1975 ISSCC conference and was voted one of the “Best Papers” of the conference. Because of this, Professor Gray (now Vice Chancellor and Provost at UCB) was relentless in the pursuit of perfection for our December 1975 JSSC paper since he believed that it “might be heavily referenced.” The paper was especially important because many of our peers were skeptical about the viability of charge-redistribution even after the conference paper. Over the following two months, the paper was revised and revised without mercy. During this process significant additional lab work was performed and more precise data was taken that allowed identification and measurement of error sources as well as detailed suggestions for reducing error sources. As a result, the paper reflected a heavy emphasis upon teaching others how to implement the new technique. It included a full disclosure of what was done in the design of the circuit and how to reduce the remaining error sources. Supporting data was provided and anticipated questions were answered proactively. This was essential to convey the reality of charge-redistribution to a skeptical peer group. The paper became the perfect template for others to use to replicate the technique. This is exactly what happened over the next few years. As co-workers were able to reproduce and improve upon the results, skeptics became believers, ideas became reality, and the market began to see a new generation of MOS data converter products based upon charge-redistribution.

Industry Impact
The essence of the novel circuit was that it inherently included a sample-hold circuit, and the sample-hold capacitor was the same capacitor used for the quantizer. This reduced area by a factor of two and eliminated the need for an external sample-hold circuit. Also intrinsic in the design was the elimination of the parasitic capacitance by creating a virtual ground at the capacitor top plate and the driving of the bottom plate by voltage sources. This allowed high accuracy in the technique independent of the parasitic capacitance. In addition the technique of charge-redistribution requires zero DC current—making it suitable for low-power applications. All of these benefits provided a cost-performance tradeoff that exceeded conventional technology at the time. This led to a fundamental patent. Within the next two years charge-redistribution was used in PCM CODECs and switched capacitor filters used in telephony. Within the next five years this technique became the dominant approach for digital telephony throughout the world and was licensed by nearly all major telecommunications companies during the seventeen-year lifetime of the patent.

Continued on page 8
Legacy
The legacy of the work done at Berkeley in 1975 was more fundamental than its impact upon telephony. Moreover, the work published in the JSCC paper demonstrated that while bipolar technology provides excellent current quantization, MOS technology provides superior charge quantization. In order to implement mixed analog-digital ICs that required high accuracy, it was necessary for analog designers to think in terms of charge rather than current—quite a challenge for 1975. The technique is described in most CMOS analog IC design textbooks used in the classroom today.

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2003 IEEE Fellows

An IEEE Fellow is a member of unusual distinction in the profession. This recognition is conferred by the Board of Directors upon a person of outstanding and extraordinary qualifications and accomplishment in IEEE designated fields, who has made important individual contributions to one or more of these fields. No more than one member in a thousand of the total Institute membership may be advanced to Fellow grade in any given year.

A nomination for Fellow must be accompanied by references from at least five current IEEE Fellows. A nominee must be a Senior Member of the Institute and must have been a member in any grade for at least five years prior to the year of election. Each nomination is evaluated by the relevant technical society or council and is ranked by the 26-member IEEE Fellows Committee. Multiple reviewers produce a composite viewpoint that is used in recommending to the Board of Directors suitable candidates for election to Fellow grade. Information for nomination can be obtained on the IEEE Web site at www.ieee.org/fellows.

The IEEE conferred the distinction of Fellow on 260 of its members of the class of 2003. Here are fourteen new Fellows who are members of the Solid-State Circuits Society.

Professor Milos Ercegovc
University of California
Los Angeles, CA
For contributions to the theory and practice of digital arithmetic

Professor Rolf Ernst
Technical University of Braunschweig
Braunschweig, Germany
For contributions to the design automation of co-design hardware and software embedded systems

Dr. Norman Paul Jouppi
Hewlett-Packard
Palo Alto, CA
For contributions to the design and analysis of high-performance processors and memory systems

Dr. Rochit Rajsuman
Advantest America R&D Center
Santa Clara, CA
For contributions to the testing of very large semiconductor memory and logic integrated circuits

Dr. Graham Arnold Jullien
University of Calgary
Calgary, Alberta, Canada
For contributions to the application of number theoretic techniques in signal processing

Professor Sachin Suresh Sapatnekar
University of Minnesota
Minneapolis, MN
For contributions to the optimization of timing and layout in VLSI circuits

Dr. Wilhelm Wolfgang Jutzi
University of Karlsruhe
Karlsruhe, Baden-Wurttemberg, Germany
For contributions to superconducting digital integrated circuits and microwave technologies

Professor Rolf Ernst
Technical University of

Dr. Heinrich Peter Baltes
ETH Zurich
Zurich, Kanton, Switzerland
For contributions to the development and commercialization of CMOS-based MEMS

Dr. David Lynn Cave
Motorola
Tempe, AZ
For contributions to analog product development and smart power devices

Dr. Mohamed Jamal Deen
McMaster University
Dundas, Ontario, Canada
For contributions to modeling, noise, and parameter extraction in silicon transistors and high-speed photodetectors

Professor Tadahiro Ohmi
Tohoku University
Sendai, Miyagi, Japan
For contributions and leadership in semiconductor engineering

Professor Mark James Rodwell
University of California
Santa Barbara, CA
For contributions to high-speed electron devices and integrated circuits

Steven Howard Voldman
IBM
Essex Junction, VT
For contributions to electrostatic discharge protection in CMOS, silicon on insulator, and RF silicon germanium technology

Dr. Mitsuo Makimoto
Matsushita Electric Ind. Co.
Kawasaki, Japan
For contributions to the development of microwave and radio frequency devices

continued from page 7
Congratulations to New Senior Members

Sudhir Aggarwal  
Salman Akram  
Walid Y. Ali-Ahmad  
Mohamed Arefah  
Hugh J. Barnaby  
Bruce A. Bernhardt  
Thomas Brazil  
Gert Cauwenberghs  
Lee H. Colby  
Robert H. Eklund  
David R. Figueroa  
Denis Flandre  
Gregory Freeman  
George E. Georgiou  
Robert J. Gresham  
Yan Kit G. Hau  
Seong-Ook Jung  
Pradeep B. Khannur  
Duy-Loan Le  
Khanh Tuan Le  
Dain C. Miller  
Lawrence Nagel  
Robert L. Nielsen  
Tobias G. Noll  
Piotr Pawlowski  
Paul A. Potyray  
Norman J. Rohrer  
Mary J. Saccamango  
David B. Scott  
Osama Shana’a  
Shye Shapira  
Zhongming Shi  
Malcolm H. Smith  
Gerhard Stelzer  
Toshib Sunaga  
Wanlop Surakampontorn  
Tang Ting-ao  
Gregory Uvieghara  
José M. López-Villegas  
Scott F. Wettenkamp  
David A. Wood

How to Apply for Senior Membership

There are many benefits associated with upgrading to Senior Membership. Details of the program and how to apply can be found at: www.ieee.org/organizations/rab/md/smprogram.html. Among the benefits of IEEE Senior Membership are:

- Professional recognition of your peers for technical and professional excellence.
- A letter of commendation to your employer on the achievement of Senior Member grade (upon request of the Senior Member).
- Announcement of elevation in Section/Society and/or local newsletters, newspapers, and publications.
- Eligibility to hold executive IEEE volunteer positions.
- An attractive wood and bronze engraved Senior Member plaque to display proudly.
- Up to $25.00 toward one new Society membership.

One requirement for Senior Membership is ten years of experience. Education counts toward this requirement according to one’s highest degree. Normally three references are required. However, if one is nominated by an IEEE Fellow, a Senior Member, an IEEE Society, or an IEEE Section, only two references are required. The application, reference, and nomination forms can be obtained from the IEEE Web site at www.ieee.org/organizations/rab/md/smelev.htm.

SSCS Thanks Schuster and Garverick

Stan Schuster and Steven Garverick were honored at the SSCS Administrative Committee meeting last February for serving as co-chairs of the Solid-State Circuits Technology Workshop program for close to a decade, going back to the days when the Society existed as a Council. The workshops, scheduled twice a year, were designed as small gatherings on a specific technical area, often an emerging technology, to ensure that dialog among participants was a primary feature. Workshops left the spark of ideas in participants’ minds and sometimes the vision of the depth of challenges before them, but never in a published proceedings — you had to be there. Programs of some past workshops are still listed in the history section on the Society’s Web pages.

sscs.org\TC_workshops\past-workshops.htm

Here is a partial list of the technology topics the workshop series featured:

- Implications of Near-Limit CMOS on Circuits and Applications (Feb. ’03)
- Analog Telecom Access Circuits and Concepts (Feb. ’02)
- Circuits for 2.5- and 3-G Wireless Systems (Feb. ’01)
- Low-Power Circuits (Oct. ’01)
- Biomedical Electronics Workshop (Oct. ’00)
- Design for Multi-GigaHertz Processors (Feb. ’00)
- MEMS Interface Circuits (Oct. ’99)
- Internal Cool Electronics (Oct. ’98)
- CMOS Imaging Technology (Feb. ’96)

The Society will continue to organize workshops, but in conjunction with existing conferences. Combining workshop events with conferences makes attendance more convenient for many participants and ensures the success essential for continuation of this kind of program.

Stan Schuster (left) and Steven Garverick (absent for photo) are the recipients of the grateful appreciation of the Solid-State Circuits Society, expressed by SSCS President Charlie Sodini (right), for their eight years of service organizing Solid-State Circuits Technology Workshops.
Wireless communications is a burgeoning market area and a major driver behind the semiconductor industry, and SiGe BiCMOS and III-V technologies have emerged as the manufacturing processes of choice for many wireless ICs. If you work or are interested in this exciting area, then the IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM) is a conference you want to attend.

Historically, BCTM has been held in Minneapolis, MN. However, due to popular demand, the conference is now on the road — in 2002 in Monterey, CA, and in 2003 (for the first time in Europe), in Toulouse, France. Through the years, Europe has been a stronghold of bipolar research and development, in manufacturing technologies and circuits, and in both industry and academic institutions. So we moved BCTM to one of the main bipolar centers of gravity. The pent-up demand for a European venue showed up in paper submissions for 2003, 30% more overall than in 2002, more than twice as many submissions from Europe as ever before, and for the first time there were more submissions from Europe than from North America.

The technical program for BCTM consists of one day of Short Courses given by noted industry experts, and two days of invited and contributed technical presentations, including a special session on emerging technologies. There will be exhibits from vendors with products of interest to those working in the bipolar/BiCMOS area. In conjunction with BCTM, TU Delft will be holding a one-day workshop in Toulouse on Compact Modeling for RF/Microwave Applications, on Wednesday, 1 October.

Social events have always been a highlight of BCTM, and this year will be no exception. There will be a welcome and registration reception on the Sunday evening. Several local tours have been arranged for people accompanying BCTM attendees, and there will be a banquet on the Monday evening, featuring a Renaissance dance troupe. Tours of local technical facilities (Airbus Industrie, LAAS, Motorola, and CNES) have been arranged for Wednesday, 1 October, and there is a tour to the nearby historic walled town of Carcassonne on Thursday, 2 October.

The Short Course will be in three parts. Professor Hermann Schumacher (University of Ulm) will address Si/SiGe HBT MMIC design techniques for 20 GHz and beyond. Professor Albert Wang (Illinois Institute of Technology) will cover ESD protection issues and design in RF and advanced BiCMOS technologies. Dr. Peter Magnee (Philips Research) will discuss state-of-the-art RF BiCMOS processes.

The keynote talk will be given by Dr. Jan Slotboom (Philips Research and TU Delft), an international authority on BJTs, on BJT evolution in Europe. The luncheon talk on Monday, always a conference favorite, will be given by Dr. Jean-Marie Chopin (Airbus Industrie) on the evolution of fly-by-wire.

The technical program consists of 11 sessions, with 44 papers in all (including 5 double-length invited papers), plus the special emerging technologies session. Session topics include RF and high-speed circuits, process technology (including power devices), bipolar device physics, and modeling and simulation of BJTs. The special emerging technologies session will start with Professor Jean Therme (LETI/CEA Grenoble) talking about MINATEC, the European Center for Innovation in Micro and Nano-Technologies. Dr. Joost van Beek of Philips will present “High-Q integrated RF passive and micro-mechanical capacitors on silicon.” Dr. Jean-Luc Pelloie (SOISIC) will cover “Reliability issues in SOI technologies and circuits.” Professor Rashid Bashir (Purdue) will present “From BioMEMS to bionanotechnology: interfacing life sciences and engineering at the micro and nanoscale.”

So between the exciting move to Europe, the technical presentations, and the associated TU Delft workshop and BCTM tours and banquet, BCTM2003 is a must for those working in bipolar/BiCMOS technologies. And did we mention the local French culture, food, and wine? And the reduced-fare TGV from Paris via Bordeaux?

We hope you will join the BCTM World Tour, — see you in Toulouse! See www.ieee-bctm.org for more details (links to other local activities and sites are included).

Colin McAndrew
General Program Chair
Ross Teggatz
Technical Program Chair
Marise Bafleur
Local Arrangements Chair
Shanghai Chapter — The Shanghai Chapter held an inaugural meeting on 22 March 2003 at the Hotel Equatorial in Shanghai. Seventy-eight people, including members, attended the meeting. The representative of the IEEE Beijing Section and CIE, Mingui Zhou, introduced the IEEE and SSCS activities. The Dean of the Information Science and Engineering School of Fudan University, Professor Liangyao Chen, congratulated the members on the foundation of the Shanghai Chapter. Shanghai Chapter Chair, Professor Ting-Ao Tang, reported the activity plan of the chapter: to recruit new members, to organize seminars, to hold the 5th International Conference on ASIC, and to cosponsor ASP-DAC 2005. Two seminars comprised the remainder of the agenda: Professors Sichang Zou spoke on the “Establishment of the Shanghai semiconductor industrial base” and Shoujue Wang spoke on “An analysis method of high-dimension space geometry and its application in the future digital world.” Both speakers are Academicians of the Chinese Academy of Sciences.

Bangalore Chapter — The formal inauguration of the Bangalore Chapter was held on 16 March 2002 at the Indian Institute of Science in Bangalore. The event was cosponsored by the ECE Department, IISc, Bangalore.

On this occasion a one-day workshop titled “Future challenges in the deep sub-micron era” was conducted. The workshop included five invited seminars by experts in devices and circuits. Professor Hiroshi Iwai from Tokyo Institute of Technology gave an excellent introduction on "Silicon technology scaling trend from millimeter to nanometer." The other seminar topics were “Impact of advanced process modules on low-frequency noise in CMOS technology” by Professor Cor Claeyts, IMEC, Belgium; “Silicon-on-insulator devices for analog applications” by Professor J. Vasi, IIT, Bombay; “Designing reset systems for mixed-signal VLSI” by Rajat Gupta, Cypress Semiconductors, Bangalore; and “Building in reliability for deep sub-micron devices” by Dr. Radhakrishnan, Phillips, Singapore. The workshop received an extremely good response with about 130 attendees from industry and academia.

Denver–Fort Collins, Colorado, Chapter — A seminar at Colorado State University in Fort Collins was held on 11 April 2003. The Distinguished Lecturer, Albert Wang, spoke about "Mixed-mode ESD protection simulation-design for integrated circuits." Dr. Wang is the author of the book *On-Chip ESD Protection for Integrated Circuits*, is also author of more than sixty papers in the field, and holds several U.S. patents. His talk outlined the principles of ESD simulation-design methodology developed at the Integrated Electronics Laboratory, Illinois Institute of Technology. Practical ESD protection circuit design examples were provided. This lecture was aimed at assisting IC circuit designers in dealing with real-world ESD protection circuit design problems. Pictured on page 12 are Dr. Wang with some chapter officers and a photo of the seminar at Fort Collins.

West Ukraine Chapter — The West Ukraine Chapter cosponsored the 7th International Conference on the Experience of Designing and Application of CAD Systems in Microelectronics (CADSM 2003). The conference was held 18–21 February 2003 in Lviv-Slavsko, Ukraine. Many young scientists, engineers, and students participated at the conference. They presented results of their own scientific investigations, answering questions and hearing the comments of other experienced colleagues.

The CADSM Organizing Committee and the West Ukraine Joint Chapter presented four Best Young Speaker Awards to young authors of the best presentations at the conference’s closing ceremony.

Ting’ao Tang, SSCS Shanghai Chapter Chair, at their inaugural meeting on 22 March 2003.
awardees were Tomash Zacharz (University of Mining and Metallurgy, Cracow, Poland) for “Application of CF design software to visualization of flow suspension in a prototype settling tank;” Ivan Safonov (National University of Electronics, Kharkov, Ukraine) for “Novel cross-platform laser simulator for quantum well lasers investigation;” Bohdan Dunnets for “Multiblock RAM access controller IP cores generator;” and Pavlo Denysyuk for “Construction problems of the automation system designing of the hydrostatic systems by method of functional blocks” (both from the National University of Lviv Polytechnic, Lviv, Ukraine).

**Yugoslavia Chapter** — The 24th International Conference on Microelectronics (MIEL 2004) will be held 16–19 May 2004 at the Faculty of Electronic Engineering, University of Nis, Serbia and Montenegro.

The topics to be covered by the technical program of the MIEL 2004 Conference include all important aspects of microelectronic devices, circuits and systems, including materials and processes, technologies and devices, device physics and modeling, process and device simulations, circuit design and testing, system design and packaging, and characterization and reliability. Based on the past decade, the technical program is expected to consist of about 150 contributed papers by authors from more than 30 countries all around the world, which will be structured into oral and poster sessions. These authorities in the field of microelectronics will form the solid foundation of MIEL 2004. Two related scientific events, namely the workshops “Power devices and ICs” and “Microsystems technologies,” will round off the technical program.

For more information, visit the MIEL 2004 home page at europa.elfak.ni.ac.yu/miel.

**Varna, Bulgaria, Chapter** — Chapter activities for the past year have included many educational opportunities. Last July a two-week summer school was held on CAD in microelectronics, mainly based on Cadence and Xilinx. The classes featured lectures and discussions by professors from the Technical University (TU) of Varna and TU of Sofia. Professor Gady Golan (EDS) visited the TU of Varna in May, meeting with chapter members and lecturing students and teaching staff from the Department of Electronics. During the first week of September, Professor N. Stojadinovic (EDS) visited the TU of Varna, combining his visit with participation in the ISCMC 2002 in Varna. Professor Stojadinovic met with chapter members and lectured students and teaching staff. Chapter officers were elected in December 2002.

Denver–Fort Collins Chapter, from left to right: Alvin Loke, Secretary/Webmaster; Albert Wang, SSCS Distinguished Lecturer; Don McGrath, Chapter Chair; Bob Barnes, Treasurer.

Albert Wang speaking on mixed-mode ESD protection simulation-design for integrated circuits to the Denver-Fort Collins SSCS Chapter in April.
The leading European solid-state conferences, ESSCIRC, which deals with solid-state circuits and systems, and ESSDERC, which deals with solid-state devices and technologies, will be jointly held in Estoril, Portugal, 16–18 September. The main themes of this year’s ESSCIRC conference include: analog circuits; data converters; digital circuits, DSP, and memories; mixed-signal circuits and Systems On a Chip; and RF and VCOs. The main themes of the companion ESSDERC conference include: CMOS and memory devices; modeling, characterization, and simulation; photonics, quantum, and spin electronics; sensors, biosensors, and displays; Si IC technology, interconnect, and packaging; and solid-state and power devices.

The Technical Program Committees of both conferences have completed the selection of an exciting program encompassing a total of 51 technical sessions, 32 of which are within the ESSCIRC technical program and 19 within the ESSDERC technical program. More than 300 papers will be presented by some of the world’s leading researchers.

To complement the normal technical sessions, there will be 12 Plenary Sessions presented by renowned experts from industry and academia:

- “Trends in wireless integration,” by Josef Fenk, Infineon, Germany
- “Complex analog signal processing is not complicated,” by Ken Martin, University of Toronto, Canada
- “Power management,” by Dennis Monticelli, National Semiconductors, Italy
- “Polymer electronics and circuits,” by Eugenio Cantatore and Eduard Meijer, Philips, The Netherlands
- “Novel nonvolatile memories,” by Gerhard Mueller, Infineon, USA
- “Real IIP development and use in SOC products,” by Takashi Yoshimori, Toshiba, Japan
- “SOC and the internet age,” by Peter Kirk, Texas Instruments, USA
- “Coupled device, circuit, and interconnect simulation,” by Will Schilders, Philips, The Netherlands
- “RF CMOS devices,” by Basanthe Jagannathan, IBM Microelectronics, USA
- “Strained Si and Ge MOSFETs,” by Cristoph Jungemann, Stanford University, USA
- “Photonic crystals,” by Gregg Parker, University of Southampton, UK
- “Advanced Hi K dielectrics,” by Hiorishi Away, Tokyo Institute of Technology, Japan

A series of valuable, educational tutorials and workshops will be organized on the pre-conference day, 15 September, and on the post-conference day, 19 September. For further information about ESSCIRC-ESSDERC 2003, including a glimpse of its exciting social program and sightseeing tours of some of the most charming destinations in Europe, please visit the Web site at www.chipidea.com/esscercirc2003.
Gordon W. Day and Lewis M. Terman are the running for the position of Division 1 Delegate to the IEEE Board of Directors, both nominated by the Division. The term of office for this Board position is two years, 2004 and 2005. The Division 1 Director is elected from the members of the five Circuits and Devices Division Societies. Ballots will be mailed to all voting members of these Societies on 1 September.

- Circuits and Systems Society
- Components, Packaging, and Manufacturing Technology Society
- Electron Devices Society
- Lasers and Electro-Optics Society
- Solid-State Circuits Society.

Gordon W. Day
Division Chief, Optoelectronics Division (Retired)
National Institute of Standards and Technology (NIST)
Boulder, Colorado

Gordon Day received his BS, MS, and PhD degrees in electrical engineering from the University of Illinois. In 1969 he joined the National Institute of Standards and Technology (then NBS), and remained there in a variety of research and management positions until his recent retirement. He also has held adjunct or visiting positions at several universities in the U.S., Europe, and Australia. His research interests have included metrology for optical communications, optical fiber sensors, and laser radiometry. He participated in early laser frequency measurement research that resulted in a new determination of the speed of light and ultimately led to a redefinition of the meter. From 1994 to 2003 he led and managed the NIST Optoelectronics Division, which develops measurement technology for the optoelectronics industry and provides traceability through standards and calibration services. He continues a close association with NIST and serves in a variety of professional advisory and volunteer positions.

IEEE Activities — (S’66–M’67–SM’78–F’94):
- Conferences: Optical Fiber Communications Conference, Steering Committee, 1997-02; Optical Fiber Sensors Conference, Program Committee, 1989-96; International Steering Committee, 1992-99; General Chair, 1997; Symposium on Optical Fiber Measurements, Program Chair, 1980-98; General Chair, 2000.
- Representative To: Nanotechnology Committee, 2000-01; Coalition for Photonics and Optics, 1998-01; RAB, 2002-03.

Gordon Day’s Statement

Becoming an IEEE member and working with other members to develop and manage our journals, conferences, and other services are among the best professional investments I’ve made. With resources and good management, we can make the membership experience, and IEEE’s products and services, even better. But sadly, the IEEE is weaker than it was a few years ago. Our assets declined 42% ($56M) in the three years ending December 2002. Our Societies, Councils, and other units are now less able to invest the revenues they generate in new and improved products and services.

We must rejuvenate the Institute. The process has begun. Recommendations from a major study target greater efficiency and effectiveness in management and governance, and improvements in investment policy, among others. Some are being implemented. Others are difficult, involve hard choices, and will take time.

Electing fresh leadership, with solid management experience and the time and energy to effect change, can help speed this process. I believe that I can serve the IEEE effectively in this way, and I ask for your vote.

Lewis M. Terman
President, IBM Academy of Technology
IBM Somers
Somers, New York

Lewis Terman received his BS in Physics and his MS and PhD in electrical engineering from Stanford in 1956, 1958, and 1961, respectively. He joined the IBM Research Division in 1961, where he has worked on solid-state circuits, semiconductor technology, memory design and technology, digital and analog circuits, and processor design. He did two tours of duty on the Research Division’s technical planning staff, 1979–80 and 1991–93. He was manager and senior manager of groups working in MOS logic and memory design and technology, and has been involved with several programs leading to products. He is a member of the National Academy of Engineering. He was elected to the IBM Academy of Technology in 1991, and is serving as its president for the 2001–03 term.

IEEE Activities — (S’58–M’61–SM’74–F’95):
- Committees/Boards: Nominations and Appointments, 1993–94; Strategic Planning, 1998–99; Awards Board, Vice Chair, 1996–97; Awards Planning and Policy, Chair, 1996–97; Proceedings Editorial Board, 1990–03; Publication Services and Products...
Tales from the History of Microelectronics: A Book Review

Solid-State Circuits Society Newsletter

Microchip: An Idea, Its Genesis and the Revolution

To be immersed in the challenges of another time is the measure of well-written history. Zygmont engages the reader in great stories of the growth microchip industry: the innovations, the personalities, the visionaries and the unbelievers, and the rapid market shifts.

Zygmont brings alive the time when bonders would stitch around each bad transistor on a chip because the yield was 10 to 25 percent. Circuit designers were professionally dismissive of prefabricated expensive multi-purpose circuits where the individual components were inaccessible for testing in an IC. As the chapters move the reader quickly along, the solutions to the problems leave one refreshed and a bit in awe.

Zygmont describes complex concepts in a few clear and precise paragraphs: diffused versus grown junction transistors, Jean Hoerni’s planar technology, Frank Wanlass using an electron beam evaporator to vaporize sodium in the MOS process. A Web-hosted reviewer commented, “The depth of the treatments of all of these subjects is just enough to tell you what you need to know about the major events and players, though I have to admit, in many places I would have willingly accepted more detail.” Microchip might make a fine gift for a summer intern or a curious family member.

Allow yourself to get past the occasional error introduced by relying on first-hand memories of Shockley’s friends. Zygmont clearly goofed when he failed to correctly note Shockley’s undergraduate alma mater as Cal Tech. However, wonderfully frank first-hand recollections of early days and the self-effacing comments of Gordon Moore make up for a lack of rigorous precision. Varying corporate cultures, skills at patent writing, and royalty negotiations along with market timing and shifting teams are part of the tale. Fundamental IC tales are told along with the applications that grew the consumer market and allowed fabrication costs to drop. Linder at Motorola developed frequency synthesizers for cellular phones and then John Mitchell sold the technology to the FCC to get the spectrum licensing needed. They took cell phones out of police trunks and put them into everyone’s hands. Wang and Kuplow enabled the explosion of office automation. Fosnough, Forestner, and McConnell brought microprocessor controls to the microwave oven and overnight heated up their careers and the home appliance business.

As a business technology writer for Business Week, Inc., and CFO and staff writer for High Technology and Omni, Zygmont covers how early technical leaders had to find whole new segments of consumer acceptance. Sometimes motivated by military research goals and other times enticed by the rewards of mass-market consumption, IC producers are now culture shapers.
SSCS EVENTS CALENDAR
Also posted on www.sscs.org/meetings

SSCS SPONSORED MEETINGS
2003 CICC Custom Integrated Circuits Conference
www.his.com/~cicc
21–24 September 2003
DoubleTree Hotel, San Jose, CA, USA
Contact: Ms. Melissa Widerkehr, cicc@his.com

2004 ISSCC International Solid-State Circuits Conference
www.isscc.org
15–19 February 2004 – NOTE CHANGE OF DATE
San Francisco Marriott Hotel, San Francisco, CA, USA
Paper deadline: 5 September 2003
Contact: Courtesy Associates, ISSCC@courtesyassoc.com

TECHNICALLY CO-SPONSORED MEETINGS
2003 International Symposium on Low-Power Electronics and Design
poppy.snu.ac.kr/~islped
25–27 August 2003
Soeul, South Korea

2003 European Solid-State Circuits Conference
www.esscirc.org/
16–18 September 2003
Lisbon, Portugal

2003 Bipolar/BiCMOS Circuits and Technology Meeting
www.ieee-bctm.org/
28–30 September 2003
Toulouse, France

2003 GaAsIC Symposium
www.gaasic.org/
21–23 October 2003
Monterey, CA, USA

2003 International Conference on Computer-Aided Design
www.iccad.com
9–13 November 2003
San Jose, CA, USA

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