A Variable Delay Line Phase Locked Loop for CPU-Coprocessor Synchronization

As Microprocessor frequencies continued to increase, chip-to-chip connection speeds also had to scale upwards, and more stringent I/O timing requirements meant that large clock buffer delays (and the associated chip-to-chip timing uncertainties) could no longer be tolerated. Therefore, it became necessary to synchronize the chip clock with a global reference signal. Soon after this paper, on-chip clock synchronization techniques were adopted in a widespread fashion across most of the microprocessor industry.