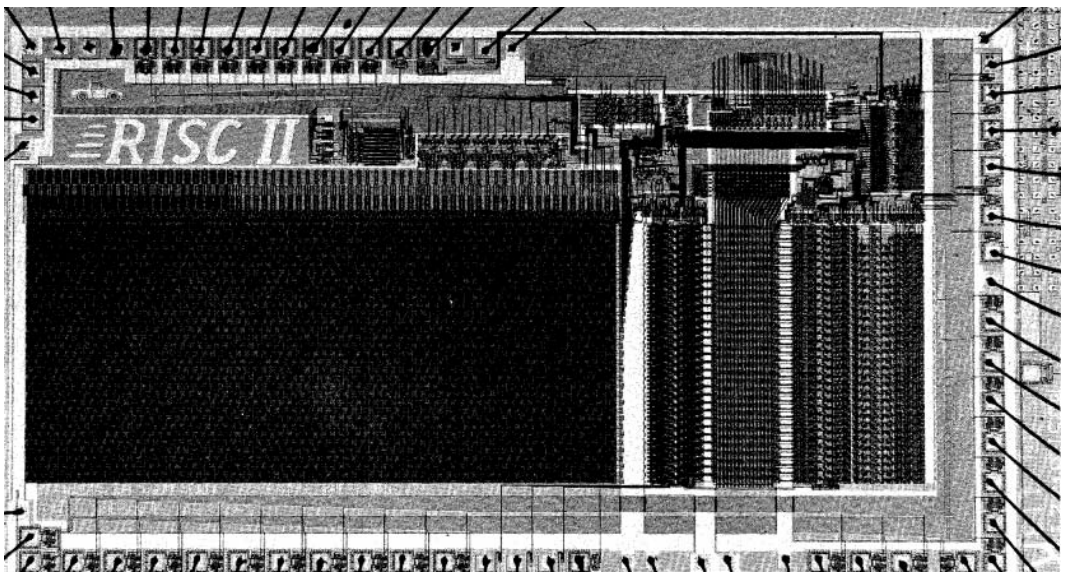
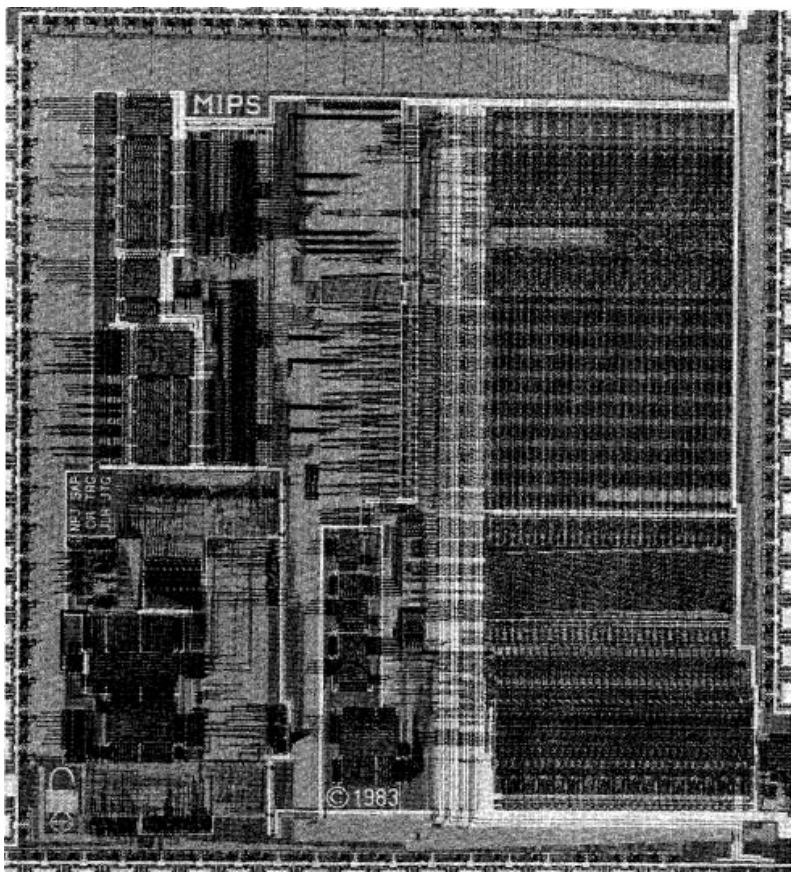
RISC PROCESSORS

ISSCC 1984





A 32b NMOS Microprocessor with a Large Register File [A]
&
A Pipelined 32b NMOS Microprocessor [B]

IN AN EFFORT to obtain higher clock frequencies, and overall higher system performance, new RISC (reduced instruction set computer) architectures appeared, as described in these two ISSCC papers. The RISC architectures focused on providing maximum throughput for a small set of simple instructions, emphasizing speed and simplicity with synchronous execution pipelines for high-speed operation. Commercial RISC processors appeared shortly after these ground-breaking papers.

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