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September 2018

NEWS

UPCOMING WEBINAR



**Energy-Efficient Deep Learning:
Challenges and Opportunities
Presented by Vivienne Sze,
Associate Professor, MIT**

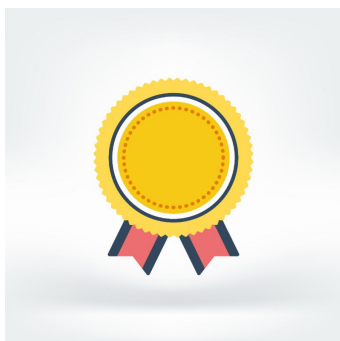
October 24, 2018 at 12 PM ET

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REGISTER**

Abstract: This talk will describe methods to enable energy-efficient processing for deep learning, specifically convolutional neural networks (CNN), which is the cornerstone of many deep-learning algorithms. Deep learning plays a critical role in extracting meaningful information out of the zettabytes of sensor data collected every day. For some applications, the goal is to analyze and understand the data to identify trends (e.g., surveillance, portable/wearable electronics); in other applications, the goal is to take immediate action based the data (e.g., robotics/drones, self-driving cars, smart

Internet of Things). For many of these applications, local embedded processing near the sensor is preferred over the cloud due to privacy or latency concerns, or limitations in the communication bandwidth. However, at the sensor there are often stringent constraints on energy consumption and cost in addition to throughput and accuracy requirements. Furthermore, flexibility is often required such that the processing can be adapted for different applications or environments (e.g., update the weights and model in the classifier). We will give a short overview of the key concepts in CNNs, discuss its challenges particularly in the embedded space, and highlight various opportunities that can help to address these challenges at various levels of design ranging from architecture, implementation-friendly algorithms, and advanced technologies (including memories and sensors).

Bio: Vivienne Sze is an Associate Professor at MIT in the Electrical Engineering and Computer Science Department. Her research interests include energy-aware signal processing algorithms, and low-power circuit and system design for portable multimedia applications, including computer vision, deep learning, autonomous navigation, and video process/coding. Prior to joining MIT, she was a Member of Technical Staff in the R&D Center at Texas Instruments, where she designed low-power algorithms and architectures for video coding. She also represented TI in the JCT-VC committee of ITU-T and ISO/IEC standards body during the development of High Efficiency Video Coding (HEVC), which received a Primetime Emmy Engineering Award. She is a co-editor of the book entitled "High Efficiency Video Coding (HEVC): Algorithms and Architectures" (Springer, 2014). Prof. Sze received the B.A.Sc. degree from the University of Toronto in 2004, and the S.M. and Ph.D. degree from MIT in 2006 and 2010, respectively. In 2011, she received the Jin-Au Kong Outstanding Doctoral Thesis Prize in Electrical Engineering at MIT. She is a recipient of the 2017 Qualcomm Faculty Award, the 2016 Google Faculty Research Award, the 2016 AFOSR Young Investigator Research Program (YIP) Award, the 2016 3M Non-Tenured Faculty Award, the 2014 DARPA Young Faculty Award, the 2007 DAC/ISSCC Student Design Contest Award, and a co-recipient of the 2017 CICC Best Invited Paper Award, the 2016 IEEE Micro Top Picks Award and the 2008 A-SSCC Outstanding Design Award.



2018-2019 SCS Predoctoral Achievement Award

Application Period is Now Open!

Deadline: October 15, 2018

For a small number of graduate students, IEEE SCS Predoctoral Achievement Awards provide a \$1000 honorarium and reimbursement for travel expenses (with certain limits) to [ISSCC](#), the Society's flagship conference. Applicants must be members of IEEE and the Solid-State Circuits Society and have completed at least one year of study in a PhD program in the area of solid-state circuits. Awards are made on the basis

of academic record and promise, quality of publications, and a graduate study program well matched to the charter of SSCS.

For application instructions, please [click here](#).

If you have any questions about the application process, please send an email to sscspredocaward2018@ieee.org.

Winners will be announced in December 2018.



Congratulations to IEEE Technical Activities Board Hall of Honor Inductee, Rakesh Kumar

SSCS Past-President Rakesh Kumar was inducted to the IEEE Technical Activities Board Hall of Honor in 2018 for "leading and growing TAB's participation Sections Congresses" [Read More...](#)



Introducing - SSCS Chip Chat

SSCS' educational programming has expanded to include a podcast called SSCS Chip Chat. This interview style podcast focuses on the stories of engineers and scientists behind the integrated circuits that power the world.

The podcast can be listened to by searching SSCS Chip Chat in the Apple Podcast App or whatever podcast app you use for your mobile device.

You can also listen to the podcast online. [Click here to listen!](#)

Episode 1: Dr. Gert Cauwenberghs

Episode 2: Albert Theuwissen

Episode 3: Shanthi Pavan

Episode 4: R. Jacob Baker

SSCS Women in Circuits Update

The SSCS Women in Circuits (WiC) committee organized the first WiC Sunday evening workshop chaired by Vivienne Sze at the 2018 ISSCC with a theme of "Circuits for Social Good". The workshop highlighted how circuits can facilitate addressing some of the important societal challenges in health care and energy conservation. The evening program consisted of invited talks from Teresa Meng, Nevine Nassif, Esther Rodriguez-Villegas, and Christine Ho, as well as round-table discussions with speakers from industry, academia and startups. The Workshop on Circuits for Social Good was open to public in addition to the ISSCC attendees with a crowd of 288 attendees. The workshop was a great success according to the attendees and also was covered in EE Times.

The WiC committee organized several successful networking events at other SSCS conferences in 2018. The joint WiC and Women in Engineering (WIE) networking event hosted Barbara De Salvo as the guest speaker at VLSI Symposium 2018 and the recent SSCS Diversity Luncheon at ESSCIRC had featured talks from Andreia Cathelin, Sven Mattisson, Alice Wang, and Jan Van der Spiegel. The luncheon was concluded with an interactive discussion on how to enhance and support diversity in the ESSCIRC and ESSDERC community.

Following the success of the 2018 ISSCC Workshop on Circuits for Social Good, the WiC committee is now organizing a workshop chaired by Kathy Wilcox with a theme of "How to Save Lives with Circuits" at the 2019 ISSCC. The upcoming workshop will highlight circuits and their impact on healthcare-related industries with a specific focus on the future of healthcare, biomedical systems for neuro-interfaces, and last but not least smart silicon chip solutions to the life science industry. The evening will conclude with an interactive panel discussion moderated by Ingrid Verbauwhede and titled as, "What Can Circuit Designers do to Bolster Security in AI-Driven Healthcare". The aim of the panel is to provide diverse perspectives from system architects, security experts, and circuit designers on the use of the large amount of data that is being generated from monitoring of our health status.

UPCOMING SOCIETY-SPONSORED EVENTS



Women in Circuits Bay Area Networking Luncheon

November 9, 2018
12:00 PM - 3:00 PM
IL Fornaio, 520 Cowper Street, Palo Alto, California 94301

Join the second Women in Circuits Bay Area Networking Luncheon. Build and sustain a community among women in circuits. Meet and network with female luminaries in engineering.

Agenda

12:00 PM - Doors Open
 12:10 PM - Women in Circuits Program Overview by Yildiz Sinangil
 12:20 PM - "Networking, Mentoring, and Advocacy for Women in Circuits" by Alice Wang, PsiKick, Senior Director, USA
 12:35 PM - Remarks by Mojtaba Sharifzadeh, SSCS Silicon Valley Chapter Chair

12:50 PM - Mentoring Roundtables

2:30 PM - Concluding Remarks

Pricing:

SSCS Member - \$20

IEEE Member - \$25

Non-Member- \$30

This event is non-refundable

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Student Design Contest & 16th International System-on-Chip (SoC) Conference

The IEEE Orange County SSCS Chapter and Lattice Semiconductor are sponsoring a Student Design Contest to be held on October 17, 2018 as part of the 16th International System-on-Chip (SoC) Conference at UCI-Calit2. All SoCal Engineering and Computer Science majors are invited to submit an abstract and present their final projects on October 17th to a group of judges. For more info visit: <http://www.socconference.com/students.htm>

IEEE Student Members receive 50% off discount for the SoC Conference and IEEE & SSCS Members receive \$50.00 discounts. More info: <http://www.socconference.com>

Women in Circuits Luncheon at A-SSCC

Nov. 6, 2018 - 12 PM at Shanghai Pavilion, Shangri-La's Far Eastern Plaza Hotel, Tainan, Taiwan

Speaker: Claire Chen, Director, Power Management BD, TSMC

Please email Ping-Hsuan Hsieh (phsieh@ee.nthu.edu.tw) with any questions.

This event will be first come first serve.

EDUCATION

October 2018 Distinguished Lectures

SSCS Japan & Kansai	RF Harmonic Oscillators Integrated in Silicon Technologies - Presented by Pietro Andreani	October 1, 2018	Tokyo Institute of Technology, Japan Click here for more information
SSCS Kansai &	Filtering $\Delta\Sigma$ - based	October 2, 2018	Kobe University,

Japan	A/D Converters - Presented by Pietro Andreani		Hyogo, Japan Click here for more information
SSCS KAIST	RF Harmonic Oscillators Integrated in Silicon Technologies - Presented by Pietro Andreani	October 4, 2018	KAIST, Daejeon, Korea Click here for more information
SSCS UNIST Korea	RF Harmonic Oscillators Integrated in Silicon Technologies - Presented by Pietro Andreani	October 5, 2018	Ulsan National Institute of Science and Technology (UNIST), Ulsan, South Korea Click here for more information
SSCS Singapore	Talk Title TBD - Presented by Vivienne Sze	October 8, 2018	National University of Singapore Click here for more information
IMESS 2018 SSCS Distinguished Lecture Talks	Fine grain power management in many core system on chip (SoC) - Presented by Vivek De Design challenges of RF transceiver satisfying the requirements of medical applications - Presented by Zhihua Wang High speed transceiver design for 100Gb/s broadband communications - Presented by Hyeon Min Bae	October 9 - 10, 2018	PSDC, Penang, Malaysia Click here for more information
SSCS Singapore	Wireless power transfer for miniaturized medical devices - Presented by Zhihua Wang	October 10, 2018	Fusionopolis, Singapore Click here for more information
SSCS Montreal	High-performance Digital Frequency Synthesizers for Millimeter-wave Applications - Presented by Jeyanandh Paramesh	October 11, 2018	Montreal, Canada Click here for more information
SSCS San Diego	High-power and Energy-Efficient Millimeter-wave Circuits and Systems for Next Generation Wireless - Presented	October 12, 2018	Qualcomm, San Diego, California Click here for more information

	by Harish Krishnaswamy		
SSCS Indonesia	Talk Title TBD - Presented by Vivek De	October 17, 2018	Institut Teknologi Bandung (ITB), Indonesia Click here for more information
SSCS Singapore	Design of Synthesizable Digital PLL - Presented by Jae-Yoon Sim	October 18, 2018	Nanyang Technological University, Singapore Click here for more information
SSCS Montreal	High-speed transceiver design for >100Gb/s broadband communications - Presented by Hyeon-Min Bae	October 25, 2018	Montreal Click here for more information
SSCS San Fernando Valley	Wireless powering for Ultra Low Power Batteryless IoT Sensing and Communication - Presented by Arun Natarajan	October 25, 2018	California State University, Northridge, California Click here for more information
SSCS Montreal - Azita Emami	Wireless Wearable and Implantable Biomedical Devices - Presented by Azita Emami	October 30, 2018	Montreal Polytechnique, Montreal, Canada Click here for more information

CONFERENCES

Upcoming Conferences

<u>2018 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)</u> San Diego, CA	October 14 - 17, 2018
<u>2018 IEEE Biomedical Circuits and Systems Conference (BioCAS)</u> Cleveland, OH	October 17 - 19, 2018
<u>2018 IEEE Asian Solid-State Circuits Conference (A-SSCC)</u> Tainan, Taiwan	November 5 - 7, 2018
<u>2019 IEEE International Solid-State Circuits Conference (ISSCC)</u> San Francisco, CA	February 17 - 19, 2019
<u>2019 IEEE Custom Integrated Circuits Conference (CICC)</u> Austin, TX	April 21 - 24, 2019

CALL FOR PAPERS

2019 VLSI-DAT - Call for Papers

2019 International Symposium on VLSI Design, Automation, and Test

The 2019 International Symposium on VLSI Design, Automation and Test will be held on April 22-25, 2019 at the Ambassador Hotel, Hsinchu, Taiwan. Original and unpublished papers on all aspects of VLSI Design, Automation and Test are solicited, including but not limited to:

ANALOG DESIGN	DIGITAL DESIGN	EDA	TEST
RF, Analog and Mixed Signal Circuits	Digital Circuits and ASICs	Logic and Behavioral Synthesis	Test Generation and Compression
Sensor and Interface Circuits	CPU, DSP and Multicore Architectures	Physical Design and Verification	Design-for-Testability and BIST
Memory Circuits and Systems	Multimedia Processing Designs	Design for Manufacturability	RF, Analog and Mixed-Signal Test
Biomedical Circuits	Communication Designs	Power/Thermal Estimation and Optimization	Memory Test
Energy-Harvesting and Power Circuits	Hardware Security and Trust	Design Verification	SOC and System Level Test
Ultra Low-Power Circuits and Systems	Designs for Edge Computing	Modeling and Simulation	Silicon Debug and Diagnosis
Memristive and Neuromorphic Circuits	Designs for Machine Learning	Electronic System Level Design	3D IC and Interposer-Based IC Test
Security Circuits for IoT and AI	SOC and NOC Architectures	Hardware/Software Co-Design	Yield and Reliability Enhancement
	Embedded System and Software	Machine Learning for EDA	On-Chip Monitoring
	System-in-Package Designs	Analog EDA	Test Data Mining and Learning
		EDA for Microfluidic Biochips	Test Standards

The length of the submitted paper must be 2-4 pages. The submission should also include an 80-100 word abstract. VLSI-DAT adopts the Double Bind Review process. Please do not reveal your name and/or affiliation anywhere in the submitted manuscript for the first paper submission.

Deadlines:

Prospective authors must submit a self-contained paper with figures and tables electronically through the conference website by **October 19, 2018**.

Notification of acceptance - Dec 28, 2018

Final Paper Submission Deadline - Jan 31, 2019

Author Registration Deadline - Feb 28, 2019

[CLICK HERE FOR MORE INFORMATION](#)

2019 IEEE CICC - Call for Papers

2019 Custom Integrated Circuits Conference (CICC)

The 2019 Custom Integrated Circuits Conference (CICC) will be held in Austin, Texas - April 14- 17, 2019.

Submission of original unpublished work is being solicited in the following areas:

- **Analog Circuits and Techniques** for areas such as communications, biomedical, aerospace, automotive, energy, environment, analog computing and security applications, ranging from building blocks to silicon sensors, interfaces, and novel clock generation architectures.
- **Power Management** circuits and design techniques including DC-DC converters, control and management circuits, linear regulators, wireless power transfer, and other methods for improvements in overall system efficiency and performance.
- **Data Converters** including ADCs, DACs, time-to-digital converters, digital-to-time converters, and frequency-to-digital converters of all types enabled by new techniques, architectures, or technologies.
- **Wireless Transceivers and RF/mm-Wave Circuits and Systems** for low-power, energy-efficient and high performance wireless links, biomedical and sensing networks, IoT applications, cellular connectivity including M2M applications (LTE-M, NB-IoT), emerging broadband and MIMO networks (5G, WLAN), vehicle-to-vehicle (V2V), millimeter-wave & THz systems (radar, sensing and imaging), frequency synthesis and LO generation.
- **Wireline and Optical Communications Circuits and Systems** for electrical and optical communications, including serial links for intra-chip and chip-to-chip interconnections, high-speed memory and graphics interfaces, backplanes, long-haul, and power line communications; novel I/O circuits for advancing data rates, improving power efficiency, and supporting extended voltage applications; clocking techniques including PLLs and CDRs; components such as equalizers, high-speed ADC-RX/DAC-TX, silicon photonic and optical interface circuitry.

Design Foundations

- High-level system modeling, digital design infrastructure, and mixed-mode (analog-digital) verification for complex SoCs. Novel digital architectures for emerging applications. Design methodologies for functional safety.
- Modeling and simulation of advanced CMOS and power devices to improve design quality, efficiency, and reliability. Design methodologies for emerging applications (deep learning, automobile, IoT, security), and design for manufacture, test, aging and reliability (novel DFT circuits, system-level testing).

Emerging Technologies, Systems, and Applications

Emerging technologies solicit hardware focused papers in the technologies of tomorrow extending from new device and memory technology to system integration, applications and packaging with focus on, but not limited to:

- **Hardware-based artificial intelligence and security.** Hardware designs for emerging algorithms, hardware security, hardware- and energy-efficient artificial intelligence, machine learning, neural networks, deep learning accelerators. Applications include autonomous transportation and cloud computing.
- **Next-generation devices, technology, integration and packaging** including nano-primitives, non-silicon based technology, MEMS, emerging memories, non-traditional circuits, mm-wave/THz passives and integration, flexible, printed, large-area and organic electronics. system in package, 2.5D, 3D and monolithic 3DIC, multi-die heterogeneous integration, silicon photonic interconnects and packaging, advanced assembly and bonding, embedded cooling technologies,
- **Biomedical circuits, systems, and applications** including neural interfaces, microarrays, lab-on-a-chip, bio-inspired circuits, implantable and/or wearable systems, closed-loop systems with sensing and actuation, medical imaging, and other biosensors including biomedical signal processing SoCs.

Papers can be 3-4 pages in length, be camera-ready, and submitted electronically in PDF format using the [CICC website](#). Double-blind review will be adopted this year. Please follow the instructions given at the submission website to submit a blind version for review and a complete version for publication.

Deadlines:

Deadline for submission of technical papers in November 5, 2018. Authors of accepted papers will be notified via email by January 16, 2019. Top-rated papers will be invited to a special issue of the IEEE Journal of Solid-State Circuits.

For more information on paper submission, please visit the conference website - www.ieee-cicc.org.

PUBLICATIONS

Effective October 1, 2018 : Mandatory Overlength Page Charges for IEEE Journal of Solid-State Circuits

The IEEE Solid-State Circuits Society Board has decided to implement overlength page charges in order to maintain the competitive and financial health of the IEEE Journal of Solid-State Circuits. The continued success of the journal serves our technical community and keeps our flagship publications competitive within the IEEE family.

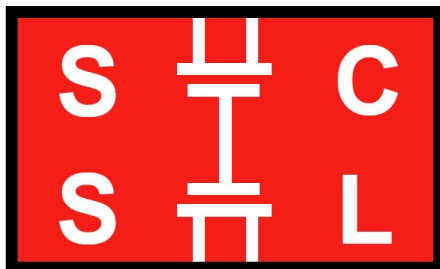
Starting October 1, 2018, the SSCS is implementing mandatory overlength page charges for the J-SSC. If a manuscript exceeds ten pages in length, overlength charges are applied beginning at the 11th page. Charges are assessed when galley proofs are prepared, which is the last step before final publication in the Journal. The page count does not include references or author biographies. However, an overlength charge will be applied if text other than references or author biographies is included on a reference/biography page. The rate for overlength submissions is \$185 per page.

This policy applies only to the J-SSC, and does not apply to Solid-State Circuits Letters (L-SSC), or other SSCS publications (e.g., SSC Magazine).

The SSCS policy on page limits is strictly enforced. Payment for overlength pages - if any - must be received at the time galley proofs are approved and submitted by the author. SSCS values its authors, members, and volunteers. This policy protects your body of work and ensures the sustainability of the J-SSC for the future.

For more information on IEEE Overlength Length Page Charges, [click here](#).

The latest in SSCS Flagship Publications...



IEEE Solid-State Circuits Letters

Volume 1, Issue 4, April 2018

[A Subranging-Based Nonuniform Sampling ADC With Sampling Event Filtering](#)
Tzu-Fan Wu ; Mike Shuo-Wei Chen

[A Wide-Tuning-Range Low-Phase-Noise mm-Wave CMOS VCO With Switchable Transformer-Based Tank](#)

Milad Haghi Kashani ; Amirahmad Tarkeshdouz ; Reza Molavi ; Ehsan Afshari ; Shahriar Mirabbasi

[A 0.083-mm225.2-to-29.5 GHz Multi-LC-Tank Class-F234VCO With a 189.6-dBc/Hz FOM](#)
Hao Guo ; Yong Chen ; Pui-In Mak ; Rui P. Martins

<p><u>Measurement and Analysis of Input-Signal Dependent Flicker Noise Modulation in Chopper Stabilized Instrumentation Amplifier</u> Hyunsoo Ha ; Chris Van Hoof ; Nick Van Helleputte</p>
<p><u>A ± 12-A High-Side Current Sensor With 25 V Input CM Range and 0.35% Gain Error From 40 °C to 85 °C</u> Long Xu ; Saleh Heidary Shalmany ; Johan H. Huijsing ; Kofi A. A. Makinwa</p>
<p><u>An Accurate dB-Linear CMOS VGA Based on Double Duplicate Biasing Technique</u> Xiong Song ; Zheng Hao Lu ; Xiao Peng Yu</p>
<p><u>A 91-GHz Fundamental VCO With 6.1% DC-to-RF Efficiency and 4.5 dBm Output Power in 0.13-μm CMOS</u> Amirahmad Tarkeshdouz ; Ali Mostajeran ; Shahriar Mirabbasi ; Ehsan Afshari</p>



IEEE Journal of Solid-State Circuits

Vol. 53, Issue 9, September 2018

<p><u>Introduction to the Special Section on the 2017 IEEE BCTM and IEEE CSICS Conferences</u> Hua Wang ; Shahriar Shahramian</p>
<p><u>A 61-GHz SiGe Transceiver Frontend for Energy and Data Transmission of Passive RFID Single-Chip Tags With Integrated Antennas</u> Christian Bredendiek ; Dominic A. Funke ; Jan Schöpfel ; Victoria Kloubert ; Benedikt Welp ; Klaus Aufinger ; Nils Pohl</p>
<p><u>A Multi-Phase Coupled Oscillator Using Inductive Resonant Coupling and Modified Dual-Tank Techniques</u> Rong Jiang ; Hossein Noori ; Fa Foster Dai</p>
<p><u>D-Band Frequency Quadruplers in BiCMOS Technology</u> Maciej Kucharski ; Mohamed Hussein Eissa ; Andrea Malignaggi ; Defu Wang ; Herman Jalli Ng ; Dietmar Kissinger</p>
<p><u>Design Considerations for a 100 Gbit/s SiGe-BiCMOS Power Multiplexer With 2Vpp Differential Voltage Swing</u> Christopher Uhl ; Horst Hettrich ; Michael Möller</p>
<p><u>A Fully Decoupled LCTank VCO Topology for Amplitude Boosted Low Phase Noise Operation</u> Bodhisatwa Sadhu ; Tejasvi Anand ; Scott K. Reynolds</p>
<p><u>A Capacitively Coupled, Pseudo Return-to-Zero Input, Latched-Bias Data Receiver</u> Brandon L. Mathieu ; Jamin J. McCue ; Lucas Duncan ; Brian Dupaix ; Hossein Miri Lavasani ; Waleed Khalil</p>
<p><u>Fully Integrated 94-GHz Dual-Polarized TX and RX Phased Array Chipset in SiGe BiCMOS Operating up to 105 °C</u> Wooram Lee ; Jean-Olivier Plouchart ; Caglar Ozdag ; Yigit Aydogan ; Mark</p>

Yeck ; Alper Cabuk ; Asim Kepkep ; Scott K. Reynolds ; Emre Apaydin ; Alberto Valdes-Garcia
<u>Wideband 240-GHz Transmitter and Receiver in BiCMOS Technology With 25-Gbit/s Data Rate</u> Mohamed Hussein Eissa ; Andrea Malignaggi ; Ruoyu Wang ; Mohamed Elkhouly ; Klaus Schmalz ; Ahmet Cagri Ulusoy ; Dietmar Kissinger
<u>Simultaneously Broadband and Back-Off Efficient mm-Wave PAs: A Multi-Port Network Synthesis Approach</u> Chandrakanth Reddy Chappidi ; Xue Wu ; Kaushik Sengupta
<u>E-Band Multi-Phase LC Oscillators With Rotated-Phase-Tuning Using Implicit Phase Shifters</u> Liang Wu ; Quan Xue
<u>A 0.5-V 1.6-mW 2.4-GHz Fractional-N All-Digital PLL for Bluetooth LE With PVT-Insensitive TDC Using Switched-Capacitor Doubler in 28-nm CMOS</u> Naser Pourmousavian ; Feng-Wei Kuo ; Teerachot Siriburanon ; Masoud Babaie ; Robert Bogdan Staszewski
<u>A Time-Interleaved 12-b 270-MS/s SAR ADC With Virtual-Timing-Reference Timing-Skew Calibration Scheme</u> Hyun-Wook Kang ; Hyeok-Ki Hong ; Wan Kim ; Seung-Tak Ryu
<u>A 0.44-fJ/Conversion-Step 11-Bit 600-kS/s SAR ADC With Semi-Resting DAC</u> Sung-En Hsieh ; Chih-Cheng Hsieh
<u>A 0.006 mm² 1.2uW Analog-to-Time Converter for Asynchronous Bio-Sensors</u> Lieuwe B. Leene ; Timothy G. Constandinou
<u>Super Class-AB Recycling Folded Cascode OTA</u> M. Pilar Garde ; Antonio Lopez-Martin ; Ramón Gonzalez Carvajal ; Jaime Ramírez-Angulo
<u>A Regulation-Free Sub-0.5-V 16-/24-MHz Crystal Oscillator With 14.2-nJ Startup Energy and 31.8-fJ/W Steady-State Power</u> Ka-Meng Lei ; Pui-In Mak ; Man-Kay Law ; Rui P. Martins
<u>A Sub-0.1°/h Bias-Instability Split-Mode MEMS Gyroscope With CMOS Readout Circuit</u> Yang Zhao ; Jian Zhao ; Xi Wang ; Guo Ming Xia ; Qin Shi ; An Ping Qiu ; Yong Ping Xu
<u>Single Photon-Counting Pixel Readout Chip Operating Up to 1.2 Gcps/mm² for Digital X-Ray Imaging Systems</u> Rafal Kleczek ; Pawel Grybos ; Robert Szczygiel ; Piotr Maj
<u>A Fully Integrated Buck Regulator With 2-GHz Resonant Switching for Low-Power Applications</u> Tianyu Jia ; Jie Gu
<u>An External Capacitorless Low-Dropout Regulator With High PSR at All Frequencies From 10 kHz to 1 GHz Using an Adaptive Supply-Ripple Cancellation Technique</u> Younghyun Lim ; Jeonghyun Lee ; Suneui Park ; Yongwoo Jo ; Jaehyouk Choi
<u>A4x45Gb/s Two-Tap FFE VCSEL Driver in 14-nm FinFET CMOS Suitable for Burst Mode Operation</u> Mohammad Mahdi Khafaji ; Guido Belfiore ; Jan Pliva ; Ronny Henker ; Frank Ellinger
<u>Loop Gain Adaptation for Optimum Jitter Tolerance in Digital CDRs</u> Joshua Liang ; Ali Sheikholeslami ; Hirotaka Tamura ; Yuuki Ogata ; Hisakatsu Yamaguchi
<u>CMOS Optical PUFs Using Noise-Immune Process-Sensitive Photonic Crystals Incorporating Passive Variations for Robustness</u> Xuyang Lu ; Lingyu Hong ; Kaushik Sengupta
<u>DNN Engine: A 28-nm Timing-Error Tolerant Sparse Deep Neural Network</u>

Processor for IoT Applications

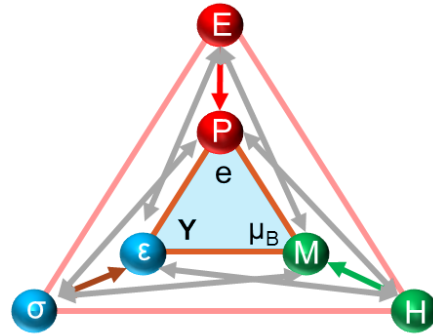
Paul N. Whatmough ; Sae Kyu Lee ; David Brooks ; Gu-Yeon Wei

Corrections to "Split-Array, C-2C Switched-Capacitor Power Amplifiers"

Zhidong Bai ; Ali Azam ; Dallas Johnson ; Wen Yuan ; Jeffrey S. Walling

Errata for "Design and Analysis of a Programmable Receiver Front End Based on Baseband Analog-FIR Filtering Using an LPTV Resistor"

Sameed Hameed ; Sudhakar Pamarti

IEEE Journal on Exploratory Solid-State Computational Devices and Circuits**Volume 4****Towards a Strong Spin-Orbit Coupling Magnetoelectric Transistor**

Peter A. Dowben ; Christian Binek ; Kai Zhang ; Lu Wang ; Wai-Ning Mei ; Jonathan P. Bird ; Uttam Singiseti ; Xia Hong ; Kang L. Wang ; Dmitri Nikonov

Using Programmable Graphene Channels as Weights in Spin-Diffusive Neuromorphic Computing

Jiaxi Hu ; Gordon Stecklein ; Yoska Anugrah ; Paul A. Crowell ; Steven J. Koester

BCB Evaluation of High-Performance and Low-Leakage Three-Independent-Gate Field Effect Transistors

Jorge Romero-Gonzalez ; Pierre-Emmanuel Gaillardon

Tunnel FET Analog Benchmarking and Circuit Design

Hao Lu ; Paolo Paletti ; Wenjun Li ; Patrick Fay ; Trond Ytterdal ; Alan Seabaugh

Improving Energy Efficiency of Low Voltage Logic by Technology-Driven Design

Kaushik Vaidyanathan ; Daniel H. Morris ; Uygur E. Avci ; Huichu Liu ; Tanay Karnik ; Hong Wang ; Ian A. Young

Inversion Charge Boost and Transient Steep-Slope Induced by Free-Charge-Polarization Mismatch in a Ferroelectric-Metal-Oxide-Semiconductor Capacitor

Sou-Chi Chang ; Uygur E. Avci ; Dmitri E. Nikonov ; Ian A. Young

JxCDC papers listed in order of popularity can be found online [HERE](#).For paper submission details, click [HERE](#).**Seeking News**

Please send any chapter news or happenings (Distinguished Lecturer visits, events hosted by your SSCS chapter, awards received by members, etc) to Abira Sengupta, SSCS Magazine News Editor, for inclusion in an upcoming issue of the magazine. Please email - Abira.Sengupta@ieee.org. We look forward to receiving your news articles!

For more chapter news, [check out](#) the **Summer 2018 issue of the Solid-State Circuits Magazine**.

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