Continuous-Time Pipelined ADC for Wide-Bandwidth Wireless Receivers

Presenter: Hajime Shibata
Friday, November 20, 2020
11:00 AM EST

ABSTRACT:
The design space of analog-to-digital converters (ADC) can be classified by two orthogonal axes - one representing the different ADC architectures such as SAR, pipeline, and ΔΣ; the other mapping the underlying circuits as discrete-time and continuous-time configurations. For ΔΣ ADCs, both discrete- and continuous-time design topologies have been explored extensively. With continuous-time implementations excelling in power efficiency and bandwidth, continuous-time ΔΣ ADCs have been widely used in a variety of applications including wireless communication systems. One then might ask - if continuous-time ΔΣ ADCs offer multiple key benefits over discrete-time counterparts, does the same rationale apply to other ADC architectures such as pipelined ADCs? This webinar attempts to answer this question. We first present how a continuous-time pipelined ADC can be derived from a discrete-time equivalent. We then cover the pros and cons of the continuous-time pipelined ADC against discrete-time pipelined and continuous-time ΔΣ ADCs. We also present the implementation examples in 28nm and 16nm CMOS technologies. We will conclude the talk with a discussion of future research directions.
BIOGRAPHY
Hajime Shibata (S'99-M'02-SM'19) received B.E. and M.E. degrees in electrical engineering from the University of Electro-Communications, Tokyo, Japan, in 1997 and 1999, respectively, and the Ph.D. degree from Tokyo Institute of Technology in 2002. Since 2002, he has been with Analog Devices, where he has been working on continuous-time ΔΣ and continuous-time pipelined analog-to-digital converter designs. Dr. Shibata was a co-recipient of the Beatrice Winner Award at ISSCC 2006. He has served as an Associate Editor of IEEE Transactions on Circuits and Systems II from 2017 to 2019.

NEWS

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Webinars for Young Excellence (WYE) Program Presents

Do's and Don'ts of Writing a Good Paper -- Recommendations from a former Editor in Chief

Presenter: Bram Nauta
Friday, November 13, 2020
10:30 AM EST
Abstract:
Congratulations! Your chip finally works and now you want to write a paper about it. Now you wonder, "Where to start? What will be my title? Shall I put a lot of measured numbers in the title, or make it fancy marketing style? What should the introduction be about? What should I present as measurements? Which numbers are important to show? How to compare to state of art?" These are questions that arise when writing your paper. And when finally done, it comes back with a lot of reviewer's comments. Some are mild while some may trash your hard work below ground level. How to deal with that? How can you smoothly bend the critics to something positive in your paper? And if the reviewer did not understand what you actually meant to say, what can you do to fix this? How to understand the viewpoints of the reviewers?
This lecture is about the Do's and Don'ts of writing a paper with focus on the IEEE Solid-State Circuits Society's publications. Also, there will be room for questions & discussions.

About the speaker:
Professor Bram Nauta leads the IC Design group at the university of Twente, Enschede, The Netherlands. Has been the editor in chief of IEEE Journal of solid-state circuits (2007-2010). Moreover, he was active in the technical program committees of various SSCS conferences like ESSCIRC, VLSI Symposium on Circuits, ESSCIRC and ISSCC. For the latter conference he served as technical program committee chair in 2013. Bram also served as the president of the IEEE Solid-State Circuits Society (2018-2019). In his various roles he has experienced most sides of the publication process.

Register Today

Webinar Available on the SSCS YouTube Channel

ABSTRACT:
In the past year, the outbreak of COVID-19 has affected many lives globally. The suboptimal response to the pandemic revealed systematic deficiencies and gaps in our modern healthcare system. One specific area with consequential shortcomings was the diagnosis of infection and the pathogen, particularly the absence (or delayed deployment) of precision tests where and when needed. In this talk, we will discuss and review highly customized IC technologies, broadly defined, that have the potential to address this unmet need, specifically integrated biosensors and CMOS biochip systems. First, we will review the system-level requirements of molecular diagnostics (MDx) systems and explain how they identify the unique DNA/RNA sequences of the pathogen (e.g., COVID-19 one-hour PCR test) to detect infections while achieving appropriate clinical specificity and selectivity. Next, we will discuss in detail methods by which we can design and implement MDx sensors using IC technologies. We will provide specific examples, tradeoff analysis, and manufacturing options for realizing a true CMOS MDx biochip. At the end, we will list key challenges and potential opportunities in this field.
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<table>
<thead>
<tr>
<th>SSCS Central Illinois Chapter Virtual DL - Dr. Keith Bowman</th>
<th>Talk Title: Adaptive and Resilient Circuits for Processors</th>
<th>VIRTUAL - [Click here for more information]</th>
</tr>
</thead>
<tbody>
<tr>
<td>11/09/2020</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
CONFERENCES

Upcoming 2020 SSCS-Sponsored Conferences

<table>
<thead>
<tr>
<th>Conference</th>
<th>Date/Location</th>
</tr>
</thead>
<tbody>
<tr>
<td>2020 European Solid-State Circuits Conference/2020 European Solid-State Device Research Conference</td>
<td>Rescheduled to September 2021. Grenoble, France</td>
</tr>
<tr>
<td>2020 IEEE Biomedical Circuits and Systems Conference (BioCAS)</td>
<td>Rescheduled for October 2021. Berlin, Germany</td>
</tr>
</tbody>
</table>

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- 2019 IEEE Custom Integrated Circuits Conference (CICC)
- 2019 IEEE Symposium on VLSI Circuits
- 2019 IEEE 45th European Solid-State Circuits Conference (ESSCIRC)

2020
- 2020 IEEE International Solid-State Circuits Conference (ISSCC)
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Technical Session Papers:
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Industry Session Papers:
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IEEE Journal of Solid-State Circuits
Vol. 55, Issue 11, November 2020

An Energy-Efficient Time-Domain Incremental Zoom Capacitance-to-Digital Converter
Xiyuan Tang; Shaolan Li; Xiangxing Yang; Linxiao Shen; Wenda Zhao; Randall P. Williams; Jiaxin Liu; Zhichao Tan; Neal A. Hall; David Z. Pan; Nan Sun

Breaking the Performance Tradeoffs in N-Path Mixer-First Receivers Using a Second-Order Baseband Noise-Canceling TIA
Prateek Kumar Sharma; Nagarjuna Nallam

A Low-Power VGA Vision Sensor With Embedded Event Detection for Outdoor Edge Applications
Yu Zou; Massimo Gottardi; Michela Lecca; Matteo Perenzoni

A 5.2-Mpixel 88.4-dB DR 12-in CMOS X-Ray Detector With 16-bit Column-Parallel Continuous-Time Incremental ΔΣ ADCs
Sangwoo Lee; Jinwoong Jeong; Taewoong Kim; Chanmin Park; Taewoo Kim; Youngcheol Chae
<table>
<thead>
<tr>
<th>Title</th>
<th>Authors</th>
</tr>
</thead>
<tbody>
<tr>
<td>A Batteryless Motion-Adaptive Heartbeat Detection System-on-Chip Powered by Human Body Heat</td>
<td>Soumya Bose; Boyu Shen; Matthew L. Johnston</td>
</tr>
<tr>
<td>A 7-bit 900-MS/s 2-Then-3-bit/cycle SAR ADC With Background Offset Calibration</td>
<td>Dengquan Li; Zhangming Zhu; Jiaxin Liu; Haoyu Zhuang; Yintang Yang; Nan Sun</td>
</tr>
<tr>
<td>Indirect Time-of-Flight CMOS Image Sensor With On-Chip Background Light Cancelling and Pseudo-Four-Tap/Two-Tap Hybrid Imaging for Motion Artifact Suppression</td>
<td>Donguk Kim; Seunghyun Lee; Dahwan Park; Canxing Piao; Jihoon Park; Yeonsoo Ahn; Kihwan Cho; Jungsoon Shin; Seung Min Song; Seong-Jin Kim; Jung-Hoon Chun; Jaehyuk Choi</td>
</tr>
<tr>
<td>Design and Analysis of a Sample-and-Hold CMOS Electrochemical Sensor for Aptamer-Based Therapeutic Drug Monitoring</td>
<td>Jun-Chau Chien; Sam W. Baker; H. Tom Soh; Amin Arbabian</td>
</tr>
<tr>
<td>Integrated Self-Adaptive and Power-Scalable Wideband Interference Cancellation for Full-Duplex MIMO Wireless</td>
<td>Yuhe Cao; Jin Zhou</td>
</tr>
<tr>
<td>A 0.58-to-0.9-V Input 0.53-V Output 2.4-μW Current-Feedback Low-Dropout Regulator With 99.8% Current Efficiency</td>
<td>Ziyu Wang; Shahriar Mirabbasi</td>
</tr>
<tr>
<td>A Cryogenic CMOS Parametric Amplifier</td>
<td>Mohammadreza Mehrpoo; Fabio Sebastianio; Edoardo Charbon; Masoud Babaie</td>
</tr>
<tr>
<td>A 117-dB In-Band CMRR 98.5-dB SNR Capacitance-to-Digital Converter for Sub-nm Displacement Sensing With an Electrically Floating Target</td>
<td>Hui Jiang; Samira Amani; Johan G. Vogel; Saleh Heidary Shalmany; Stoyan Nhtianov</td>
</tr>
<tr>
<td>A 2.6 TOPS/W 16-Bit Fixed-Point Convolutional Neural Network Learning Processor in 65-nm CMOS</td>
<td>Shihui Yin; Jae-Sun Seo</td>
</tr>
<tr>
<td>A 1-V 8.1-μW PPG-Recording Front-End With &gt; 92-dB DR Using Light-to-Digital Conversion With Signal-Aware DC Subtraction and Ambient Light Removal</td>
<td>Fatemeh Marefat; Reza Erfani; Pedram Mohseni</td>
</tr>
<tr>
<td>Novel Pulse-Based Analog Divider With Digital Output</td>
<td>Kuan-Hung Chen; Tse-An Chen; Chia-Ling Wei</td>
</tr>
<tr>
<td>Secondary Side-Channel Wireline Communication Using Transmitter Clock Frequency Modulation</td>
<td>Yi Fan Zhang; Joshua Liang; Shayan Shahrmanian; Behzad Dehlaghi; Ryan Bespalko; Michael O'Farrel; Dustin Dunwell; Davide Tonietto; Anthony Chan Carusone</td>
</tr>
<tr>
<td>A Coarse-Fine VCO-ADC for MEMS Microphones With Sampling Synchronization by Data Scrambling</td>
<td>Andres Quintero; Cesare Buffa; Carlos Perez; Fernando Cardes; Dietmar</td>
</tr>
</tbody>
</table>
Bangang Liu ; Yuncheng Zhang ; Junjun Qiu ; Hongye Huang ; Zheng Sun ; Dingxin Xu ; Haosheng Zhang ; Yun Wang ; Jian Pang ; Zheng Li ; Xi Fu ; Atsushi Shirane ; Hitoshi Kurosu ; Yoshinori Nakane ; Shunichiro Masaki ; Kenichi Okada

A 3.2-GHz Quadrature Error Corrector for DRAM Transmitters, Using Replica Serializers and Pulse-Shrinking Delay Lines
Hyeongjun Ko ; Changho Hyun ; Joo-Hyung Chae ; Gi-Moon Hong ; Suhwan Kim

Design and Packaging of a Robust 120-GHz OOK Receiver Used in a Short-Range Dielectric Fiber Link
Simon Ooms ; Patrick Reynaert

610-GHz Fourth Harmonic Signal Reactively Generated in a CMOS Voltage Controlled Oscillator Using Differentially Pumped Varactors
Zhe Chen ; Zhiyu Chen ; Wooyeol Choi ; Kenneth K. O

An Implantable Body Channel Communication System With 3.7-pJ/b Reception and 34-pJ/b Transmission Efficiencies
Beomjin Yuk ; Byeongseol Kim ; Sanggeon Park ; Yeewool Huh ; Joonsung Bae

Design of a Boost DC-DC Converter With 82-mV Startup Voltage and Fully Built-in Startup Circuits for Harvesting Thermoelectric Energy
Jhe-Jia Jhang ; Hung-Hsien Wu ; Tien Hsu ; Chia-Ling Wei

A 2T-MONOS Embedded Flash Macro With 65-nm SOTB Technology Achieving 0.15-pJ/bit Read Energy With 80-MHz Access for IoT Applications
Ken Matsubara ; Tsutomu Nagasawa ; Yoshinobu Kaneda ; Hidenori Mitani ; Takashi Iwase ; Yasunobu Aoki ; Kohei Hashimoto ; Toshiaki Morioka ; Keiichi Maekawa ; Takashi Ito ; Hiroyuki Kondo ; Takashi Kono

IEEE Journal on Exploratory Solid-State Computational Devices and Circuits

Volume 6: 2020 - June

Hybrid-Phase-Transition FET Devices for Logic Computation
Manuel Jiménez ; Juan Núñez ; María José Avedillo

Benchmarking and Optimization of Spintronic Memory Arrays
Yu-Ching Liao ; Chenyun Pan ; Azad Naeemi

Special Topic on Exploratory Devices and Circuits for Compute-in-Memory
Shimeng Yu

Accurate Inference With Inaccurate RRAM Devices: A Joint Algorithm-Design Solution
Gouranga Charan ; Abinash Mohanty ; Xiaocong Du ; Gokul Krishnan ; Rajiv V. Joshi ; Yu Cao

Early Access Articles

Accurate Inference with Inaccurate RRAM Devices: A Joint Algorithm-Design Solution
Gouranga Charan ; Abinash Mohanty ; Xiaocong Du ; Gokul Krishnan ; Rajiv V. Joshi ; Yu Cao

A DNA Read Alignment Accelerator based on Computational RAM
Zamshed I. Chowdhury ; Masoud Zabihi ; S. Karen Khatamifard ; Zhengyang Zhao ; Salonik Resch ; Meisam Razaviyayn ; Jian-Ping Wang ; Sachin S. Sapatnekar ; Ulya R. Karpuzcu
Analyzing the Effects of Interconnect Parasitics in the STT CRAM In-memory Computational Platform
Masoud Zabihi; Arvind K. Sharma; Meghna G. Mankalale; Zamsheed I. Chowdhury; Zhengyang Zhao; Salonik Resch; Ulya R. Karpuzcu; Jian-Ping Wang; Sachin S. Sapatnekar

Short-Term Long-Term Compute-In-Memory Architecture: A Hybrid Spin/CMOS Approach Supporting Intrinsic Consolidation
Shadi Sheikhfaal; Ronald F. DeMara

Energy-Efficient Moderate Precision Time-Domain Mixed-Signal Vector-by-Matrix Multiplier Exploiting 1T-1R Arrays
Shubham Sahay; Mohammad Bavandpour; Mohammad Reza Mahmoodi; Dmitri Strukov

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