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IEEE SOLID-STATE CIRCUITS SOCIETY
Where ICs are in IEEE

October 2018

NEWS

UPCOMING WEBINAR

"Neuroengineering the Next Decade"
Presented by Dejan Marković
November 21, 2018 at 11:00 AM ET

CLICK HERE TO REGISTER

Abstract: Brain disease is a growing socioeconomic problem. In the US, chronic pain affects over 100 million people, with over $600B annual cost; Alzheimer's disease affects 5.4 million people, with the cost of care exceeding sales of Google; another 5 million live with long-term disability as a result of traumatic brain injury, and there are millions with epilepsy. Drug therapy has failed. The development of neuromodulation technology has become a major medical and social priority.
While much progress has been made in generating brain-machine interface and restoring limb movement, it is much more difficult to restore memories,

especially declarative memories, or treat network-scale neuropsychiatric indications. Fueled by insights from clinical neuroscience and engineering, I will discuss a leading-edge technology that can make the fulfillment of memory restoration and the treatment of neuropsychiatric symptoms highly likely.

Bio: Dejan Marković is a Professor of Electrical and Computer Engineering at the University of California, Los Angeles. He is also affiliated with UCLA Bioengineering Department, Neuroengineering field. He completed the Ph.D. degree in 2006 at the University of California, Berkeley, for which he was awarded 2007 David J. Sakrison Memorial Prize. His current research is focused on implantable neuromodulation systems, domain-specific compute architectures, embedded systems, and design methodologies. Dr. Marković co-founded Flex Logix Technologies, a semiconductor IP startup, in 2014. He received an NSF CAREER Award in 2009. In 2010, he was a co-recipient of ISSCC Jack Raper Award for Outstanding Technology Directions. Most recently, he received 2014 ISSCC Lewis Winner Award for Outstanding Paper.

Learn if Blockchain Can Rescue the Stalled IoT-and More!

Blockchain is poised to be the greatest IT disrupter since the internet, disrupting IT networks in a variety of industries. Learn more about the future of blockchain in IoT, energy, healthcare, supply chain and finance at Advanced Blockchain for Enterprise.

This two one-hour virtual event will take place from 12:00PM-1:00PM ET on 4 and 5 December 2018, and will cover advanced blockchain concepts and innovative applications for managers, engineers and leaders. Secure your spot today and as an SSCS member you save US$50 off the US$295 registration!

Click here to register!

2019 ISSCC Student Travel Grants & Women in Circuits Travel Grants

The IEEE Solid-State Circuits Society Student Travel Grant Award (STGA) program recognizes and promotes early career accomplishments in all solid-state circuits fields by supporting student travel to SSCS-sponsored conferences.

With the help of the STGA program, up-and-coming young engineers may network with researchers from industry, academia, and government from all over the world and learn about IC design breakthroughs and about challenges that have not yet been solved or need to be addressed, in-person and in-advance.

The 2019 ISSCC Student Travel Grant Awards (STGA's) application submission is now open.

Applicants must meet the following requirements:

- Applications MUST be IEEE Solid-State Circuits Society members
- Students MUST be enrolled - for at least one year - in a PhD program and be recommended by one professor

Note - A dissertation topic does not need to be selected

Please note the Society, in conjunction with our Women in Circuits program, is pleased to include a new provision to the STGA selection process. A portion of our STGA's will be earmarked to be awarded to those members whose selection would assist SSCS in its ongoing efforts to support the number of women involved in our field of interest, industry, and academia as part of the Society's diversity and inclusion efforts in growing and serving our membership.

Click here to access and application and directions

Questions? Email Lauren Caruso at l.caruso@ieee.org.

2018 - 2019 SSCS Student Sweatshirt Design Contest

The winning design will be made into a sweatshirt and distributed to all SSCS Student & Graduate Student Members at ISSCC 2019.

This year's theme is line with the 2019 IEEE International Solid-State Circuits Conference Theme - "Envisioning the Future".

Your task: Design a sweatshirt that shows the future of solid-state circuits. Your design should illustrate how you envision the future of solid-state circuits and systems.

This contest is open only to IEEE SSCS Student and Graduate Student Members. Valid Member ID will be required for entry submission.

Click here for more information and submission instructions.

UPCOMING SOCIETY-SPONSORED EVENTS

Women in Circuits Bay Area Networking Luncheon

November 9, 2018
12:00 PM - 3:00 PM
IL Fornaio, 520 Cowper Street, Palo Alto, California 94301

Join the second Women in Circuits Bay Area Networking Luncheon. Build and sustain a community among women in circuits. Meet and network with female luminaries in engineering.

Agenda

12:00 PM - Doors open
12:10 PM - Women in Circuits Program Overview by Yildiz Sinangil
12:20 PM -Networking, Mentoring and Advocacy for Women in Circuits by Alice Wang, PsiKick, Senior Director, USA
12:35 PM - Thriving the Corporate Culture - My Story by Yan Li, Senior Fellow, Western Digital, Milpitas, CA
12:50 PM - Remarks by Mojtaba Sharifzadeh, SSCS Silicon Valley Chapter Chair
1:05 PM - Mentoring roundtables
2:30 PM - Concluding remarks

Pricing:
SSCS Member - $20
IEEE Member - $25
Non-Member- $30

This event is non-refundable

CLICK HERE
TO REGISTER

Women in Circuits Luncheon at A-SSCC

Nov. 6, 2018 - 12 PM at Shanghai Pavilion, Shangri-La's Far Eastern Plaza Hotel, Tainan, Taiwan
Speaker: Claire Chen, Director, Power Management BD, TSMC

Please email Ping-Hsuan Hsieh (phsieh@ee.nthu.edu.tw) with any questions.

Click here to RSVP

This event will be first come first serve.

SSCS Micro-Mentoring and Career Session

Nov. 6, 2018 - 17:45 - 18:45 at North Gate, B1F, Shangri-La's Far Eastern Plaza Hotel, Tainan, Taiwan

- Leading experts from industry and academia share their experience and have 1-on-1 mentoring sessions to answers all your questions on publications, entrepreneurship, industry vs. academia, and career coaching.
- Learn about SSCS member benefits for young engineers and students, such as complimentary tutorials and short courses, webinars, distinguished lecturers, networking, student fellowships, and more.
- All student participants receive a 1-year complimentary IEEE SSCS membership with access to all the benefits.

Everybody is welcome to join.

Click here to register

EDUCATION

November 2018 Distinguished Lectures

SSCS/CAS Uttar Pradesh	Energy Efficient Computing in Nanoscale CMOS - Presented by Vivek De	November 3, 2018	Indian Institute of Technology - Roorkee **For more information, please click here**.
SSCS Oregon	Towards Large-Scale Quantum computers: Cryogenic CMOS for Scalable Quantum Computation - Presented by Fabio Sebastiano	November 6, 2018	Intel Corporation **For more information, please click here**.
SSCS/CAS Central Texas	Millimeter-wave MIMO Transceivers for Future Wireless Systems - Presented by Jeyanandh Paramesh	November 8, 2018	University of Texas at Austin **For more information, please click here**.
SSCS Switzerland	Lecture Title TBD - Presented by David Stoppa	November 8, 2018	Switzerland **For more information, please click here**.

SSCS Tainan	Energy-Efficient Inverter-Based Amplifiers - Presented by Youngcheol Chae	November 8, 2018	National Chia Yi University **For more information, please click here**.
SSCS Taipei	On-Chip Epilepsy Detection: Where Machine Learning Meets Wearable, Patient-Specific Seizure Monitoring - Presented by Jerald Yoo	November 8, 2018	Chip Implementation Center, Taiwan **For more information, please click here**.
SSCS Japan & SSCS Kansai	Design Considerations of Digital PLL - Presented by Jae-Yoon Sim	November 13, 2018	University of Tokyo **For more information, please click here**.
SSCS Dallas	Broadband, Linear, and High-Efficiency Mm-Wave Power Amplifiers - The Unreasonable Quest for "Perfect" 5G Mm-Wave Power Amplifiers and Some Reasonable Solutions - Presented by Hua Wang	November 15, 2018	Dallas **For more information, please click here**.
SSCS OSU Student Chapter	A Bidirectional Closed-Loop Brain-Machine Interface - The Next Frontier - Presented by Jan Van der Spiegel	November 15, 2018	Oregon **For more information, please click here**.
SSCS Toronto	Considerations and Implementations For High Data Rate Interconnect - Presented by Daniel Friedman	November 15, 2018	University of Toronto **For more information, please click here**.
SSCS Seoul	Body Area Network - Connecting things together around the body - Presented by Yong Moon	November 16, 2018	Yonsei University **For more information, please click here**.
SSCS/EDS Nanjing	Neural Signal Recording Amplifiers - Presented by Yong Ping Xu	November 20, 2018	Southeast University **For more information, please click here**.
SSCS Tainan	Body Area Network - Connecting things together around the body - Presented by Jerald Yoo	November 22, 2018	National Cheng Kung University **For more information, please click here**.
University of Toronto Distinguished Lecture	Energy-Efficient Edge Computing for AI-	November 22, 2018	University of Toronto

Series	driven Applications - Presented by Vivienne Sze		**For more information, please click here**.
SSCS Chengdu	Continuous-Time Sigma-Delta ADCs for Receiver Applications - Basics, Non-idealities and State of the Art - Presented by Maurits Ortmanns	November 22, 2018	UESTC Shahe Campus **For more information, please click here**.
SSCS Macau	Implantable electronics for highly parallel neural interfaces - Presented by Maurits Ortmanns	November 22, 2018	University of Macau **For more information, please click here**.
SSCS Seoul	Data and Power Telemetry for Implants - Presented by Maurits Ortmanns	November 26, 2018	Korea **For more information, please click here**.
SSCS/CAS Austria	Talk Title TBD - Presented by David Stoppa	November 28, 2018	TU Graz **For more information, please click here**.
SSCS Portugal	Energy Efficient Nyquist-Rate ADCs - Presented by Klass Bult	November 29, 2018	Universidade NOVA de Lisboa **For more information, please click here**.

CONFERENCES

Upcoming Conferences

2018 IEEE Asian Solid-State Circuits Conference (A-SSCC) Tainan, Taiwan	**November 5 - 7, 2018**
2019 IEEE International Solid-State Circuits Conference (ISSCC) San Francisco, CA	**February 17 - 19, 2019**
2019 Design, Automation & Test in Europe Conference and Exhibition Florence, Italy	**March 25 - 29, 2019**
2019 IEEE Custom Integrated Circuits Conference (CICC) Austin, TX	**April 21 - 24, 2019**
2019 IEEE Radio Frequency Integrated Circuits Symposium (RFIC) Boston, MA	**June 2 - 4, 2019**
2019 IEEE Biomedical Circuits and Systems Conference (BioCAS) Nara, Japan	**October 17 - 19, 2019**
2019 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and	**November 3 - 6, 2019**

Technology Symposium (BCICTS) Nashville, TN	

CALL FOR PAPERS

Special Issue on Nonvolatile Memory for Efficient Implementation of Neural/Neuromorphic Computing

IEEE Journal on Exploratory Solid-State Computational Devices and Circuits (JxCDC)

Guest Editor -
Shimeng Yu, Georgia Institute of Technology, shimeng.yu@ece.gatech.edu
Editor-in-Chief -
Ian Young, Intel, ian.young@intel.com

Aims and Scope
In recent years, artificial intelligence based on machine/deep learning has shown significantly improved accuracy in large-scale visual/auditory recognition and classification tasks, some even surpassing human-level accuracy. In particular, deep neural networks (DNN) and their variants have proved their efficacy in a wide range of image, video, speech, and biomedical applications. To achieve incremental accuracy improvement, state-of-the-art deep learning algorithms tend to aggressively increase the depth and size of the network, which imposes ever-increasing computational capacity and storage cost in hardware. Though GPUs are the dominant technology in the training of the DNN models at the cloud, specifically designed ASIC hardware accelerators have been developed to run large-scale deep learning algorithms for inference (or even training) on-chip. This provides opportunities to bring the AI closer to the edge device for applications such as autonomous driving, machine translation, and smart wearable devices, where severe constraints exist in performance, power, and area.

In particular, the silicon CMOS ASIC designs show that limited on-chip memory capacity is the biggest bottle-neck for energy-efficient neural/neuromorphic computing, in terms of storing millions/billions of parameters and loading/communicating them to the place where computing actually occurs.

Today's ASIC designs typically utilize SRAM as the synaptic memory. Although SRAM technology has been following the CMOS scaling trend well, the SRAM density and on-chip SRAM capacity are insufficient for storing the extremely large number of parameters in deep learning algorithms. Leakage current is undesirable, and parallelism is limited due to row-by-row operation in the digital SRAM array. As an alternative hardware platform, non-volatile memory (NVM) devices have been proposed for weight storage with higher density and fast

parallel analog computing with low power consumption. A special subset of NVM devices that show multilevel resistance/conductance states could naturally emulate analog synapses in the neural network. Because NVMs are potentially higher density than SRAM, they could hold most of the weights on-chip, thereby reducing or eleminating the off-chip memory access (i.e. from DRAM). The parallelism of the crossbar arrays for matrix-vector multiplication (or dot product) further enables significant acceleration of core neural computations. NVMs also offers much lower standby leakage, which could be another advantage for smart edge devices.

This special issue of the IEEE Journal on Exploratory Computational Devices and Circuits (JXCDC) aims to call for the recent research progress of the NVM based neuromorphic computing from device-level, array-level up to system-level. The interaction and co-optimization between materials/device engineering and circuit/architecture is solictated.

Topics of Interests

Prospective authors are invited to submit original works and/or extended works based on conference presentations on the topics from a wide range of NVM based neuromorphic computing. Here the NVM devices include but not limit to the following: PCM, RRAM/CBRAM, STT-MRAM (or other spintronic memory), ferroelectric based memory including FeFET or Ferroelectric Tunnel Junction (FTJ), floating-gate or charge-trap transistor, NOR and NAND Flash, etc. The following topics are solicited:

- NVM materials/devices for neurons
- NVM materials/devices for synapses
- Selector materials/devices for crossbar array for analog in-memory computation
- Array-level demonstration for analog in-memory computation
- NVM based inference engine design including peripheral circuitry
- NVM based training accelerator design including peripheral circuitry
- Architectural-level design for processing-in-memory or compute-in-memory with NVM
- Brain-inspired spiking neural networks with NVM
- ·Hardware-aware neuromorphic learning algorithms and architectures
- Benchmarking tools for NVM based hardware accelerator design

Important Dates

Open for Submission: August 1st, 2018
Submission Deadline: December 31st, 2018
First Notification: February 15th, 2019
Revision Submission: March 15th, 2019
Final Decision: April 10th, 2019
Publication Online: May 1st, 2019

Submission Guidelines:

The IEEE Journal on Exploratory Solid-State Computational Devices and Circuits (JXCDC) IS AN OPEN ACCESS ONLY PUBLICATION: Charge for Authors: $1,350 USD per paper. Paper submissions must be done through the ScholarOne Manuscripts website: **https://mc.manuscriptcentral.com/jxcdc** Guidelines for papers and supplementary materials, as well as a paper template, are provided at this website (also on the next page).

Inquiries for the JxCDC Journal should be sent to: JXCDC@IEEE.ORG

2019 IEEE CICC - Call for Papers

2019 Custom Integrated Circuits Conference (CICC)

The 2019 Custom Integrated Circuits Conference (CICC) will be held in Austin, Texas - April 14- 17, 2019.

Submission of original unpublished work is being solicited in the following areas:

- **Analog Circuits and Techniques** for areas such as communications, biomedical, aerospace, automotive, energy, environment, analog computing and security applications, ranging from building blocks to silicon sensors, interfaces, and novel clock generation architectures.
- **Power Management** circuits and design techniques including DC-DC converters, control and management circuits, linear regulators, wireless power transfer, and other methods for improvements in overall system efficiency and performance.
- **Data Converters** including ADCs, DACs, time-to-digital converters, digital-to-time converters, and frequency-to-digital converters of all types enabled by new techniques, architectures, or technologies.
- **Wireless Transceivers and RF/mm-Wave Circuits and Systems** for low-power, energy-efficient and high performance wireless links, biomedical and sensing networks, IoT applications, cellular connectivity including M2M applications (LTE-M, NB-IoT), emerging broadband and MIMO networks (5G, WLAN), vehicle-to-vehicle (V2V), millimeter-wave & THz systems (radar, sensing and imaging), frequency synthesis and LO generation.
- **Wireline and Optical Communications Circuits and Systems** for electrical and optical communications, including serial links for intra-chip and chip-to-chip interconnections, high-speed memory and graphics interfaces, backplanes, long-haul, and power line communications; novel I/O circuits for advancing data rates, improving power efficiency, and supporting extended voltage applications; clocking techniques including PLLs and CDRs; components such as equalizers, high-speed ADC-RX/DAC-TX, silicon photonic and optical interface circuitry.

Design Foundations

- High-level system modeling, digital design infrastructure, and mixed-mode (analog-digital) verification for complex SoCs. Novel digital architectures for emerging applications. Design methodologies for functional safety.
- Modeling and simulation of advanced CMOS and power devices to improve design quality, efficiency, and reliability. Design methodologies for emerging applications (deep learning, automobile, IoT, security), and design for manufacture, test, aging and reliability (novel DFT circuits, system-level testing).

Emerging Technologies, Systems, and Applications

Emerging technologies solicit hardware focused papers in the technologies of tomorrow extending from new device and memory technology to system integration, applications and packaging with focus on, but not limited to:

- **Hardware-based artificial intelligence and security**. Hardware designs for emerging algorithms, hardware security, hardware- and energy-efficient artificial intelligence, machine learning, neural networks, deep learning accelerators. Applications include autonomous transportation and cloud computing.
- **Next-generation devices, technology, integration and packaging** including nano-primitives, non-silicon based technology, MEMS, emerging memories, non-traditional circuits,mm- wave/THz passives and integration, flexible, printed, large-area and organic electronics. system in package, 2.5D, 3D and monolithic 3DIC, multi-die heterogeneous integration, silicon photonic interconnects and packaging, advanced assembly and bonding, embedded cooling technologies,

- **Biomedical circuits, systems, and applications** including neural interfaces, microarrays, lab-on-a-chip, bio-inspired circuits, implantable and/or wearable systems, closed-loop systems with sensing and actuation, medical imaging, and other biosensors including biomedical signal processing SoCs.

Papers can be 3-4 pages in length, be camera-ready, and submitted electronically in PDF format using the CICC website. Double-blind review will be adopted this year. Please follow the instructions given at the submission website to submit a blind version for review and a complete version for publication.

Deadlines:
Deadline for submission of technical papers in **November 5, 2018**. Authors of accepted papers will be notified via email by January 16, 2019. Top-rated papers will be invited to a special issue of the IEEE Journal of Solid-State Circuits.

For more information on paper submission, please visit the conference website - www.ieee-cicc.org.

2019 IEEE Symposia on VLSI Circuits -Call for Papers

The VLSI Symposia is an international conference on semiconductor technology and circuits that offers an opportunity to interact and synergize on topic ranging from process technology to systems-on-chip.

The 2019 Symposia on VLSI Technology and Circuits will be held June 9 - 14 in Kyoto, Japan at the RIHGA Royal Hotel.

The Circuits Symposium is placing special emphasis on several Innovative System focus areas, and encourages paper submissions on:

- Machine and deep learning
- Internet of Things
- Industrial electronics
- Big Data management
- Biomedical Applications
- Robotics and autonomous transportation

New focus sessions comprising invited and contributed papers will be offered.

In addition, submissions are welcomed in all of the following circuits areas:

- Processors, SoCs, and Machine Learning
- Digital circuits, signal integrity, and IOs
- Hardware security
- Memory circuits, architectures, and interfaces
- Biomedical circuits
- Sensors, imagers, and display circuits
- Power conversion circuits
- Analog, amplifier and filter circuits
- Wireless receivers and transmitters
- Data converters
- Frequency generation and clock circuits
- Wireline receivers and transmitters

Call for Workshop - The call for proposals for the Sunday Workshop is now open. You organize the workshop, VLSI provides the venue. Check the details in: **www.vlsisymposium.org**.

Prospective authors must submit two-page camera-ready papers and abstracts using the Symposia's website, **www.vlsisymposium.org**.

Accepted papers will be published as submitted, with no revisions permitted. Authors must follow detailed instructions provided within the "Authors" section of the website, including the Authors' Guide and Pre-publication Policy. Extended versions of selected papers from the Symposium will be published in a Special Issue of the IEEE Journal of Solid-State Circuits.

Paper Submission Deadline is Monday, January 28, 2019 at 23:59 JST.

CALL FOR PAPERS
RFIC 2019: IEEE Radio Frequency Integrated Circuits Symposium

The 2019 IEEE Radio Frequency Integrated Circuits Symposium (RFIC 2019) will be held 2-4 June 2019 at the Boston Convention and Exhibition Center in Boston, MA, USA. For the latest information, please visit: rfic-ieee.org.

Electronic Paper Submission/Communication: Technical papers must be submitted via the RFIC 2019 website at rfic-ieee.org. Hard copies will not be

accepted. Complete information on how and when to submit a paper can be found on the RFIC 2019 website. As in last year, a double-blind review process will be followed.

Technical Areas: The symposium solicits papers describing original work in all areas related to RF and millimeter-wave integrated circuits and systems. Work should be demonstrated through integrated-circuit hardware results.

Original contributions are solicited in areas including but not limited to the following:

- **Wireless Cellular and Connectivity:** innovative circuit and system-on-chip concepts related to wireless applications below 6GHz, including those designed for existing and emerging standards such as 2G/3G/4G/5G (sub-6GHz), LTE, WWAN, WLAN, BT, GPS, FM, and UWB.
- **Low Power Transceivers:** RF circuits designed for extremely low power or harvested-energy operation, wake-up receivers, SOCs designed for operation within emerging RFID, NFC, Zigbee, 802.15.4, WPAN, WBAN, Biomedical, Sensor Nodes, or IR-UWB applications
- **Receiver Components and Circuits:** LNAs, mixers, VGAs, stand-alone phase shifters, T/R switches, integrated FEM, amplifiers, filters, demodulators, for RF through millimeter-wave frequencies
- **Analog and Mixed-Signal Blocks and SOCs:** RF and baseband converters (ADC/DAC), sub-sampling/over-sampling circuits, converters for digital beamforming, converters for emerging TX and RX architectures, power (DC-DC) converters for RF applications, I/O transceivers and CDRs for wireline and optical connectivity
- **Reconfigurable and Tunable Front-Ends:** SDR/cognitive radio, N-path receivers/filters, wideband/multi-band front-ends, interference cancellation, full-duplex, adaptive front-ends
- **Transmitter Sub-Systems and Power Amplifiers:** power amplifiers, drivers, modulators, digital transmitters, advanced TX circuits, linearization and efficiency enhancement techniques, for RF through millimeter-wave frequencies
- **Oscillators:** VCOs, injection-locking frequency dividers/multipliers
- **Frequency Synthesis:** PLLs, DLLs, MDLLS, DDS, LO drivers, frequency dividers
- **Device Technologies, Packaging, Modeling, and Testing:** RF device technology (both silicon and compound semiconductors) MEMS, integrated passives, photonic, reliability, packaging, modeling and testing, EM modeling/co-simulation, built-in-self-test (BIST)
- **Millimeter- and Sub-Millimeter Wave Communication and Sensing Systems:** >20GHz SoCs/SiPs for wireless communication (5G mm-wave, WiGig, 802.11ay), phased-arrays, imaging, radar, spectroscopy, and remote sensing
- **Emerging Circuit Technologies (NEW This Year):** RF circuits and systems incorporating MEMs sensors and actuators, heterogeneous and 3D ICs, silicon photonics, quantum computing ICs, hardware security, and machine learning applications, Wearable systems, Biomedical applications, autonomous systems e.g. automotive and drones Implantable systems

Electronic Submission Deadlines:

Technical Paper in PDF Format - 14 January 2019
Final Manuscripts for the Digest and USB - 22 March 2019

All submissions must be made at **rfic-ieee.org** in PDF form. Hard copies are not accepted.

PUBLICATIONS

Effective October 1, 2018 : Mandatory Overlength Page Charges for IEEE Journal of Solid-State Circuits

The IEEE Solid-State Circuits Society Board has decided to implement overlength page charges in order to maintain the competitive and financial health of the IEEE Journal of Solid-State Circuits. The continued success of the journal serves our technical community and keeps our flagship publications competitive within the IEEE family.

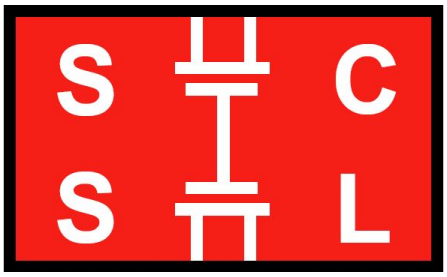
Starting October 1, 2018, the SSCS is implementing mandatory overlength page charges for the J-SSC. If a manuscript exceeds ten pages in length, overlength charges are applied beginning at the 11th page. Charges are assessed when galley proofs are prepared, which is the last step before final publication in the Journal. The page count does not include references or author biographies. However, an overlength charge will be applied if text other than references or author biographies is included on a reference/biography page. The rate for overlength submissions is $185 per page.

This policy applies only to the J-SSC, and does not apply to Solid-State Circuits Letters (L-SSC), or other SSCS publications (e.g., SSC Magazine).

The SSCS policy on page limits is strictly enforced. Payment for overlength pages - if any - must be received at the time galley proofs are approved and submitted by the author.
SSCS values its authors, members, and volunteers. This policy protects your body of work and ensures the sustainability of the J-SSC for the future.

For more information on IEEE Overlength Length Page Charges, **click here**.

The latest in SSCS Flagship Publications...



IEEE Solid-State Circuits Letters

Volume 1, Issue 4, April 2018

A Subranging-Based Nonuniform Sampling ADC With Sampling Event Filtering
Tzu-Fan Wu ; Mike Shuo-Wei Chen

A Wide-Tuning-Range Low-Phase-Noise mm-Wave CMOS VCO With Switchable Transformer-Based Tank **Milad Haghi Kashani ; Amirahmad Tarkeshdouz ; Reza Molavi ; Ehsan Afshari ; Shahriar Mirabbasi**
A 0.083-mm225.2-to-29.5 GHz Multi-LC-Tank Class-F234VCO With a 189.6-dBc/Hz FOM **Hao Guo ; Yong Chen ; Pui-In Mak ; Rui P. Martins**
Measurement and Analysis of Input-Signal Dependent Flicker Noise Modulation in Chopper Stabilized Instrumentation Amplifier **Hyunsoo Ha ; Chris Van Hoof ; Nick Van Helleputte**
A ± 12-A High-Side Current Sensor With 25 V Input CM Range and 0.35% Gain Error From 40 °C to 85 °C **Long Xu ; Saleh Heidary Shalmany ; Johan H. Huijsing ; Kofi A. A. Makinwa**
An Accurate dB-Linear CMOS VGA Based on Double Duplicate Biasing Technique **Xiong Song ; Zheng Hao Lu ; Xiao Peng Yu**
A 91-GHz Fundamental VCO With 6.1% DC-to-RF Efficiency and 4.5 dBm Output Power in 0.13-Î¼m CMOS **Amirahmad Tarkeshdouz ; Ali Mostajeran ; Shahriar Mirabbasi ; Ehsan Afshari**

IEEE Journal of Solid-State Circuits

Vol. 53, Issue 9, October 2018

Introduction to the Special Section on the 2017 Asian Solid-State Circuits Conference (A-SSCC) **Tsung-Hsien Lin ; Chia-Hsiang Yang ; Seung-Tak Ryu**
Dual-Source Energy-Harvesting Interface With Cycle-by-Cycle Source Tracking and Adaptive Peak-Inductor-Current Control **Chi-Wei Liu ; Hui-Hsuan Lee ; Pei-Chun Liao ; Yi-Lun Chen ; Ming-Jie Chung ; Po-Hung Chen**
An 88% Efficiency 0.1-300-uW Energy Harvesting System With 3-D MPPT Using Switch Width Modulation for IoT Smart Nodes **Karim Rawy ; Taegeun Yoo ; Tony Tae-Hyoung Kim**
A 0.5-V 12-bit SAR ADC Using Adaptive Time-Domain Comparator With Noise Optimization **Sung-En Hsieh ; Chen-Che Kao ; Chih-Cheng Hsieh**
A 72.9-dB SNDR 20-MHz BW 2-2 Discrete-Time Resolution-Enhanced Sturdy MASH Delta-Sigma Modulator Using Source-Follower-Based Integrators **Yong-Sik Kwak ; Kang-Il Cho ; Ho-Jin Kim ; Seung-Hoon Lee ; Gil-Cho Ahn**
A 5.35-mW 10-MHz Single-Opamp Third-Order CT Delta Sigma Modulator With CTC Amplifier and Adaptive Latch DAC Driver in 65-nm CMOS **Wei Wang ; Yan Zhu ; Chi-Hang Chan ; Rui Paulo Martins**
An Element-Matched Electromechanical Delta Sigma ADC for Ultrasound

Imaging
Michele D'Urbino ; Chao Chen ; Zhao Chen ; Zu-Yao Chang ; Jacco Ponte ; Boris Lippe ; Michiel Pertijs

A 0.4-V, 0.138-fJ/Cycle Single-Phase-Clocking Redundant-Transition-Free 24T Flip-Flop With Change-Sensing Scheme in 40-nm CMOS
Van Loi Le ; Juhui Li ; Alan Chang ; Tony Tae-Hyoung Kim

A 2.56-mm2 718GOPS Configurable Spiking Convolutional Sparse Coding Accelerator in 40-nm CMOS
Chester Liu ; Sung-Gun Cho ; Zhengya Zhang

Fully Synthesizable PUF Featuring Hysteresis and Temperature Compensation for 3.2% Native BER and 1.02 fJ/b in 40 nm
Sachin Taneja ; Anastacia B. Alvarez ; Massimo Alioto

A 12.8-ns-Latency DDFS MMIC With Frequency, Phase, and Amplitude Modulations in 65-nm CMOS
Abdel Martinez Alonso ; Masaya Miyahara ; Akira Matsuzawa

A 77-GHz Mixed-Mode FMCW Signal Generator Based on Bang-Bang Phase Detector
Jianfu Lin ; Zheng Song ; Nan Qi ; Woogeun Rhee ; Zhihua Wang ; Baoyong Chi

Analog to Sequence Converter-Based PAM-4 Receiver With Built-In Error Correction
Aurangozeb ; Maruf Mohammad ; Masum Hossain

A 2.1-Gb/s 12-Channel Transmitter With Phase Emphasis Embedded Serializer for 55-in UHD Intra-Panel Interface
Jihwan Park ; Joo-Hyung Chae ; Yong-Un Jeong ; Jae-Whan Lee ; Suhwan Kim

Chip-Package-Board Interactive PUF Utilizing Coupled Chaos Oscillators With Inductor
Noriyuki Miura ; Masanori Takahashi ; Kazuki Nagatomo ; Makoto Nagata

A CMOS Time-of-Flight Depth Image Sensor With In-Pixel Background Light Cancellation and Phase Shifting Readout Technique
Tzu-Hsiang Hsu ; Ting Liao ; Nien-An Lee ; Chih-Cheng Hsieh

Dual-Loop Two-Step ZQ Calibration for Dynamic Voltage-Frequency Scaling in LPDDR4 SDRAM
Chang-Kyo Lee ; Junha Lee ; Kiho Kim ; Jin-Seok Heo ; Jin-Hyeok Baek ; Gil-Hoon Cha ; Daesik Moon ; Dong-Hun Lee ; Jong-Wook Park ; Seunseob Lee ; Si-Hyeong Cho ; Young-Ryeol Choi ;Kyung-Soo Ha ; Eunsung Seo ; Younsik Park ; Seung-Jun Bae ;Indal Song ; Seok-Hun Hyun ; Hyuck-Joon Kwon ; Young-Soo Sohn ; Jung-Hwan Choi ; Kwang-Il Park ; Seong-Jin Jang

Write and Read Frequency-Based Word-Line BatchVTHModulation for 2-D and 3-D-TLC NAND Flash Memories
Yoshiaki Deguchi ; Shun Suzuki ; Ken Takeuchi

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Marco Vigilante ; Patrick Reynaert

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Md Shakil Akter ; Rohan Sehgal ; Frank van der Goes ; Kofi A. A. Makinwa ; Klaas Bult

A Digitally Calibrated Bandgap Reference With 0.06% Error for Low-Side Current Sensing Application
Veeresh Babu Vulligaddala ; RaviKumar Adusumalli ; Sudhakar Singamala ; M. B. Srinivas

Miniaturized, 0.01 mm2, Resistor-Based Thermal Sensor With an Energy Consumption of 0.9 nJ and a Conversion Time of 80Î¼s for Processor Applications
Anatoli Mordakhay ; Joseph Shor

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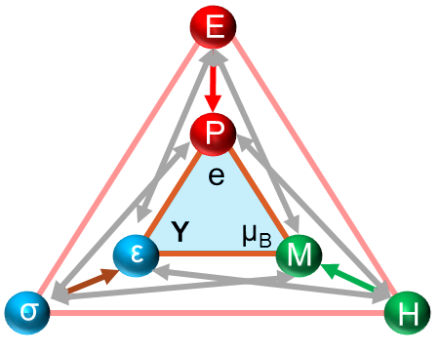
A 0.75-3.0-Gb/s Dual-Mode Temperature-Tolerant Referenceless CDR With a Deadzone-Compensated Frequency Detector Jahoon Jin ; Xuefan Jin ; Jaehong Jung ; Kiwon Kwon ; Jintae Kim ; Jung-Hoon Chun
A 0.4-V 0.93-nW/kHz Relaxation Oscillator Exploiting Comparator Temperature-Dependent Delay to Achieve 94-ppm/Â°C Stability Haowei Jiang ; Po-Han Peter Wang ; Patrick P. Mercier ; Drew A. Hall

IEEE Journal on Exploratory Solid-State Computational Devices and Circuits

Volume 4



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