



**IEEE SOLID-STATE  
CIRCUITS SOCIETY**  
Where ICs are in IEEE

**October 2017**

## **NEWS**



### **Upcoming Webinar**

**Phase-Locked Loops:  
System Perspectives  
Tailored for IC Designers**

**Presented by Professor Woogeun  
Rhee**

**Thursday, November 30 @ 11 AM ET**

**\*Professional Development Hours can be requested for this webinar\***

**[CLICK HERE TO REGISTER!](#)**

**This webinar was prerecorded. Prof. Rhee will be available during the presentation to answer questions regarding content, formulas, or theories. Please follow the link to register for the webinar which is free and open to all SSCS members.**

**Abstract: A phase-locked loop is a key building block in wireline and wireless systems. In the wireline systems, low-jitter clock generation and versatile clock-and-data recovery circuits are critical in high data rate I/O**

links. In the wireless systems, the fractional-N frequency synthesizer plays a critical role in modern transceivers not only as a local oscillator but also as a phase modulator with direct digital modulation. However, the traditional PLL in advanced CMOS technology suffers from poor scalability, loop parameter variability and leakage current problems. Accordingly, diversified PLL architectures and circuit techniques have been proposed in consideration of performance, power and cost, thus making it difficult for circuit designers to choose the right design solution. In this talk, system perspectives and application aspects of the PLL which are useful for IC designers will be discussed.

**Bio:** Woogeun Rhee received the B.S. degree in electronics engineering from Seoul National University, Seoul, Korea, in 1991, the M.S. degree in electrical engineering from the University of California, Los Angeles, in 1993, and the Ph.D. degree in electrical and computer engineering from the University of Illinois, Urbana-Champaign, in 2001. From 1997 to 2001, he was with Conexant Systems, Newport Beach, CA, where he was a Principal Engineer and developed low-power, low-cost fractional-N synthesizers. From 2001 to 2006, he was with IBM Thomas J. Watson Research Center, Yorktown Heights, NY and worked on clocking area for high-speed I/O serial links, including low-jitter phase-locked loops, clock-and-data recovery circuits, and on-chip testability circuits. In August 2006, he joined the faculty as an Associate Professor at the Institute of Microelectronics, Tsinghua University, Beijing, China, and became a Professor in December 2011. His current research interests include short-range low-power radios for next generation wireless systems and clock/frequency generation circuits for wireline and wireless communications. He holds 23 U.S. patents. Dr. Rhee is currently an IEEE Distinguished Lecturer of the Solid-State Circuits Society (2016-2017) and serves as an Associate Editor for IEEE JSSC. He has been an Associate Editor for IEEE TCAS-II (2008-2009) and a Guest Editor for IEEE JSSC Special Issue in November 2012 and November 2013. He has served as a member of several IEEE conferences, including ISSCC (2012-2016), CICC, and A-SSCC.

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## Earn Continuing Education Hours

Have you attended an SSSC webinar? Attendees of upcoming and past webinars have the opportunity to earn professional development hours. Certificates of completion are offered to participants who view a webinar. A certificate of completion confirms one hour of professional development. After you attend the webinar, you may request a certificate of completion by completing the form [HERE](#).

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**Download the new SSSC Mobile App**



### ***VOLTA is now available for download via the Apple Store and GooglePlay***

Integrated Circuits (ICs) are at the core of our hi-tech world. They are inside everything electronics. In the coming robot/IoT/AR/VR era, the application and deployment of ICs will become even more prolific and widespread. IEEE Volta is an app developed by IEEE Solid-State Circuits Society (SSCS) aiming at educating the general public about the importance and the history of ICs over the years.

The application is named after Alessandro Volta, a pioneer of electricity and power. The puzzle themes feature the most significant ICs that have changed our way of living. Through learning about these ICs, users gain the historic perspective about this fascinating field and shed some light on what the future ICs may bring for us.

- [Click here](#) to download via the Apple App Store
- [Click here](#) to download via GooglePlay

## **2018 ISSCC Student Travel Grant Awards**

**The 2018 ISSCC Student Travel Grant Awards (STGA's) are now open.**

[Applications will be accepted until November 25, 2017.](#)

Applicants must meet the following requirements:

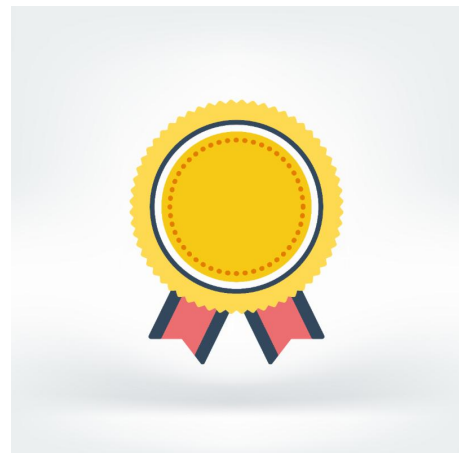
- Applicants **MUST** be Solid-State Circuits Society Members
- Students **MUST** be enrolled, for at least one year, in a PhD program and be recommended by one professor

\*Note\* - A dissertation topic need not be selected

To apply for an STGA, [please click here](#) to access the application and directions.

Please note that the Society, in conjunction with our Women in Circuits program, is pleased to include a new provision to the STGA selection process. A portion of our STGA's will be earmarked to be awarded to those members whose selection would assist SSCS in its ongoing efforts to support the number of women involved in our field of interest, industry, and academia as part of the Society's diversity and inclusion efforts in growing and serving our membership. Female graduate students are strongly encouraged to apply and participate in the WIC activities at SSCS sponsored conferences.

If you have any questions, please email Lauren Caruso at [l.caruso@ieee.org](mailto:l.caruso@ieee.org).



**NEW!** SSCS Members, IEEE Members, and Non-Members can now earn Professional Development Hours (PDH's) and Continuing Education Units (CEU's) for our [CONFedu series](#).



In an effort to increase member benefits, SSCS has created the SSCS Resource Center. This informational hub will house technical information such as past webinar videos and slides, ISSCC tutorials and short courses, and more.

**Top 3 Downloaded Products on the SSCS Resource Center:**

- 1). [Demystifying Linear Time Varying Circuits](#) by Shanthi Pavan
- 2). [Enabling and Exploiting Machine Learning in Ultra-low-power Devices](#) by Naveen Verma
- 3). [Bringing Flexibility to Ultra Low Energy IoE Circuits and Systems](#) by Edith Beigne

[Click here to visit the SSCS Resource Center.](#)

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## EDUCATION

### Upcoming Distinguished Lecturer Events in November

	SPEAKER	CHAPTER	TOPIC
November 10	Ehsan Afshari	SSCS/CPMT Vancouver	TBD  For more information, <a href="#">please click here</a>
November 10	Dennis Sylvester	SSCS Tsinghua	Ultra-low Power IC Design 101  For more information, <a href="#">please click here</a>
November 13	Carlo Samori	SSCS Atlanta	DTC-Based Digital PLLs

			For more information, <a href="#">please click here</a>
November 14	Hyeon-min Bae	SSCS Singapore	High-speed transceiver design for >100Gb/s broadband communications  For more information, <a href="#">please click here</a>
November 15	Carlo Samori	SSCS Princeton	DTC-Based Digital PLLs  For more information, <a href="#">please click here</a>
November 15	Piet Wambacq	University of Bordeaux - SCS Student Branch	Basics of 60GHz front-end building blocks in CMOS  For more information, <a href="#">please click here</a>
November 16	Hyeon-Min Bae	SSCS Beijing	High-speed transceiver design for >100Gb/s broadband communications  For more information, <a href="#">please click here</a>
November 20	Yong Ping Xu	SSCS Saintgits - Student Chapter	MEMS Inertial Sensors  For more information, <a href="#">please click here</a>
November 30	Pieter Harpe	SSCS Sweden	Advanced SAR ADCs - efficiency, accuracy, calibration, and references  For more information, <a href="#">please click here</a>

For more information on upcoming Distinguished Lecturer Tours, [CLICK HERE.](#)

## CONFERENCES

### Upcoming Conferences

<a href="#"><u>2017 IEEE Asian Solid-State Circuits Conference (A-SSCC)</u></a> Korea (South)	November 6 - 8, 2017
<a href="#"><u>2018 International Solid-State Circuits Conference (ISSCC)</u></a> San Francisco, CA	February 11 - 15, 2018
<a href="#"><u>2018 IEEE Custom Integrated Circuits Conference (CICC)</u></a> San Diego, CA	April 8 - 11, 2018

<b><u>2018 International Symposium on VLSI Technology, Systems and Application (VLSI-TSA)</u></b> Hsinchu, Taiwan	April 16 - April 19, 2018
<b><u>2018 International Symposium on VLSI Design, Automation and Test (VLSI-DAT)</u></b> Hsinchu, Taiwan	April 16-19, 2018
<b><u>2018 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)</u></b> Philadelphia, PA	June 10 - 12, 2018
<b><u>2018 IEEE Symposium on VLSI Technology</u></b> Honolulu, HI	June 18 - 22, 2018
<b><u>2018 IEEE Symposium on VLSI Circuits</u></b> Honolulu, HI	June 18 - 22, 2018

## Young Professionals in Space

[Young Professionals in Space](#) is an event planned by the IEEE Young Professionals (YP) Affinity Group from 24th to 26th November 2017 at the Sterlings Mac Hotel, Bengaluru, India.



Young Professionals in Space (YPS) is an initiative to bring scientists, practitioners, engineers, and leaders of the space industry and agencies under one roof. Join us for discussion on recent research breakthroughs, technical advancements, existing opportunities, and emerging space technologies. This three-day program brings in scientists, experts, engineers and researchers from different disciplines of space technology and engineering. This event addresses the wild west of space applications, startups in space, a hands-on space bootcamp cube satellite development, and many other events.

[Click here to register!](#)

## ISSCC 2018 Workshop on Circuits for Social Good

February 11, 2018  
 Reception: 5 PM - 6 PM  
 Workshop: 6 PM - 9 PM  
 OPEN TO ALL

*The Workshop on Circuits for Social Good highlights various ways that circuits can help address some of the most important challenges facing society today, ranging from health care to energy conservation.*

*The program aims to give a broad perspective of how one can have impact. It begins with several keynotes and invited talks from industry, academia and startups followed by interactive round-table discussions on topics including machine learning, medical devices, next generation communications, security and IoT, as well as discussions on career paths in research, product development, and entrepreneurship.*

### KEYNOTES

- Teresa H. Meng, Professor Emeritus at Stanford, Founder of Atheros

- Nevine Nassif, Intel Fellow, "Low power design: how can we help become green?"

### INVITED TALKS

- Esther Rodriguez-Villegas, Associate Professor at Imperial College London, "Pioneering ultra-low power technologies to empower personal healthcare"
- Christine Ho, Co-Founder at Imprint Energy, "Driving a Ground-Breaking Ultrathin Flexible Printed Battery to Market - My Journey From Technologist to Entrepreneur"

### ROUND TABLES (ASK AN EXPERT!)

- Next-Generation Communications
- Machine Learning & Multimedia Systems
- Medical Devices and Applications
- Security and IoT
- Careers in Industry
- Careers in Academia
- Entrepreneurship

[Click here for more information](#)

## CALL FOR PAPERS

### 2018 IEEE Custom Integrated Circuits Conference (CICC) - Call for Papers

IEEE CICC is a premier conference devoted to IC development. The conference program is a blend of oral presentations, exhibits, panels, and forums. The conference sessions present original first published technical work and innovative circuit techniques that tackle practical problems. CICC is the conference to find out how to solve design problems, improve circuit design techniques, get exposure to new technology areas, and network with peers, authors, and industry experts.

CICC 2018 welcomes submissions of original and unpublished work on:

- **Analog Circuits and Techniques** for areas such as communications, biomedical, aerospace, automotive, energy, environment, analog computing and security applications, ranging from building blocks to silicon sensors, interfaces, and novel clock generation architectures.
- **Power Management** circuits and design techniques including DC-DC converters, control and management circuits, linear regulators, wireless power transfer, and other methods for improvements in overall system efficiency and performance.
- **Data Converters** of all types enabled by new techniques, architectures, or technologies.
- **Wireless Transceivers and RF/mm-Wave Circuits** for low-power, energy-efficient and high performance wireless links, biomedical and sensing networks, IoT applications, cellular connectivity including M2M applications (LTE-M, NB-IoT), emerging broadband and MIMO networks (5G, WLAN), vehicle-to-vehicle (V2V), millimeter-wave & THz systems (radar, sensing and imaging), frequency synthesis and LO generation.
- **Wireline and Optical Communications Circuits and Systems** for electrical and optical communications, including serial links for intra-chip and chip-to-chip interconnections, high-speed memory and graphics interfaces, backplanes, long-haul, and power line communications; novel I/O circuits for advancing data rates, improving power efficiency, and supporting extended voltage applications; clocking techniques including PLLs and CDRs; components such as equalizers, high-speed ADC-RX/DAC-TX, silicon photonic and optical interface circuitry.
- **Design Foundations**
  - High-level system modeling, digital design infrastructure, and mixed-mode (analog-digital)

- verification for complex SOCs. Novel digital architectures for emerging applications. Design methodologies for functional safety.
  - Modeling and simulation of advanced CMOS and power devices to improve design quality, efficiency, and reliability. Design methodologies for emerging applications (deep learning, automobile, IoT, security), and design for manufacture, test, aging and reliability (novel DFT circuits, system-level testing).
- **Emerging Technologies, Systems, and Applications** - Emerging technologies solicit hardware focused papers in the technologies of tomorrow extending from new device and memory technology to system integration, applications and packaging with focus on, but not limited to:
  - **Hardware-based artificial intelligence and security.** Hardware designs for emerging algorithms, hardware security, hardware and energy-efficient artificial intelligence, machine learning, deep learning accelerators. Applications include autonomous transportation and cloud computing.
  - **Next-generation devices, technology, integration and packaging** including nano-primitives, non-silicon based technology, MEMS, emerging memories, non-traditional circuits, mm-wave/THz passives and integration, flexible, printed, large-area and organic electronics. system in package, 2.5D, 3D and monolithic 3DIC, multi-die heterogeneous integration, silicon photonic interconnects and packaging, advanced assembly and bonding, embedded cooling technologies,
  - **Biomedical circuits, systems, and applications** including neural interfaces, microarrays, lab-on-a-chip, bio-inspired circuits, implantable and/or wearable systems, closed-loop systems with sensing and actuation, medical imaging, and other biosensors including biomedical signal processing SoCs.

**Paper Submission Information:** The deadline for submission of technical papers is November 6, 2017. Authors of accepted papers will be notified via email by January 16, 2018. Top-rated papers are eligible for publication in a special issue of IEEE Journal of Solid-State Circuits.

For more information on paper submission, visit [www.ieee-cicc.org](http://www.ieee-cicc.org).

## RFIC 2018: IEEE Radio Frequency Integrated Circuits Symposium - Call for Papers

The 2018 IEEE Radio Frequency Integrated Circuits Symposium (RFIC 2018) will be held in Philadelphia, PA, USA on June 10-12, 2018. For latest information, please visit [rfic-ieee.org](http://rfic-ieee.org).

The conference is soliciting papers describing original work in RFIC circuits, systems engineering, design methodology, RF modeling and CAD simulation, RFIC technologies, devices, fabrication, testing, reliability, packaging and modules to support RF applications in areas such as, but not limited to:

- **Wireless Cellular and Connectivity:** 2G/3G/4G/5G (sub-6GHz), LTE, WWAN, WLAN, BT, GPS, FM,UWB
- **Low Power Transceivers:** RFID, NFC, Zigbee, 802.15.4, WPAN, WBAN, Biomedical, Sensor Nodes, IR-UWB, Wake-up Receivers
- **Receiver Sub-Systems and Circuits:** LNAs, Mixers, VGAs, phase shifters, switches, Integrated FEM, amplifiers, filters, demodulators
- **Mixed-Signal RF and Data Converters:** RF and baseband converters(ADC/DAC),Sub-sampling/Over-sampling Circuits
- **Reconfigurable and Tunable Front-Ends:** SDR/Cognitive Radio,Wideband/Multi-band Front-Ends,Interference Cancellation, Full-Duplex, Adaptive Front-Ends
- **Transmitter Sub-Systems and Power Amplifiers:** Power Amplifiers, Drivers, modulators, digital transmitters, Advanced TX circuits, linearization and efficiency enhancement techniques
- **Oscillators:** VCOs, injection-locking frequency dividers/multipliers
- **Frequency Synthesis:** PLLs, DLLs, MDLLS, DDS, LO drivers, frequency dividers
- **Device Technologies, Packaging, Modeling, and Testing:** CMOS, SOI, FinFet, SiGe, GaAs, GaN, MEMS, Integrated Passives, Photonic, Emerging Devices, Reliability, Packaging, Modeling and Testing, EM Modeling/Co-Simulation, Built-in-Self-Test (BIST)
- **Millimeter-and SubMillimeter Wave Systems:** >20GHzSoCs/SiPs for wireless communication (5Gmm-Wave, WiGig, 802.11ay), phased-arrays, imaging, radar, remote sensing
- **High-Speed Data Transceivers:** Wireline, Optical Transceivers, and CDRs for High-Speed



**\*NEW THIS YEAR\*** - A double-blind review process will be used to ensure anonymity for both authors and reviewers.

**Electronic Submission Deadlines**- Technical Paper Summaries in PDF Format are due 12 January 2018, Final Manuscripts for the Digest and USB are due 22 March 2018.

Submissions must be made at [rfic-ieee.org](http://rfic-ieee.org).

## 2018 Symposium on VLSI Circuits: Call for Papers

The 2018 Symposium on VLSI Circuits will be held at the Hilton Hawaiian Village, Honolulu, Hawaii, USA on Monday, June 18, 2018 to Friday, June 22, 2018. Short courses will be held on June 18, the technical sessions will be held on June 19, June 20, and June 21, and the forum will be held on June 22.

The Circuits Symposium is seeking papers and placing special emphasis on several innovative system focus areas. Paper submissions are encouraged in the following areas:

- Machine and deep learning
- Internet of Things
- Industrial electronics
- Big Data management and analytics
- Robotics and autonomous transportation

In addition, submissions are welcomed in all of the following circuits areas:

- Processors, architectures, and SoCs
- Digital circuits, signal integrity, and IOs
- Memory circuits, architectures, and interfaces
- Biomedical circuits
- Sensors, imagers, and display circuits
- Power conversion circuits
- Analog, amplifier and filter circuits
- Wireless receivers and transmitters
- Data converters
- Frequency generation and clock circuits
- Wireline receivers and transmitters

**Submission Due Date: Monday, January 29, 2018 @ 23:59 PST.**

The symposia website is the central resource for additional information, including details on paper submissions - <http://vlsisymposium.org>

## BioCAS 2018: Call for Papers *Biomedical Circuits and Systems Conference*

BioCAS 2018 is a premier international forum for presenting the interdisciplinary research and development activities at the crossroads of medicine, life sciences, physical sciences and engineering that shape tomorrow's medical devices and healthcare systems.

This conference brings together members of our communities to broaden their knowledge in emerging areas of research at the interface of the life sciences and the circuits and systems engineering. The three-day single-track program for BioCAS 2018 is multidisciplinary in topics including but not limited to:

### **Biomedical Technologies**

- \* Assistive, Rehabilitation, and Quality of Life Technologies
- \* Biofeedback, Neuromodulation, and Closed-Loop Systems
- \* Bio-Inspired and Neuromorphic Circuits and Systems
- \* Biosensor Devices and Interface Circuits
- \* Biotelemetry and Energy Harvesting/Scavenging Circuits and Systems

- \* Body Area/ Sensor and Wireless/Wearable Health Monitoring
- \* Electronics for Neuroscience
- \* Implantable Medical Electronics
- \* Lab-on-Chip and BioMEMS

### Biomedical Applications

- \* Point-of-Care Technologies for Healthcare
- \* Biomedical Imaging and Image Processing
- \* Biosignal Recording, Processing, and Machine Learning
- \* Genomics and Systems Biology
- \* Human-Machine Interfaces
- \* Medical Information Systems and Bioinformatics

### Submission Guidelines

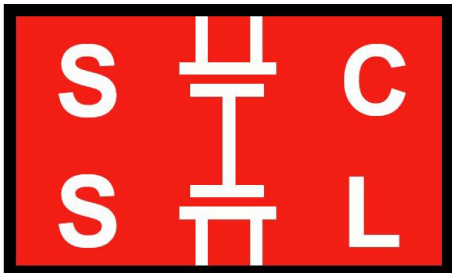
The complete 4-page paper (in standard IEEE double-column format), including the title, authors' names, affiliations and e-mail addresses, as well as a short abstract and an optional demonstration video link (3 minute max) are requested. Papers must be submitted electronically in PDF format through

[www.biocas2018.org](http://www.biocas2018.org).

### Important Dates

- Monday, April 23, 2018: Special Session Proposal Deadline
- Monday, June 11, 2018: Regular Paper Submission Deadline
- Monday, July 16, 2018: Live Demo Session deadline
- Monday, August 13, 2018: Author Notification Date
- Friday, August 31, 2018: Author Registration/Final Paper Submission Deadline

## PUBLICATIONS



### IEEE Solid-State Circuits Letters - Officially Launches

We're happy to announce that our new publication, IEEE Solid-State Circuits Letters, has launched. We are now accepting paper submissions.

For more information, visit:

<http://sscs.ieee.org/publications/ieee-solid-state-circuits-letters-ssc-l>

For paper submission, visit:

<https://mc.manuscriptcentral.com/ssc-l>

### The latest in SCS Flagship Publications...



### IEEE Journal of Solid-State Circuits

Vol. 52, Issue 11, November 2017

<p><b><a href="#">Rail-to-Rail-Input Dual-Radio 64-Channel Closed-Loop Neurostimulator</a></b>  Hossein Kassiri ; Muhammad Tariqus Salam ; Mohammad Reza Pazhouhandeh ; Nima Soltani ; Jose Luis Perez Velazquez ; Peter Carlen ; Roman Genov</p>
<p><b><a href="#">An 80-mVpp Linear-Input Range, 1.6- GÎ© Input Impedance, Low-Power Chopper Amplifier for Closed-Loop Neural Recording That Is Tolerant to 650-mVpp Common-Mode Interference</a></b>  Hariprasad Chandrakumar ; Dejan Marković</p>
<p><b><a href="#">A 1.4-m Î© -Sensitivity 94-dB Dynamic-Range Electrical Impedance Tomography SoC and 48-Channel Hub-SoC for 3-D Lung Ventilation Monitoring System</a></b>  Minseo Kim ; Jaeun Jang ; Hyunki Kim ; Jihee Lee ; Jaehyuck Lee ; Jiwon Lee ; Kyoung-Rog Lee ; Kwantae Kim ; Yongsu Lee ; Kyuho Jason Lee ; Hoi-Jun Yoo</p>
<p><b><a href="#">A Pixel Pitch-Matched Ultrasound Receiver for 3-D Photoacoustic Imaging With Integrated Delta-Sigma Beamformer in 28-nm UTBB FD-SOI</a></b>  Man-Chia Chen ; Aldo Peña Perez ; Sri-Rajasekhar Kothapalli ; Philippe Cathelin ; Andreia Cathelin ; Sanjiv Sam Gambhir ; Boris Murmann</p>
<p><b><a href="#">A Fully Integrated CMOS Fluorescence Biochip for DNA and RNA Testing</a></b>  Arun Manickam ; Rituraj Singh ; Mark W. McDermott ; Nicholas Wood ; Sara Bolouki ; Pejman Naraghi-Arani ; Kirsten A. Johnson ; Robert G. Kuimelis ; Gary Schoolnik ; Arjang Hassibi</p>
<p><b><a href="#">64-QAM 60-GHz CMOS Transceivers for IEEE 802.11ad/ay</a></b>  Rui Wu ; Ryo Minami ; Yuuki Tsukui ; Seitaro Kawai ; Yuuki Seo ; Shinji Sato ; Kento Kimura ; Satoshi Kondo ; Tomohiro Ueno ; Nurul Fajri ; Shoutarou Maki ; Noriaki Nagashima ; Yasuaki Takeuchi ; Tatsuya Yamaguchi ; Ahmed Musa ; Korkut Kaan Tokgoz ; Teerachot Siriburanon ; Bangan Liu ; Yun Wang ; Jian Pang ; Ning Li ; Masaya Miyahara ; Kenichi Okada ; Akira Matsuzawa</p>
<p><b><a href="#">A 54.4-90 GHz Low-Noise Amplifier in 65-nm CMOS</a></b>  Yiming Yu ; Huihua Liu ; Yunqiu Wu ; Kai Kang</p>
<p><b><a href="#">Broadband Oscillator-Free THz Pulse Generation and Radiation Based on Direct Digital-to-Impulse Architecture</a></b>  M. Mahdi Assefzadeh ; Aydin Babakhani</p>
<p><b><a href="#">A 312-GHz CMOS Injection-Locked Radiator With Chip-and-Package Distributed Antenna</a></b>  Liang Wu ; Shaowei Liao ; Quan Xue</p>
<p><b><a href="#">A 2.4-GHz 1.5-mW Digital Multiplying Delay-Locked Loop Using Pulsewidth Comparator and Double Injection Technique</a></b>  Hyunik Kim ; Yongjo Kim ; Taeik Kim ; Hyung-Jong Ko ; Seonghwan Cho</p>
<p><b><a href="#">A Sierpinski Space-Filling Clock Tree Using Multiply-by-3 Fractal-Coupled Ring Oscillators</a></b>  Yi-Wei Lin ; Shawn S. H. Hsu</p>
<p><b><a href="#">A 40-Gb/s Quarter-Rate SerDes Transmitter and Receiver Chipset in 65-nm CMOS</a></b>  Xuqiang Zheng ; Chun Zhang ; Fangxu Lv ; Feng Zhao ; Shuai Yuan ; Shigang Yue ; Ziqiang Wang ; Fule Li ; Zhihua Wang ; Hanjun Jiang</p>
<p><b><a href="#">A 7.1-fJ/Conversion-Step 88-dB SFDR SAR ADC With Energy-Free"Swap To Reset</a></b>  Maoqiang Liu ; Arthur H. M. van Roermund ; Pieter Harpe</p>
<p><b><a href="#">A 0.8-1.2 V 10-50 MS/s 13-bit Subranging Pipelined-SAR ADC Using a Temperature-Insensitive Time-Based Amplifier</a></b>  Minglei Zhang ; Kyoohyun Noh ; Xiaohua Fan ; Edgar Sánchez-Sinencio</p>
<p><b><a href="#">A Low-Power CMOS Crystal Oscillator Using a Stacked-Amplifier Architecture</a></b>  Shunta Iguchi ; Takayasu Sakurai ; Makoto Takamiya</p>
<p><b><a href="#">A Precision Capacitance-to-Digital Converter With 16.7-bit ENOB and 7.5-ppm/Â°C Thermal Drift</a></b>  Ruimin Yang ; Michiel A. P. Pertjjs ; Stoyan Nihtianov</p>
<p><b><a href="#">A Noise-Efficient 36 nV/ Hz Chopper Amplifier Using an Inverter-Based 0.2-V Supply Input Stage</a></b>  Frank M. Yaul ; Anantha P. Chandrakasan</p>
<p><b><a href="#">A 144-MHz Fully Integrated Resonant Regulating Rectifier With Hybrid Pulse Modulation for mm-Sized Implants</a></b></p>

Chul Kim ; Sohyung Ha ; Jiwoong Park ; Abraham Akinin ; Patrick P. Mercier ; Gert Cauwenberghs

**[Self-Regulated Reconfigurable Voltage/Current-Mode Inductive Power Management](#)**

Hesam Sadeghi Gougheri ; Mehdi Kiani

**[A Fully Integrated Digital Low-Dropout Regulator Based on Event-Driven Explicit Time-Coding Architecture](#)**

Doyun Kim ; Mingoo Seok

**[A 6 A, 93% Peak Efficiency, 4-Phase Digitally Synchronized Hysteretic Buck Converter With  \$\hat{A}\pm 1.5\%\$  Frequency and  \$\hat{A}\pm 3.6\%\$  Current-Sharing Error](#)**

Ming Sun ; Zhe Yang ; Kishan Joshi ; Debashis Mandal ; Philippe Adell ; Bertan Bakkaloglu

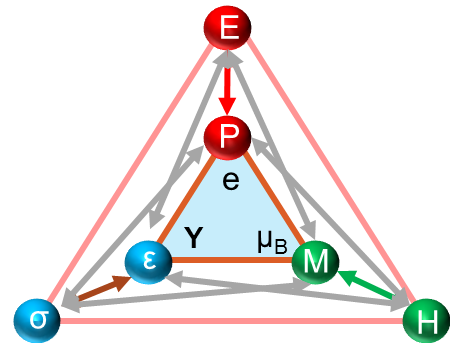
**[A Thin-Film, a-IGZO, 128b SRAM and LPRAM Matrix With Integrated Periphery on Flexible Foil](#)**

Florian De Roose ; Kris Myny ; Marc Ameys ; Jan-Laurens P. J. van der Steen ; Joris Maas ; Joris de Riet ; Jan Genoe ; Wim Dehaene

**[Patent Abstracts](#)**

**IEEE Journal on Exploratory Solid-State Computational Devices and Circuits**

**2017 Highlights**



**[MagCAD: Tool for the Design of 3-D Magnetic Circuits](#)**

Fabrizio Riente ; Umberto Garlando ; Giovanna Turvani ; Marco Vacca ; Massimo Ruo Roch ; Mariagrazia Graziano

**[A Thermodynamic Perspective of Negative-Capacitance Field-Effect Transistors](#)**

Sou-Chi Chang ; Uygur E. Avci ; Dmitri E. Nikonov ; Ian A. Young

**[An Energy-Efficient Digital ReRAM-Crossbar-Based CNN With Bitwise Parallelism](#)**

Leibin Ni ; Zichuan Liu ; Hao Yu ; Rajiv V. Joshi

**[Nonboolean Pattern Recognition Using Chains of Coupled CMOS Oscillators as Discriminant Circuits](#)**

Vahnood Pourahmad ; Sasikanth Manipatruni ; Dmitri Nikonov ; Ian Young ; Ehsan Afshari

**[Compact Modeling of Distributed Effects in 2-D Vertical Tunnel FETs and Their Impact on DC and RF Performances](#)**

Jie Min ; Peter M. Asbeck

**[Nonvolatile Spintronic Memory Array Performance Benchmarking Based on Three-Terminal Memory Cell](#)**

Chenyun Pan ; Azad Naeemi

**[CoMET: Composite-Input Magnetolectric- Based Logic Technology](#)**

Meghna G. Mankalale ; Zhaoxin Liang ; Zhengyang Zhao ; Chris H. Kim ; Jian-Ping Wang ; Sachin S. Sapatnekar

**[Electrical-Spin Transduction for CMOS-Spintronic Interface and Long-Range Interconnects](#)**

Rouhollah Mousavi Iraei ; Sasikanth Manipatruni ; Dmitri E. Nikonov ; Ian A. Young ; Azad Naeemi

JxCDC papers listed in order of popularity can be found online [HERE](#).

For paper submission details, click [HERE](#).

## Seeking News

Please send any chapter news or happenings (Distinguished Lecturer visits, events hosted by your SSCS chapter, awards received by members, etc) to Abira Sengupta, SSCS Magazine News Editor, for inclusion in an upcoming issue of the magazine. Please email - [Abira.Sengupta@ieee.org](mailto:Abira.Sengupta@ieee.org). We look forward to receiving your news articles!

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For more chapter news, [check out](#) the Summer 2017 issue of the Solid-State Circuits Magazine.

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## FEEDBACK

Let us know what you think! Please [email us](#) to send us your comments about the newsletter, what you would like to see included each month, or any other comments.

[CLICK HERE TO VISIT OUR WEBSITE](#)

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