IEEE SOLID-STATE CIRCUITS SOCIETY

Where ICs are in IEEE

# November 2017

## NEWS

## Upcoming Webinar

### Phase-Locked Loops: System Perspectives Tailored for IC Designers

**Presented by Professor Woogeun Rhee**

**Thursday, November 30 @ 11 AM ET**

***Professional Development Hours can be requested for this webinar***

**CLICK HERE TO REGISTER!**

**This webinar was prerecorded. Prof. Rhee will be available during the presentation to answer questions regarding content, formulas, or theories. Please follow the link to register for the webinar which is free and open to all SSCS members.**

**Abstract: A phase-locked loop is a key building block in wireline and wireless systems. In the wireline systems, low-jitter clock generation and versatile clock-and-data recovery circuits are critical in high data rate I/O**

**links. In the wireless systems, the fractional-N frequency synthesizer plays a critical role in modern transceivers not only as a local oscillator but also as a phase modulator with direct digital modulation. However, the traditional PLL in advanced CMOS technology suffers from poor scalability, loop parameter variability and leakage current problems. Accordingly, diversified PLL architectures and circuit techniques have been proposed in consideration of performance, power and cost, thus making it difficult for circuit designers to choose the right design solution. In this talk, system perspectives and application aspects of the PLL which are useful for IC designers will be discussed.**

**Bio: Woogeun Rhee received the B.S. degree in electronics engineering from Seoul National University, Seoul, Korea, in 1991, the M.S. degree in electrical engineering from the University of California, Los Angeles, in 1993, and the Ph.D. degree in electrical and computer engineering from the University of Illinois, Urbana-Champaign, in 2001. From 1997 to 2001, he was with Conexant Systems, Newport Beach, CA, where he was a Principal Engineer and developed low-power, low-cost fractional-N synthesizers. From 2001 to 2006, he was with IBM Thomas J. Watson Research Center, Yorktown Heights, NY and worked on clocking area for high-speed I/O serial links, including low-jitter phase-locked loops, clock-and-data recovery circuits, and on-chip testability circuits. In August 2006, he joined the faculty as an Associate Professor at the Institute of Microelectronics, Tsinghua University, Beijing, China, and became a Professor in December 2011. His current research interests include short-range low-power radios for next generation wireless systems and clock/frequency generation circuits for wireline and wireless communications. He holds 23 U.S. patents. Dr. Rhee is currently an IEEE Distinguished Lecturer of the Solid-State Circuits Society (2016-2017) and serves as an Associate Editor for IEEE JSSC. He has been an Associate Editor for IEEE TCAS-II (2008-2009) and a Guest Editor for IEEE JSSC Special Issue in November 2012 and November 2013. He has served as a member of several IEEE conferences, including ISSCC (2012-2016), CICC, and A-SSCC.**

## Earn Continuing Education Hours

Have you attended an SSCS webinar? Attendees of upcoming and past webinars have the opportunity to earn professional development hours. Certificates of completion are offered to participants who view a webinar. A certificate of completion confirms one hour of professional development. After you attend the webinar, you may request a certificate of completion by completing the form **HERE**.

## SSCS 2017 Outstanding Chapter Award

The 2017 Outstanding Chapter Award is scheduled to be presented at ISSCC 2018.

The selection of the Outstanding Chapter Award is based on:

- the quality and quantity of activities and programs sponsored by the chapter
- the accrual of practical benefits for local chapter members
- demonstrations of successful outreach programs to the professional community
- growth of chapter membership

If you would like to submit a nomination for this 2017 award, **please click here** to view application instructions.

Email Lauren Caruso **l.caruso@ieee.org** if you have any questions.

**The application deadline is December 21, 2017.**

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## Download the new SSCS Mobile App

***VOLTA is now available for download via the Apple Store and GooglePlay***

Integrated Circuits (ICs) are at the core of our hi-tech world. They are inside everything electronics. In the coming robot/IoT/AR/VR era, the application and deployment of ICs will become even more prolific and widespread. IEEE Volta is an app developed by IEEE Solid-State Circuits Society (SSCS) aiming at educating the general public about the importance and the history of ICs over the years.

The application is named after Alessandro Volta, a pioneer of electricity and power. The puzzle themes feature the most significant ICs that have changed our way of living. Through learning about these ICs, users gain the historic perspective about this fascinating field and shed some light on what the future ICs may bring for us.

- **Click here** to download via the Apple App Store
- **Click here** to download via GooglePlay

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# SSCS Resource Center

**NEW! SSCS Members, IEEE Members, and Non-Members can now earn Professional Development Hours (PDH's) and Continuing Education Units (CEU's) for our CONFedu series.**


**In an effort to increase member benefits, SSCS has created the SSCS Resource Center. This informational hub will house technical information such as past webinar videos and slides, ISSCC tutorials and short courses, and more.**

**Top 3 Downloaded Products on the SSCS Resource Center:**

**1). Demystifying Linear Time Varying Circuits by Shanthi Pavan**

**2). Enabling and Exploiting Machine Learning in Ultra-low-power Devices by Naveen Verma**

**3). Bringing Flexibility to Ultra Low Energy IoE Circuits and Systems by Edith Beigne**

**Click here to visit the SSCS Resource Center.**

# EDUCATION

## Upcoming Distinguished Lecturer Events in December

| | SPEAKER | CHAPTER | TOPIC |
|---|---|---|---|
| December 1 | Patrick Yue | SSCS Silicon Valley | Recent Developments in Transceiver SoC Design for Next Generation Optical Networks<br><br>For more information, please click here |
| December 4 | Woogeun Rhee | SSCS Kansai | Phase-Locked Frequency Synthesis and Modulation for Modern Wireless Transceivers<br><br>For more information, please click here |
| December 6 | Yong Ping Xu | SSCS Taiwan | MEMS Inertial Sensors<br><br>For more information, please click here |

| | | | |
|---|---|---|---|
| **December 7** | **Yong Ping Xu** | **SSCS Taipei** | **TBD**<br><br>**For more information, please click here** |
| **December 12** | **Marian Verhelst** | **SSCS Benelux** | **Analog-to-information sensing, going beyond compressive sampling**<br><br>**For more information, please click here** |
| **December 15** | **Pieter Harpe** | **SSCS France** | **Ultra low-power analog front-end design**<br><br>**Power-efficient, high resolution and reconfigurable SAR ADCs**<br><br>**For more information, please click here** |
| **December 15** | **Ehsan Afshari** | **SSCS Hong Kong Student Chapter** | **Circuit Design at Extreme: Pushing the Limits of Silicon**<br><br>**For more information, please click here** |

**For more information on upcoming Distinguished Lecturer Tours, CLICK HERE.**

# CONFERENCES

## Upcoming Conferences

| | |
|---|---|
| **2018 International Solid-State Circuits Conference (ISSCC)**<br>San Francisco, CA | **February 11 - 15, 2018** |
| **2018 Design, Automation & Test in Europe Conference and Exhibition (DATE)**<br>Dresden, Germany | **March 19 - 23, 2018** |
| **2018 IEEE Custom Integrated Circuits Conference (CICC)**<br>San Diego, CA | **April 8 - 11, 2018** |
| **2018 International Symposium on VLSI Technology, Systems and Application (VLSI-TSA)**<br>Hsinchu, Taiwan | **April 16 - April 19, 2018** |
| **2018 International Symposium on VLSI Design, Automation and Test (VLSI-DAT)**<br>Hsinchu, Taiwan | **April 16-19, 2018** |
| **2018 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)**<br>Philadelphia, PA | **June 10 - 12, 2018** |
| **2018 IEEE Symposium on VLSI Technology**<br>Honolulu, HI | **June 18 - 22, 2018** |
| **2018 IEEE Symposium on VLSI Circuits**<br>Honolulu, HI | **June 18 - 22, 2018** |

# ISSCC 2018 Workshop on Circuits for Social Good

**February 11, 2018**
**Reception: 5 PM - 6 PM**
**Workshop: 6 PM - 9 PM**
**OPEN TO ALL**

*The Workshop on Circuits for Social Good highlights various ways that circuits can help address some of the most important challenges facing society today, ranging from health care to energy conservation.*

*The program aims to give a broad perspective of how one can have impact. It begins with several keynotes and invited talks from industry, academia and startups followed by interactive round-table discussions on topics including machine learning, medical devices, next generation communications, security and IoT, as well as discussions on career paths in research, product development, and entrepreneurship.*

**KEYNOTES**

- Teresa H. Meng, Professor Emeritus at Stanford, Founder of Atheros, "Winning the game in a male-dominated industry"
- Nevine Nassif, Intel Fellow, "Low power design: how can we help become green?

**INVITED TALKS**

- Esther Rodriguez-Villegas, Associate Professor at Imperial College London, "Pioneering ultra-low power technologies to empower personal healthcare"
- Christine Ho, Co-Founder at Imprint Energy, "Driving a Ground-Breaking Ultrathin Flexible Printed Battery to Market - My Journey From Technologist to Entrepreneur"

**ROUND TABLES (ASK AN EXPERT!)**

- Next-Generation Communications

*Alyssa Apsel, Professor at Cornell, Ithaca, NY, USA*
*Azita Emami, Professor at Caltech, Pasadena, CA, USA*

- Machine Learning & Multimedia Systems

*Vivienne Sze, Associate Professor at MIT, Cambridge, MA, USA*
*Marian Verhelst, Assistant Professor at KU Leuven, Leuven, Belgium*

- Medical Devices and Applications

*Rikky Muller, Assistant Professor at UC Berkeley, Berkeley, CA, USA*
*Esther Rodriguez-Villegas, Associate Professor at Imperial College London, London, UK*

- Security and IoT

*Edith Beigne, Senior Scientist at CEA-LETI, Grenoble, France*
*Ingrid Verbauwhede, Professor at KU Leuven, Leuven, Belgium*

- Careers in Industry

*Andreia Cathelin, Fellow at ST Microelectronics, Crolles, France*
*Yildiz Sinangil, Circuit Designer at Apple, Cupertino, CA, USA*
*Trudy Stetzler, Engineering Project Manager at Halliburton, Houston, TX, USA*

*Bich-Yen Nguyen, Senior Fellow at Soitec, Austin, TX, USA*
*Sonia Leon, Principal Engineer at Intel, Santa Clara, CA, USA*

- Careers in Academia

*Terri Fiez, Professor & Vice Chancellor of Research at University of Colorado Boulder, Boulder, CO, USA*
*Milin Zhang, Assistant Professor, Tsinghua University, Beijing, China*

- Entrepreneurship

*Christine Ho, Co-Founder of Imprint Energy, Alameda, CA, USA*
*Teresa H. Meng, Founder of Atheros Communications, Palo Alto, CA, USA*

**Click here for more information**

# CALL FOR PAPERS

## IEEE 5G World Forum 2018 (WF-5G) - Call for Papers

The 2018 IEEE 1st 5G World Forum (5GWF'18) in Santa Clara, California, seeks contributions on how to nurture and cultivate 5G technologies and applications for the benefit of society. This conference aims to bring researchers from industry, academia and research to exchange their vision as well as their achieved advances towards 5G, and encourage innovative cross-domain studies, research, early deployment and large-scale pilot showcases that address the challenges of 5G.
Original, innovative and high quality papers are solicited in the following technical topics of interest, but are not limited to:

- Track 1: 5G Technologies
- Track 2: Applications and Services
- Track 3: 5G & IoT
- Track 4: 5G Security and Privacy
- Track 5: 5G Trials, Experimental Results and Deployment Scenarios
- Track 6: 5G Hardware and Test / Measurements
- Track 7: 5G Special Verticals
- Track 8: 5G Special Topical

Proposals for sessions and events of general interest and relevance to 5G will be considered. These should address the Technical Community and/or provide educational or expository material or recognition of significant contributions to the advancement of 5G technologies.

- Workshop and Special Sessions
- Tutorials
- Industry Forum and Panel
- Doctoral Symposium
- Start-Ups
- Exhibitions

Suggestions for speakers, panels, demonstrations, and sessions aimed at: industry technologists, practitioners, managers, and operators; policy makers, public sector administrators, operators of public infrastructure and services; and others involved in the use of 5G; addressing the conference focus Verticals and Topical Areas identified below and in the full-length CFP.

- 5G Special Vertical Conference
- 5G Special Topical Area

**Important Dates**
Technical Paper Submission Deadline: November 30, 2017
Acceptance Notification: January 15, 2018
Camera-Ready Submission: February 28, 2018

For more information, **click here**.

# RFIC 2018: IEEE Radio Frequency Integrated Circuits Symposium - Call for Papers

The 2018 IEEE Radio Frequency Integrated Circuits Symposium (RFIC 2018) will be held in Philadelphia, PA, USA on June 10-12, 2018. For latest information, please visit **rfic-ieee.org**.

The conference is soliciting papers describing original work in RFIC circuits, systems engineering, design methodology, RF modeling and CAD simulation, RFIC technologies, devices, fabrication, testing, reliability, packaging and modules to support RF applications in areas such as, but not limited to:

- **Wireless Cellular and Connectivity:** 2G/3G/4G/5G (sub-6GHz), LTE, WWAN, WLAN, BT, GPS, FM,UWB
- **Low Power Transceivers:** RFID, NFC, Zigbee, 802.15.4, WPAN, WBAN, Biomedical, Sensor Nodes, IR-UWB, Wake-up Receivers
- **Receiver Sub-Systems and Circuits:** LNAs, Mixers, VGAs, phase shifters, switches, Integrated FEM, amplifiers, filters, demodulators
- **Mixed-Signal RF and Data Converters:** RF and baseband converters(ADC/DAC),Sub-sampling/Over-sampling Circuits
- **Reconfigurable and Tunable Front-Ends:** SDR/Cognitive Radio,Wideband/Multi-band Front-Ends,Interference Cancellation, Full-Duplex, Adaptive Front-Ends
- **Transmitter Sub-Systems and Power Amplifiers:** Power Amplifiers, Drivers, modulators, digital transmitters, Advanced TX circuits, linearization and efficiency enhancement techniques
- **Oscillators:** VCOs, injection-locking frequency dividers/multipliers
- **Frequency Synthesis:** PLLs, DLLs, MDLLS, DDS, LO drivers, frequency dividers
- **Device Technologies, Packaging, Modeling, and Testing:** CMOS, SOI, FinFet, SiGe, GaAs, GaN, MEMS, Integrated Passives, Photonic, Emerging Devices, Reliability, Packaging, Modeling and Testing, EM Modeling/Co-Simulation, Built-in-Self-Test (BIST)
- **Millimeter-and SubMillimeter Wave Systems:** >20GHzSoCs/SiPs for wireless communication (5Gmm-Wave, WiGig, 802.11ay), phased-arrays, imaging, radar, remote sensing
- **High-Speed Data Transceivers:** Wireline, Optical Transceivers, and CDRs for High-Speed Data links

***NEW THIS YEAR*** - A double-blind review process will be used to ensure anonymity for both authors and reviewers.

**Electronic Submission Deadlines**- Technical Paper Summaries in PDF Format are due 12 January 2018, Final Manuscripts for the Digest and USB are due 22 March 2018.

Submissions must be made at **rfic-ieee.org**.

# 2018 Symposium on VLSI Circuits: Call for Papers

The 2018 Symposium on VLSI Circuits will be held at the Hilton Hawaiian Village, Honolulu, Hawaii, USA on Monday, June 18, 2018 to Friday, June 22, 2018. Short courses will be held on June 18, the technical sessions will be held on June 19, June 20, and June 21, and the forum will be held on June 22.

The Circuits Symposium is seeking papers and placing special emphasis on several innovative system focus areas. Paper submissions are encouraged in the following areas:

- Machine and deep learning
- Internet of Things
- Industrial electronics
- Big Data management and analytics
- Robotics and autonomous transportation

In addition, submissions are welcomed in all of the following circuits areas:

- Processors, architectures, and SoCs
- Digital circuits, signal integrity, and IOs
- Memory circuits, architectures, and interfaces
- Biomedical circuits
- Sensors,imagers, and display circuits
- Power conversion circuits
- Analog, amplifier and filter circuits
- Wireless receivers and transmitters
- Data converters
- Frequency generation and clock circuits
- Wireline receivers and transmitters

**Submission Due Date: Monday, January 29, 2018 @ 23:59 PST.**

The symposia website is the central resource for additional information, including details on paper submissions - **http://vlsisymposium.org**

## BioCAS 2018: Call for Papers
## *Biomedical Circuits and Systems Conference*

BioCAS 2018 is a premier international forum for presenting the interdisciplinary research and development activities at the crossroads of medicine, life sciences, physical sciences and engineering that shape tomorrow's medical devices and healthcare systems.
This conference brings together members of our communities to broaden their knowledge in emerging areas of research at the interface of the life sciences and the circuits and systems engineering. The three-day single-track program for BioCAS 2018 is multidisciplinary in topics including but not limited to:

**Biomedical Technologies**
* Assistive, Rehabilitation, and Quality of Life Technologies
* Biofeedback, Neuromodulation, and Closed-Loop Systems
* Bio-Inspired and Neuromorphic Circuits and Systems
* Biosensor Devices and Interface Circuits
* Biotelemetry and Energy Harvesting/Scavenging Circuits and Systems
* Body Area/Sensor Network and Wireless/Wearable Health Monitoring
* Electronics for Neuroscience
* Implantable Medical Electronics
* Lab-on-Chip and BioMEMS

**Biomedical Applications**
* Point-of-Care Technologies for Healthcare
* Biomedical Imaging and Image Processing
* Biosignal Recording, Processing, and Machine Learning
* Genomics and Systems Biology
* Human-Machine Interfaces
* Medical Information Systems and Bioinformatics

**Submission Guidelines**
The complete 4-page paper (in standard IEEE double-column format), including the title, authors' names, affiliations and e-mail addresses, as well as a short abstract and an optional demonstration video link (3 minute max) are requested. Papers must be submitted electronically in PDF format through **www.biocas2018.org.**

**Important Dates**
Monday, April 23, 2018: Special Session Proposal Deadline
Monday, June 11, 2018: Regular Paper Submission Deadline
Monday, July 16, 2018: Live Demo Session deadline
Monday, August 13, 2018: Author Notification Date
Friday, August 31, 2018: Author Registration/Final Paper Submission Deadline

# PUBLICATIONS

## IEEE Solid-State Circuits Letters -

## Officially Launches

We're happy to announce that our new publication, IEEE Solid-State Circuits Letters, has launched. We are now accepting paper submissions.

**For more information, visit:**
**http://sscs.ieee.org/publications/ieee-solid-state-circuits-letters-ssc-l**

**For paper submission, visit:**
**https://mc.manuscriptcentral.com/ssc-l**

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## The latest in SSCS Flagship Publications...

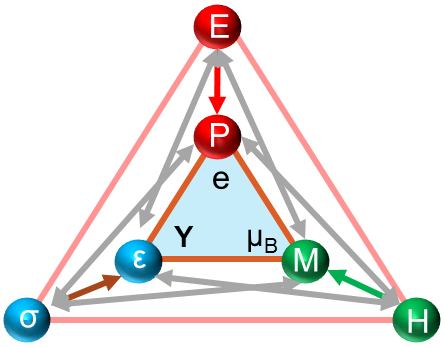

### IEEE Journal of Solid-State Circuits

### Vol. 52, Issue 11, November 2017

| |
|---|
| **Rail-to-Rail-Input Dual-Radio 64-Channel Closed-Loop Neurostimulator**<br>*Hossein Kassiri ; Muhammad Tariqus Salam ; Mohammad Reza Pazhouhandeh ; Nima Soltani ; Jose Luis Perez Velazquez ; Peter Carlen ; Roman Genov* |
| **An 80-mVpp Linear-Input Range, 1.6- GÎ© Input Impedance, Low-Power Chopper Amplifier for Closed-Loop Neural Recording That Is Tolerant to 650-mVpp Common-Mode Interference**<br>*Hariprasad Chandrakumar ; Dejan Marković* |
| **A 1.4-m Î© -Sensitivity 94-dB Dynamic-Range Electrical Impedance Tomography SoC and 48-Channel Hub-SoC for 3-D Lung Ventilation Monitoring System**<br>*Minseo Kim ; Jaeeun Jang ; Hyunki Kim ; Jihee Lee ; Jaehyuck Lee ; Jiwon Lee ; Kyoung-Rog Lee ; Kwantae Kim ; Yongsu Lee ; Kyuho Jason Lee ; Hoi-Jun Yoo* |
| **A Pixel Pitch-Matched Ultrasound Receiver for 3-D Photoacoustic Imaging With Integrated Delta-Sigma Beamformer in 28-nm UTBB FD-SOI**<br>*Man-Chia Chen ; Aldo Peña Perez ; Sri-Rajasekhar Kothapalli ; Philippe Cathelin ; Andreia Cathelin ; Sanjiv Sam Gambhir ; Boris Murmann* |
| **A Fully Integrated CMOS Fluorescence Biochip for DNA and RNA Testing**<br>*Arun Manickam ; Rituraj Singh ; Mark W. McDermott ; Nicholas Wood ; Sara Bolouki ; Pejman Naraghi-Arani ; Kirsten A. Johnson ; Robert G. Kuimelis ; Gary Schoolnik ; Arjang Hassibi* |
| **64-QAM 60-GHz CMOS Transceivers for IEEE 802.11ad/ay**<br>*Rui Wu ; Ryo Minami ; Yuuki Tsukui ; Seitaro Kawai ; Yuuki Seo ; Shinji Sato ; Kento Kimura ; Satoshi Kondo ; Tomohiro Ueno ; Nurul Fajri ; Shoutarou Maki ; Noriaki Nagashima ; Yasuaki Takeuchi ; Tatsuya Yamaguchi ; Ahmed Musa ; Korkut Kaan Tokgoz ; Teerachot Siriburanon ; Bangan Liu ; Yun Wang ; Jian Pang ; Ning Li ; Masaya Miyahara ; Kenichi Okada ; Akira Matsuzawa* |

## IEEE Journal on Exploratory Solid-State Computational Devices and Circuits

## 2017 Highlights




**MagCAD: Tool for the Design of 3-D Magnetic Circuits**
Fabrizio Riente ; Umberto Garlando ; Giovanna Turvani ; Marco Vacca ; Massimo Ruo Roch ; Mariagrazia Graziano

**A Thermodynamic Perspective of Negative-Capacitance Field-Effect Transistors**
Sou-Chi Chang ; Uygar E. Avci ; Dmitri E. Nikonov ; Ian A. Young

**An Energy-Efficient Digital ReRAM-Crossbar-Based CNN With Bitwise Parallelism**
*Leibin Ni ; Zichuan Liu ; Hao Yu ; Rajiv V. Joshi*

**Nonboolean Pattern Recognition Using Chains of Coupled CMOS Oscillators as Discriminant Circuits**
Vahnood Pourahmad ; Sasikanth Manipatruni ; Dmitri Nikonov ; Ian Young ; Ehsan Afshari

**Compact Modeling of Distributed Effects in 2-D Vertical Tunnel FETs and Their Impact on DC and RF Performances**
Jie Min ; Peter M. Asbeck

**Nonvolatile Spintronic Memory Array Performance Benchmarking Based on Three-Terminal Memory Cell**
Chenyun Pan ; Azad Naeemi

**CoMET: Composite-Input Magnetoelectric- Based Logic Technology**
*Meghna G. Mankalale ; Zhaoxin Liang ; Zhengyang Zhao ; Chris H. Kim ; Jian-Ping Wang ; Sachin S. Sapatnekar*

**Electrical-Spin Transduction for CMOS-Spintronic Interface and Long-Range Interconnects**
*Rouhollah Mousavi Iraei ; Sasikanth Manipatruni ; Dmitri E. Nikonov ; Ian A. Young ; Azad Naeemi*

JxCDC papers listed in order of popularity can be found online **HERE**.

For paper submission details, click **HERE**.

## Seeking News

Please send any chapter news or happenings (Distinguished Lecturer visits, events hosted by your SSCS chapter, awards received by members, etc) to Abira Sengupta, SSCS Magazine News Editor, for inclusion in an upcoming issue of the magazine. Please email - **Abira.Sengupta@ieee.org**. We look forward to receiving your news articles!

**For more chapter news, check out the Summer 2017 issue of the Solid-State Circuits Magazine.**

# FEEDBACK

Let us know what you think! Please **email us** to send us your comments about the newsletter, what you would like to see included each month, or any other comments.

**CLICK HERE TO VISIT OUR WEBSITE**

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