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May 2018

NEWS

UPCOMING SSCS WEBINARS

These webinars are part of a two-part series on time-based circuits



PART 1

Time-Based Circuits - not just the Single Slope!

Wednesday, June 6, 2018

12:00 PM ET

Presenter: Matt Straayer, Maxim Integrated Inc.

Abstract: Compared to circuits utilizing voltage or current to convey analog signals, time-based circuits offer unique attributes, ranging from simple, area efficient quantization to more complex techniques for time-based processing such as integration, interpolation, and noise shaping. Although time-based circuits are not new, the availability of fast, low-power transistors in advanced process nodes, combined with the challenges of traditional analog design techniques, has renewed interest in time as a signal domain both in academia and in industry. This talk will look at some obvious and more subtle differences between voltage and time-based circuits, and discuss tradeoffs in the context of application requirements. A few advanced state-of-the-art time-based circuits will motivate the audience to consider how time-based circuits can be a useful tool for their own designs.

[CLICK HERE TO REGISTER](#)

PART 2



Applications of Time-Based Circuits in Data Conversion, Filtering, and Control

Wednesday, July 11, 2018

11:00 AM ET

**Presenter: Pavan K. Hanumolu,
University of Illinois, Urbana-Champaign**

Abstract: In the 2nd part of this 2 part series on time based circuits, I will present time based signal representation as an alternative to classical voltage or charge based signal representations. I will then show how this representation enables the implementation of fundamental building blocks such as integrators using mostly digital circuits. Finally, I will present case studies of time based analog filters, analog to digital converters, and DC DC converters to highlight the advantages, opportunities, and drawbacks of the time based approach.

CLICK HERE TO REGISTER

Please note that moving forward all SSCS webinar registrations will be processed through the SSCS Resource Center. SSCS webinars are a members-only benefit. If you are not an SSCS member and would like to attend an SSCS webinar, a fee will be charged. In addition, PDH's for SSCS webinars will now be processed through the SSCS Resource Center. PDH's will still remain free.

If you have any questions about this policy, please email sscs-staff@ieee.org.



Introducing - SSCS Chip Chat

SSCS' educational programming has expanded to include a podcast called SSCS Chip Chat. This interview style podcast focuses on the stories of engineers and scientists behind the integrated circuits that power the world.

The podcast can be listened to by searching SSCS Chip Chat in the Apple Podcast App or whatever podcast app you use for your mobile device.

You can also listen to the podcast online. [Click here to listen!](#)

Episode 1: Dr. Gert Cauwenberghs



Women in Engineering Networking Event at VLSI Symposium 2018

Tuesday, June 19th
6 PM
TAPA 3 Room
Hilton Hawaii Village, Honolulu, Hawaii

Special Guest: Barbara De Salvo, Chief Scientist and Deputy Director of CEA-Leti, Grenoble, France

Build and sustain a community among women in engineering. Meet and network with female luminaries in engineering.

This event is open to all genders and everyone in all phases of their careers.

[CLICK HERE TO RSVP](#)

Walk-in's are also welcome!

SSCS & EDS Joint Mentoring Session at VLSI Symposium 2018

Wednesday, June 20th
6 PM
TAPA 3 Room, Hilton Hawaiian Village,
Honolulu, Hawaii



- Complimentary event for all students, faculty, & engineers within 15 years of their first degree, even if not registered for the conference.
- Leading experts from industry and academia, IEEE SSCS & EDS Executives and Distinguished Leaders will share their experiences
- 1 on 1 answers to all your questions on publications, entrepreneurship, industry vs. academia and career coaching.
- Free T-Shirt to event attendees and all student participants get complimentary SSCS & EDS membership.
- Learn about SSCS & EDS member benefits for young engineers & students

[CLICK HERE TO RSVP](#)

Walk-in's are also welcome!

SSCS Members can Join CASS for Just \$5

As a member of the IEEE Solid-State Circuits Society, you can add [IEEE Circuits and Systems Society \(CASS\)](#) annual membership for just \$5.



More than 20% of SSCS members are already members of CASS.

If you have not yet renewed for 2018, join CASS for just \$5 by entering promotion code SSCXCAS2018 at checkout. If you have already renewed for 2018, sign in with your [IEEE account](#) and the discounted CASS membership will be present in your cart.

EDUCATION

June 2018 Distinguished Lectures

CHAPTER	TALK DETAILS	DATE	LOCATION
SSCS Montreal - Sorin Voinigescu	Circuit Topologies and Design Methodologies for High Data-Rate mm-Wave Radio Transceivers in SOI and FDSOI CMOS	June 1, 2018	Polytechnique Montreal Click here for more information
SSCS Japan & SSCS Kansai	Higher Performance MEMS Inertial Sensors	June 15, 2018	University of Tokyo Click here for more information

CONFERENCES

Upcoming Conferences

<u>2018 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)</u> Philadelphia, PA	June 10 - 12, 2018
<u>2018 IEEE Symposium on VLSI Technology</u> Honolulu, HI	June 18 - 22, 2018
<u>2018 IEEE Symposium on VLSI Circuits</u> Honolulu, HI	June 18 - 22, 2018
<u>2018 IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED)</u> Seattle, WA	July 23 - 25, 2018
<u>ESSCIRC/ESSDERC 2018 - 44th European Solid-State Circuits Conference/44th European Solid-State Device Research Conference</u> Dresden, Germany	September 3 - 6, 2018
<u>2018 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)</u> San Diego, CA	October 14 - 17, 2018
<u>2018 IEEE Biomedical Circuits and Systems Conference (BioCAS)</u>	October 17 - 19, 2018

Cleveland, OH	
<u>2018 IEEE Asian Solid-State Circuits Conference (A-SSCC)</u> Tainan, Taiwan	November 5 - 7, 2018

ISSCC in the Media

Recently, two articles about ISSCC 2018 were published in IEEE Transmitter:

Silicon Engineering a Social World (Part 1) - [Click here to read the article](#)

Silicon Engineering a Social World (Part 2) - [Click here to read the article](#)

2018 RFIC Symposium

June 10 - 12, 2018
Philadelphia, Pennsylvania

We cordially invite you to participate in the [2018 IEEE Radio Frequency Integrated Circuits Symposium \(RFIC 2018\)](#). This international event will be held in Philadelphia, PA from 10-12 June, 2018. The RFIC Symposium is the premier integrated circuit (IC) design conference focused exclusively on the latest advances in RF, microwave, and millimeter-wave IC technologies and designs, as well as innovations in high-frequency analog/mixed-signal ICs and ultra-low power radios. With a wide range of papers from industry and academia, all attendees will find plenty of relevant and technically interesting topics to choose from!

The RFIC Symposium is an annual IEEE conference that is co-located with the International Microwave Symposium (IMS), ARFTG, and the Industry Exhibition to form "Microwave Week", the largest worldwide RF/microwave technical meeting of the year. This year, the Microwave week key themes are "Microwaves, Medicine, and Mobility", and the 2018 International Microwave Biomedical Conference (IMBioC) will be part of the Microwave Week in parallel to IMS, RFIC, and ARFTG. The Microwave Week will be held at the Pennsylvania Convention Center in Philadelphia, PA. In addition to the vast array of technical content, attendees will have the opportunity to interact with world experts, expand their networks, and leave invigorated with new ideas and a drive to innovate.

The 2018 RFIC Symposium will begin on Sunday, 10 June 2018, with 12 RFIC focused workshops (8 full day and 4 half day). In addition, there will be several joint RFIC/IMS workshops on Sunday and Monday. These workshops cover a wide range of advanced topics in RFIC technology and IC design, including 5G systems and beyond.

12 Sunday RFIC Focused Workshops include the following topics:

- RFIC Design in CMOS FinFET and FD-SOI
- ICs for Quantum Computing and Quantum Technologies
- 5G mm-Wave Power Amplifiers, Transmitters, and Beamforming Techniques with Massive MIMO
- eXtreme-bandwidth architecture for RF and mmW transceivers in nanoscale CMOS
- Integrated mm-wave & THz sensing technology for automotive, industrial and healthcare
- Advanced integrated RF filtering circuits and techniques

- Synthesizer Design and Frequency Generation/Synchronization Schemes for High-Performance Wireless Systems
- High-performance WLAN Transceiver Design and Calibration Techniques
- High Efficiency Power Amplification for Emerging Wireless Communication Solutions from Devices to Circuits and Systems
- Millimeter-wave Systems, Manufacturing, Packaging and Built-in Self-Test
- Towards Direct Digital RF Transceivers
- Ultra Low-Power Transceiver SoC Designs for IoT Applications

Following the full day of workshops, the RFIC Plenary Session will be held on Sunday evening beginning with conference highlights, the presentation of the Student Paper Awards, and the Industry Paper Awards. The plenary session talks begin with Mr. Zachary J. Lemnios, Vice President of Science, Technology, and Government programs at IBM research, who will talk about "Compact Silicon Integrated mmWave Circuits: From Skepticism to 5G and Beyond"; the second talk will be given by NXP's Automotive Chief Technology Officer, Mr. Lars Reger, who will share his vision on "The road ahead for autonomous cars - what's in for RFIC". Immediately following the plenary session will be the RFIC reception that will highlight our industry showcase and student paper finalists in an engaging social and interactive technical evening event supported by the RFIC Symposium corporate sponsors. You will not want to miss the RFIC Reception this year!

On Monday and Tuesday, RFIC will have multiple tracks of oral technical paper sessions as well as the popular Interactive Forum poster session.

17 Technical Paper Sessions on Monday and Tuesday include the following topics:

- Building Blocks for 5G Transceivers
- Advances in Packaging, Modeling and Optical Phased Arrays
- Techniques for High-Performance Frequency Synthesis
- 28 GHz Phased Arrays, Beamformers and Sub-Components for 5G Applications
- Technology Optimization for RF Applications
- ADC-Based RF/Mixed-Signal Systems and Wireline Transceiver Techniques
- RF Front-Ends for Emerging Wireless Paradigms
- Mixed Signal Transmitters and Power Amplifiers
- cm/mm-Wave CMOS Integrated Phased-Array Building Blocks
- Ultra-Low Power Radios for Security, Ranging and Connectivity
- Silicon Integrated mm-Wave Transmitters
- Highly Efficient mm-Wave Oscillators with Wide Tuning Range
- mm-Wave Power Amplifiers
- Submillimeter Wave and Terahertz ICs
- mm-Wave Radar and Beamforming Transceivers
- mm-Wave LNAs and RF Receiver Front-Ends
- Wireless Transceivers and Transmitters for Connectivity and Cellular

Enlightening lunchtime panels focusing on the Microwave Week key themes will be featured on both days. The Monday panel session, titled "How will the future self-driving cars see? Lidar vs Radar", will cover the state of the art in radar and lidar technologies and attempt to draw contrasts between the two approaches in the context of self-driving cars. The Tuesday panel session, titled "Can a residential wireless Gbps internet connection compete with wired alternatives?", will convene expert panelists to discuss some of the technology advancements that are enabling Gbps internet connections and will debate the merits of both the wired and wireless technology alternatives. Please make sure to bring your engaging opinions and questions to both panel sessions and they will be highly interactive!

The 5G Summit technical sessions on Tuesday will provide high-level 5G overview presentations that will complement the 5G-focused RFIC technical sessions on Monday morning. A separate registration will be required for the 5G Summit sessions. On behalf of the RFIC Steering and Executive Committees, we welcome you to join us at the 2018 RFIC Symposium in Philadelphia, Pennsylvania!

Please visit the RFIC 2018 website (<http://rfic-ieee.org/>) for more details and updates.

2018 Symposia on VLSI Technology and Circuits

June 18 - 22, 2018

Honolulu, Hawaii

***Registration is open now, and the deadline for the early discount is
May 24th.***

The [2018 Symposia on VLSI Technology & Circuits](#) will deliver a unique perspective built around the theme of "Technology, Circuits & Systems for Smart Living." The Symposia program integrates advanced technology developments, innovative circuit design, and the applications that they enable as part of our global society's adoption of smart, connected devices and systems that change the way humans interact with each other.

This weeklong conference is packed with technical presentations, a demonstration session, panel discussions, and focus sessions. There will be two full-day short courses on "Designing for the Next Wave of Cloud Computing" and "Bio-Sensors, Circuits, and Systems for Wearable and Implantable Medical Devices." The plenary sessions will explore the impact of circuits on higher-level systems, including Bill Dally of nVidia speaking on artificial intelligence, and Tsuneo Komatsuzaki of SECOM discussing security service platforms.

New to the Hawaii Symposia is a Friday Forum, June 22nd, on "Machine Learning Today and Tomorrow", which will include talks from academia and industry thought leaders, providing insight into the complex and dynamic landscape of machine-learning algorithms, their uses, and the technological trends driving their progression.

We look forward to seeing you all at 2018 VLSI Symposia in Honolulu!

[Click here for more information.](#)

Call for Participation International Symposium on Low Power Electronics and Design (ISLPED'18)

Bellevue, Washington

July 23-25, 2018

ISLPED is the world's premier event on low power design. It is sponsored by the IEEE Circuits and Systems Society and the ACM Special Interest Group on Design Automation.

The technical program highlights the following areas:

* Machine Learning - Inference

- * Hardware Security
- * Approximate Computing
- * SRAM and 3D Integration
- * Energy-efficient Training of NNs
- * Non-Volatile Memory - Technology to System
- * Architectural Techniques for Energy-Efficiency
- * Mobile Applications
- * Special Session on SRC JUMP Centers

A preliminary list of the accepted papers is available on the conference website. As with prior years, the program will also include several keynote presentations, special sessions, the annual design contest, as well as a rich social program.

Early registration and discounted hotel rates are available until June 15, 2018.

For more information and registration, visit: <http://www.islped.org/>

CALL FOR PAPERS

BioCAS 2018: Call for Papers ***Biomedical Circuits and Systems Conference***

October 17 - 19, 2018
Cleveland, OH

BioCAS 2018 is a premier international forum for presenting the interdisciplinary research and development activities at the crossroads of medicine, life sciences, physical sciences and engineering that shape tomorrow's medical devices and healthcare systems.

This conference brings together members of our communities to broaden their knowledge in emerging areas of research at the interface of the life sciences and the circuits and systems engineering. The three-day single-track program for BioCAS 2018 is multidisciplinary in topics including but not limited to:

Biomedical Technologies

- * Assistive, Rehabilitation, and Quality of Life Technologies
- * Biofeedback, Neuromodulation, and Closed-Loop Systems
- * Bio-Inspired and Neuromorphic Circuits and Systems
- * Biosensor Devices and Interface Circuits
- * Biotelemetry and Energy Harvesting/Scavenging Circuits and Systems
- * Body Area/Sensor Network and Wireless/Wearable Health Monitoring
- * Electronics for Neuroscience
- * Implantable Medical Electronics
- * Lab-on-Chip and BioMEMS

Biomedical Applications

- * Point-of-Care Technologies for Healthcare
- * Biomedical Imaging and Image Processing
- * Biosignal Recording, Processing, and Machine Learning
- * Genomics and Systems Biology
- * Human-Machine Interfaces
- * Medical Information Systems and Bioinformatics

Submission Guidelines

The complete 4-page paper (in standard IEEE double-column format), including the title, authors' names, affiliations and e-mail addresses, as well as a short abstract and an optional demonstration video link (3 minute max) are requested. Papers must be submitted electronically in PDF format through www.biocas2018.org.

Important Dates

Monday, June 11, 2018: Regular Paper Submission Deadline

Monday, July 16, 2018: Live Demo Session deadline

Monday, August 13, 2018: Author Notification Date

Friday, August 31, 2018: Author Registration/Final Paper Submission Deadline

A-SSCC 2018: Call for Papers IEEE Asian Solid-State Circuits Conference

Conference Theme: Silicon Enabling Mobile Intelligence

The miniaturized silicon technology enabled big success in the realization of software solutions such as machine learning, big data, virtual and augmented reality in the image and speech recognition, the medical diagnosis and the autonomous driving automobiles. The current software solutions, however, consume huge power by employing cloud computers along with many graphic processing units and a large amount of memory. Nowadays, the integrated circuit design community tries to develop efficient low-power mobile intelligence solutions by taking challenges in the design of digital and analog circuits, processor architecture, and system for compact IoT devices.

Prospective authors are invited to submit four-page or two page (NEW) manuscripts, including figures, tables, and references to the official A-SSCC 2018 website. The two-page submission can include two-page supplements with figures and figure captions. All papers will be handled and reviewed electronically.

Papers are solicited in the following categories:

Regular Session

- 1. Analog Circuits & Systems:** Amplifiers, comparators, switched capacitor circuits, continuous-time & discrete-time filters, voltage/current references; DC- DC converters, power-control circuits; IF/baseband analog circuits, AGC/VGA; non-linear analog circuits.
- 2. Data Converters:** Nyquist-rate and oversampling A/D and D/A converters, time-to-digital converters, and capacitance-to-digital converters; sub-circuits for data converters including sample-and-hold circuits, calibration circuits, etc.
- 3. Digital Circuits & Systems:** Design, fabrication, and test of digital VLSI systems; high-speed low-power digital circuits, power-reduction and management methods for digital VLSI, ultra-low-voltage and sub-threshold logic design; leakage reduction techniques; clock distribution, I/O circuits, reconfigurable logic-array circuits; supply/substrate noise measurement and cancellation for digital VLSI, variation and fault-tolerant circuits.
- 4. SoC & Signal Processing Systems:** System-on-chip(including 3D integration), microprocessors, network processors, baseband communication processing system & architectures, system-level power management; multimedia and recognition processing systems; cryptographic, security, machine-learning, deep-learning, and neuromorphic circuits and systems; bio-medical/neural-network processors and sensor network systems.
- 5. RF:** Receivers/transmitters/transceivers for wireless systems; narrowband RF, ultra-wideband and millimeter-wave circuits; circuits and building-blocks including RF front-end, LNA, mixer, power amplifiers, VCOs, frequency synthesizers, RF filters, RF switches, power detectors, active antennas.
- 6. Wireline:** Receivers/transmitters/transceivers for wireline systems; optical/electrical data links and backplane transceivers; power-line communication; clock generation circuits, PLL,

DLL, spread-spectrum clock generation; building blocks for high-speed wireline communication; analog-digital mixed-mode circuits.

7. Emerging Technologies and Applications: Advanced system designs and circuit solutions for technologies and applications including state-of-the-art devices and packaging technologies; flexible and printable electronics; smart sensors and transducers; MEMS for analog, RF, and sensor applications; image sensors and displays; energy harvesting systems; transceiver systems; medical/bio-electronics/bio-inspired chip design and silicon systems.

8. Memory: Volatile and Non-volatile memory; new memory designs for 3D/2D architectures, emerging devices such as resistive-/phase change-/magnetic-/ferro-electric- memory devices; data storage and multi-bit-cell memory design; cache-memory system, multi-port memory, memory subsystem, processing in memory, and CAM design; yield-enhancing and ECC techniques; memory testing and built-in self-test.

Special Session

1. Industry Program: This special category accepts only papers based on state-of-the-art industrial products. Strong emphasis on systems realized by silicon chips is encouraged. The papers should cover architecture, circuits, process technology, packaging and testing, including characterization results, die and system photos, as well as product demos.

2. Student Design Contest: A student design contest is held among the accepted papers with system prototypes or measurement results of which operations can be demonstrated on-site. Refer to the web for further information.

3. FPGA Session (NEW) : This session accepts papers describing FPGA implementation with novel algorithm and/or architecture. The demo results(eg. video or slide) must be included in the paper submission. The authors of accepted papers are required to participate in demo sessions.

Papers related to integrated circuits for intelligent systems are highly solicited. Papers on low-power and/or low-voltage approaches, signal integrity, noise, test, and manufacturability for all the above categories are welcomed. Measurement results are highly recommended, especially for analog, and RF categories. Design methodologies for SiP, and SoC are included in the scope of the conference; the papers only describing CAD tools and CAD algorithms are not considered. Authors must follow detailed instructions provided within the "Authors" section of the website, including the Authors' Guide and Pre-publication Policy. The technical content beyond the abstract of the accepted paper must not be announced, published, or in any way put in the public domain prior to the Conference. Extended versions of selected papers from the Conference will be published in a Special Issue of the IEEE Journal of Solid-State Circuits.

Important Dates

Paper Submission: June 3, 2018 (20:00 GMT)

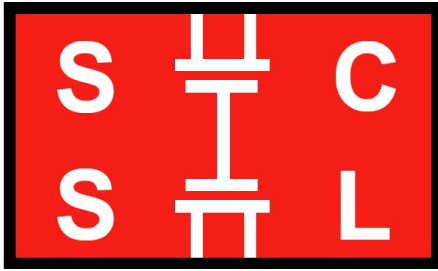
Acceptance Notification: August 6, 2018

Final Paper Submission: September 9, 2018

PUBLICATIONS

The latest in SSCS Flagship Publications...

IEEE Solid-State Circuits Letters



Volume 1, Issue 3, March 2018

[A Neuromodulator Frontend With Reconfigurable Class-B Current and Voltage Controlled Stimulator](#)

Michael Haas ; Patrick Vogelmann ; Maurits Ortmanns

[A 183 GHz Desensitized Unbalanced Cascode Amplifier With 9.5-dB Power Gain and 10-GHz Band Width and -2 dBm Saturation Power](#)

Hamid Khatibi ; Somayeh Khiyabani ; Ehsan Afshari

[Fast Cascoded Quenching Circuit for Decreasing Afterpulsing Effects in 0.35- u m CMOS](#)

R. Enne ; B. Steindl ; M. Hofbauer ; H. Zimmermann

[A 5.8-GHz Bidirectional and Reconfigurable RF Energy Harvesting Circuit With Rectifier and Oscillator Modes](#)

Soroush Dehghani ; Shahriar Mirabbasi ; Thomas Johnson

[A 174 pW-488.3 nW 1 S/s-100 kS/s All-Dynamic Resistive Temperature Sensor With Speed/Resolution/Resistance Adaptability](#)

Haoming Xin ; Martin Andraud ; Peter Baltus ; Eugenio Cantatore ; Pieter Harpe

[A 0.009 mm² Wide-Tuning Range Automatically Placed-and-Routed ADPLL in 14-nm FinFET CMOS](#)

David M. Moore ; Thucydides Xanthopoulos ; Scott Menering ; David D. Wentzloff



IEEE Journal of Solid-State Circuits

Vol. 53, Issue 6, June 2018

[Wideband Dual-Injection Path Self-Interference Cancellation Architecture for Full-Duplex Transceivers](#)

Tong Zhang ; Chenxin Su ; Ali Najafi ; Jacques Christophe Rudell

[A Reconfigurable Architecture Using a Flexible LO Modulator to Unify High-Sensitivity Signal Reception and Compressed-Sampling Wideband Signal Detection](#)

Tanbir Haque ; Matthew Bajor ; Yudong Zhang ; Jianxun Zhu ; Zaron A. Jacobs ; Robert Blayne Kettlewell ; John Wright ; Peter R. Kinget

[Design and Analysis of a Programmable Receiver Front End Based on Baseband Analog-FIR Filtering Using an LPTV Resistor](#)

Sameed Hameed ; Sudhakar Pamarti

<p>A Chopping Switched-Capacitor RF Receiver With Integrated Blocker Detection Yang Xu ; Peter R. Kinget</p>
<p>A 0.18-V 382-Î¼W Bluetooth Low-Energy Receiver Front-End With 1.33-nW Sleep Power for Energy-Harvesting Applications in 28-nm CMOS Haidong Yi ; Wei-Han Yu ; Pui-In Mak ; Jun Yin ; Rui P. Martins</p>
<p>Design of 1.8-mW PLL-Free 2.4-GHz Receiver Utilizing Temperature-Compensated FBAR Resonator Keping Wang ; Lei Qiu ; Jabeom Koo ; Richard Ruby ; Brian Otis</p>
<p>A Near-Zero-Power Wake-Up Receiver Achieving $\hat{\sim}$69-dBm Sensitivity Po-Han Peter Wang ; Haowei Jiang ; Li Gao ; Pinar Sen ; Young-Han Kim ; Gabriel M. Rebeiz ; Patrick P. Mercier ; Drew A. Hall</p>
<p>A 500-MHz Bandwidth 7.5-mVpp Ripple Power-Amplifier Supply Modulator for RF Polar Transmitters Chul Kim ; Chang-Seok Chae ; Young-Sub Yuk ; Chris M. Thomas ; Yi-Gyeong Kim ; Jong-Kee Kwon ; Sohmyung Ha ; Gert Cauwenberghs ; Gyu-Hyeong Cho</p>
<p>Split-Array, C-2C Switched-Capacitor Power Amplifiers Zhidong Bai ; Ali Azam ; Dallas Johnson ; Wen Yuan ; Jeffrey S. Walling</p>
<p>Power-Efficient W -Band (92-98 GHz) Phased-Array Transmit and Receive Elements With Quadrature-Hybrid-Based Passive Phase Interpolator Sadia Afroz ; Hyunchul Kim ; Kwang-Jin Koh</p>
<p>A Self-Tuning Resonant-Inductive-Link Transmit Driver Using Quadrature Symmetric Delay Trimmable Phase-Switched Fractional Capacitance Henry Kennedy ; Rares Bodnar ; Teerasak Lee ; William Redman-White</p>
<p>A 2.4-GHz RF Fractional- N Synthesizer With BW =0.25fREF Long Kong ; Behzad Razavi</p>
<p>Digital Fractional- N PLLs Based on a Continuous-Time Third-Order Noise-Shaping Time-to-Digital Converter for a 240-GHz FMCW Radar System Mehmet Batuhan Dayanik ; Michael P. Flynn</p>
<p>0.04-mm² 103-dB-A Dynamic Range Second-Order VCO-Based Audio ÎfÎ" ADC in 0.13-Î¼m CMOS Fernando Cardes ; Eric Gutierrez ; Andres Quintero ; Cesare Buffa ; Andreas Wiesbauer ; Luis Hernandez</p>
<p>A Bypass-Switching SAR ADC With a Dynamic Proximity Comparator for Biomedical Applications Tzu-Yun Wang ; Hao-Yu Li ; Zong-Yu Ma ; Yang-Jing Huang ; Sheng-Yu Peng</p>
<p>A 12-bit 150-MS/s Sub-Radix-3 SAR ADC With Switching Miller Capacitance Reduction Kwuang-Han Chang ; Chih-Cheng Hsieh</p>
<p>A 12-Bit 1.6, 3.2, and 6.4 GS/s 4-b/Cycle Time-Interleaved SAR ADC With Dual Reference Shifting and Interpolation Jae-Won Nam ; Mohsen Hassanpourghadi ; Aoyang Zhang ; Mike Shuo-Wei Chen</p>
<p>An FFE Transmitter Which Automatically and Adaptively Relaxes Impedance Matching Minsoo Choi ; Sooeun Lee ; Myungguk Lee ; Ji-Hoon Lee ; Jae-Yoon Sim ; Hong-June Park ; Byungsub Kim</p>
<p>1.23-pJ/bit 25-Gb/s Inductor-Less Optical Receiver With Low-Voltage Silicon Photodetector Monireh Moayedi Pour Fard ; Odile Liboiron-Ladouceur ; Glenn E. R. Cowan</p>
<p>Low-Jitter Multi-Output All-Digital Clock Generator Using DTC-Based Open Loop Fractional Dividers Ahmed Elkholy ; Saurabh Saxena ; Guanghua Shu ; Amr Elshazly ; Pavan Kumar Hanumolu</p>
<p>A 6.75-8.25-GHz $\hat{\sim}$250-dB FoM Rapid ON/OFF Fractional-N Injection-Locked Clock Multiplier Ahmed Elkholy ; Ahmed Elmallah ; Mostafa Gamal Ahmed ; Pavan Kumar Hanumolu</p>
<p>An EEG-NIRS Multimodal SoC for Accurate Anesthesia Depth Monitoring</p>

Unsoo Ha ; Jaehyuk Lee ; Minseo Kim ; Taehwan Roh ; Sangsik Choi ; Hoi-Jun Yoo

[0.293-mm² Fast Transient Response Hysteretic Quasi-V2DC-DC Converter With Area-Efficient Time-Domain-Based Controller in 0.35- \$\mu\$ m CMOS](#)

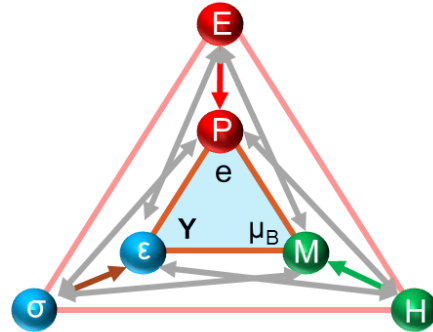
Dong-Hoon Jung ; Kiryong Kim ; Sunghwan Joo ; Seong-Ook Jung

[A Hysteretic Buck Converter With 92.1% Maximum Efficiency Designed for Ultra-Low Power and Fast Wake-Up SoC Applications](#)

Francesco Santoro ; Rüdiger Kuhn ; Neil Gibson ; Nicola Rasera ; Thomas Tost ; Helmut Graeb ; Bernhard Wicht ; Ralf Brederlow

IEEE Journal on Exploratory Solid-State Computational Devices and Circuits

2018 Early Access Papers



[Using Programmable Graphene Channels as Weights in Spin-Diffusive Neuromorphic Computing](#)

Jiaxi Hu ; Gordon Stecklein ; Yoska Anugrah ; Paul A. Crowell ; Steven J. Koester

[BCB Evaluation of High-Performance and Low-Leakage Three-Independent-Gate Field Effect Transistors](#)

Jorge Romero-Gonzalez ; Pierre-Emmanuel Gaillardon

[Tunnel FET Analog Benchmarking and Circuit Design](#)

Hao Lu ; Paolo Paletti ; Wenjun Li ; Patrick Fay ; Trond Ytterdal ; Alan Seabaugh

[Improving Energy Efficiency of Low Voltage Logic by Technology-Driven Design](#)

Kaushik Vaidyanathan ; Daniel H. Morris ; Uygur E. Avci ; Huichu Liu ; Tanay Karnik ; Hong Wang ; Ian A. Young

JxCDC papers listed in order of popularity can be found online [HERE](#).

For paper submission details, click [HERE](#).

Seeking News

Please send any chapter news or happenings (Distinguished Lecturer visits, events hosted by your SSCS chapter, awards received by members, etc) to Abira Sengupta, SSCS Magazine News Editor, for inclusion in an upcoming issue of the magazine. Please email -

Abira.Sengupta@ieee.org. We look forward to receiving your news articles!

For more chapter news, [check out](#) the Winter 2018 issue of the Solid-State Circuits Magazine.

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