Abstract: In large SoC's, data converters take a dominant position both from a performance point of view as well as from an energy consumption point of view. The past two decades have shown a strongly intensified search for more power efficient data converters, in particular power efficient ADCs. This presentation will focus on power efficiency of Nyquist-rate ADCs and discuss what has been proposed in open literature to reduce the energy consumption, both from a circuit point of view as well as from an architectural point of view. To get a good grasp of how circuit and architectural choices affect the power consumption, a method will be introduced that allows a quick estimation of the power consumption of an ADC, based on the required SNDR, the sampling frequency, the used technology as well as the chosen ADC architecture and circuit implementations. The proposed method enables a comparison based on these choices and can show what their impact is on the power efficiency, without going through the elaborate design of several architectures. It also shows which recent inventions made a large impact on power efficiency and how these inventions can also be of use in other architectures than the ones they have been introduced in.
Biography: Klaas Bult received an MSc. and a PhD. degree from Twente University in 1984 and 1988 respectively. From 1988 to 1994 he worked as a Research Scientist at Philips Research Labs, where he worked on Analog CMOS Building Blocks, mainly for application in Video and Audio Systems. In 1993-1994 he was also a part-time professor at Twente University. From 1994 to 1996 he was an associate professor at UCLA, where he worked on Analog and RF Circuits for Mixed-Signal Applications. In the same period he was also a consultant with Broadcom Corporation, in Los Angeles, CA and later in Irvine, CA, during which he started the Analog Design Group at Broadcom. In 1996 he joined Broadcom full-time as a Director, responsible for Analog and RF Circuits for embedded applications in broadband communication systems. In 1999 he became a Sr. Director and started Broadcom's Design Center in Bunnik, The Netherlands. In 2005 he was appointed Vice President and CTO of Central Engineering. As of 2016 he's an independent consultant Analog IC Design, operating from The Netherlands. Klaas Bult is an author of more than 60 international publications and holds more than 60 issued US patents. He is a Broadcom Fellow, an IEEE Fellow, was awarded the Lewis Winner Award for outstanding conference paper on ISSCC 1990, 1992 and 1997, was co-recipient of the Jan Van Vessem best European Paper Award at ISSCC 2004 and the Distinguished paper Award of ISSCC 2014. He was also awarded the ISSCC Best Evening Panel Award in 1997 and 2006 and the Best Forum Speaker Award at ISSCC 2011. Klaas Bult has served more than 12 years on the ISSCC Technical Program Committee, 18 years on the ESSCIRC Technical Program Committee and 7 years as a member of the ESSCIRC/ESSDERC Steering Committee.

2020 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium

We invite you to join us in the 2020 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, to be held as a virtual symposium beginning on Tuesday 4 August 2020 with the plenary Session.

A single registration will allow attendees to access all Microwave Week content, including RFIC, IMS, ARFTG, the 5G Summit, a virtual exhibition, panel sessions, and more. This registration is free to all members of the IEEE Microwave Theory and Technique Society (MTTS). All Microwave Week content will be available on-line beginning on 4 August 2020 and lasting
through 30 September 2020.

Our technical program features 95 paper presentations organized within 21 technical sessions. These pre-recorded video presentations will be available to attendees on demand allowing attendees to digest all that our symposium has to offer.

A joint RFIC/IMS live-streamed panel session is scheduled for Wednesday, 5 August 2020 at 11:30 AM PDT. This panel will feature speakers discussing the important topic of "Who needs RF when we can digitize at the antenna interface". This topic is sure to interest both experts and newcomers alike. Finally, as students of today will be our leaders for tomorrow, the RFIC 2020, in partnership with IMS, offers opportunities for students to enhance their career growth and educational experiences. These include the RFIC student paper contest and the Three-Minute Thesis (3MT®) program.

On behalf of the RFIC Steering, Executive and Technical Committees, we welcome you to join us at the 2020 RFIC Symposium! Please visit the RFIC 2020 website (http://rfic-ieee.org/) for more details and updates.

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**SSCS Webinars for Young Excellence: Inaugural Webinar**

**Talk Title:** The Intersection of SSCS and AI -- A Tale of Two Journeys

**Abstract:** Today's technology landscape is dominated by the inescapable excitement of applications and possibilities enabled by artificial intelligence (AI). The timing could not be riper given the availability of big data, sufficient computing capability, and new machine learning techniques. How can aspiring students and professionals both young and seasoned in the field of solid-state circuits get into the action? In this webinar, we will hear two distinguished professors in cutting-edge AI research -- Vivienne Sze of MIT and Boris Murmann of Stanford -- offer their personal stories, insights, and perspectives of how they see circuits applied to the AI realm. They will provide their views of what AI is and isn't, address the types of AI problems they seek to solve and the angle they apply to leverage their established design expertise. Profs. Sze and Murmann will also offer their projections on future research opportunities and advice on how one can prepare to intersect them.

The webinar recording is now available on the [SSCS Resource Center](http://rfic-ieee.org/).

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- **Tutorials and Short Courses**: SSCS members have access to free tutorials and short courses from past years of ISSCC. Renowned experts in the field talk about new and ongoing developments in integrated circuits. [Click here to access.]
- **Webinars**: Monthly webinars are held for free for SSCS members on topics ranging from Analog/RF and future microprocessors to new biomedical applications. [Register for an upcoming webinar] or [view past webinars]
- **CONFedu Series**: The CONFedu series features short 10-minute talks from SSCS sponsored conferences including ISSCC, CICC, ESSCIRC, and VLSI. [Click here to access.]
- **SSCSx Lecture Series**: The first series of lectures is five parts and is presented by Prof. Behzad Razavi on Noise. [Click here to access.]

Educational credits (PDH's and CEU's) are available at a low cost for select products.

SSCS Educational content can be accessed via the [SSCS Resource Center] and the [SSCS YouTube Channel]. The material is free for Society members.

### EDUCATION

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SSCS-Sponsored Conferences: Proceedings

Click the links below to access the latest SSCS-Sponsored conference proceedings.

2019
- 2019 IEEE International Solid-State Circuits Conference (ISSCC)
- 2019 IEEE Custom Integrated Circuits Conference (CICC)
- 2019 IEEE Symposium on VLSI Circuits
- 2019 IEEE 45th European Solid-State Circuits Conference (ESSCIRC)

2020
- 2020 IEEE International Solid-State Circuits Conference (ISSCC)
- 2020 IEEE Custom Integrated Circuits Conference (CICC)

PUBLICATIONS

JxCDC Call for Papers: Special Topic on Tunneling FETs for Energy-Efficient Computing & Information Processing

A call for papers is now open for Special Topic on Tunneling FETs for Energy-Efficient Computing & Information Processing

Guest Editor:
Uygar Avci, Intel Corporation, uygar.e.avci@intel.com
Editor-in-Chief:
**Aims and Scope:**
The Tunneling Field-Effect Transistor (T-FET) is considered a future transistor option due to its steep-slope prospects and the resulting advantages in operating at low supply voltage (VDD).

Reducing supply voltage (VDD) while keeping a low leakage current and a reasonably high on-current is critical for minimizing energy consumption and improving the energy efficiency of computing and information processing. The thermal limit (Boltzmann’s Tyranny) of the MOSFET transistor subthreshold swing (SS) restricts lowering its threshold voltage (Vt), causing significant performance degradation at low VDD. A Tunneling Field Effect Transistor’s (T-FET) SS is not limited by this thermal tail and may perform better at low VDD. Since the first experimental proof of subthreshold swing (SS) < 60mV/dec, T-FET’s prospects have attracted the interest of researchers. Silicon’s large indirect bandgap and large carrier mass prevents Si T-FET from achieving high drive currents. But due to the availability of high-quality material together with years of know-how, Si and Si/Ge T-FETs have been studied initially, and showed the first of many devices with SS < 60mV/dec. III-V materials for T-FETs attracted attention next because of their low bandgap and carrier mass. While more challenging to fabricate, the broken bandgap hetero-junctions III-V T-FETs eventually showed the highest T-FET drive-current. Beyond III-V materials, Transition Metal Dichalcogenide and other 2D materials may provide a path in the future to high performance energy efficient transistors, thanks to thinner channels enabling better control of the tunneling field.

This call for papers on Tunneling FETs is for rapid publication of seminal results across the areas of T-FET materials, devices, and circuits for novel computation and information processing paradigms. Paper submissions with key insights into the advantages and challenges of specific T-FET device and material designs and circuit techniques are especially valued in order to guide the semiconductor industry and academia on a path toward more energy-efficient computing.

**Topics of Interest:**
Special Topic on Tunneling Field Effect Transistors (Tunneling FETs, T-FETs)

- N- and P- Tunneling FET experimental transistors demonstrating high performance at low supply voltage
- T-FET material and device design, including hetero-junction III-V materials, transition metal dichalcogenides, other two-dimensional materials and their hetero-junctions
- T-FET circuits for energy efficient computing and information processing
- Energy-Efficient computing and information processing with T-FET transistor circuits and architectures.

**Important Dates:**
Open for Submission: April 15th, 2020
Submission Deadline: June 30th, 2020
First Notification: August 1st, 2020
Revision Submission: August 21st, 2020
Final Decision: September 30th, 2020
Publication Online: December 1st, 2020

**Submission Guidelines:**
The IEEE Journal on Exploratory Solid-State Computational Devices and Circuits (JXCD) is an open access only publication:

Charge for Authors: $1,350 USD per paper.

Paper submissions must be done through the ScholarOne Manuscripts website: https://mc.manuscriptcentral.com/jxcd

Guidelines for papers and supplementary materials, as well as a paper template, are provided at this website.

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IEEE Journal of Solid-State Circuits

Vol. 55, Issue 5, May 2020

Special Issue on the 2019 RFIC Symposium

Introduction to the Special Section on the 2019 RFIC Symposium
Hongtao Xu

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