IEEE SOLID-STATE CIRCUITS SOCIETY

Where ICs are in IEEE

June 2016

Education

Upcoming Webinar

"Energy-efficient circuit technologies for sub-14nm microprocessors and SoCs: challenges and opportunities", Presented by Ram Krishnamurthy

Wednesday, July 13th @ 2:00 PM EST.

CLICK HERE TO REGISTER!

The webinar entitled **"Energy-efficient circuit technologies for sub 14nm microprocessors and SoCs: challenges and opportunities"** will be presented by Dr. Ram Krishnamurthy from Intel Corporation. Please follow the link above to register for the webinar. The webinar is free and open to all SSCS members.

Abstract: This seminar presents some of the prominent barriers to designing energy-efficient circuits in the sub-14nm technology regime and outlines new paradigm shifts necessary in next-generation multi-core microprocessors and systems-on-chip. Emerging trends and key challenges in sub-14nm design are outlined, including (i) device and on-chip interconnect technology projections, (ii) performance, leakage and voltage scalability, (iii) special-purpose hardware accelerators and reconfigurable co-processors for compute-intensive signal processing algorithms, (iv) fine-grain power management with integrated voltage regulators, and (v) resilient circuit design to enable robust variation-tolerant operation. Energy-efficient arithmetic and logic circuit techniques, static/dynamic supply scaling, on-die interconnect fabric circuits, ultra-low-voltage and near-threshold logic and memory circuit techniques, and multi-supply/multi-clock domain design for switching and leakage energy reduction are described. Special purpose hardware accelerators and data-path building blocks for enabling high GOPS/Watt on specialized DSP tasks such as encryption, graphics and media processing are presented. Power efficient optimization of microprocessors to span a wide operating range across high performance servers to ultra-mobile SoCs, dynamic on-the fly configurability and adaptation, and circuit techniques for active/standby-mode leakage reduction with robust low-voltage operability are reviewed. Specific chip design examples and case studies supported by silicon measurements and trade-offs will be discussed.

Upcoming Distinguished Lecturer Tours

JUNE/JULY			
June 27	SSCS Macau - Hideto Hidaka & Makoto Ikeda	University of Macau, China	Topic: "How Future Mobility Meets IT: Embedded Cyber-Physical System Designs Revisit Semiconductor Technology" Topic: "Basics of CMOS Image Sensors" For more details please click here
June 27	SSCS Hong Kong University of Science & Technology - Hideto Hidaka & Makoto Ikeda	Hong Kong University of Science & Technology, China	Topic: "Embedded Memory Technology Applications and Prospects in Embedded Systems" Topic: "Smart Image Sensors and Applications to 3D Range-Finding" For more details please click here
June 29	SSCS Vietnam - Hideto Hidaka	Ho Chi Minh City, Vietnam	Topic: "How Future Mobility Meets IT: Embedded Cyber-Physical System Designs Revisit Semiconductor Technology" For more details please click here
June 30	SSCS Shanghai - Hideto Hidaka	Fudan University, China	Topic: "Embedded Flash Memory for Embedded Systems: Technology, Circuits to Systems and MCU/SOC Applications" For more details please click here
July 28	SSCS Benelux - Peter Kinget	KU Leuven, Belgium	Topic: "Scaling Analog Circuits: Why and How" For more details please click here

For more information on upcoming Distinguished Lecturer Tours, CLICK HERE.

Conferences

Upcoming Conferences

2016 IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC) Hong Kong	August 3 - 5, 2016
2016 International Symposium on Low Power Electronics and Design (ISLPED) San Francisco	August 8 - 10, 2016
ESSCIRC-ESSDERC 2016 Lausanne, Switzerland	September 12 - 15, 2016
2016 IEEE Bipolar/BiCMOS Circuits and Technology Meeting - BCTM New Jersey	September 25 - 27, 2016
IEEE Dallas Circuits and Systems Conference 2016 Texas	October 9 - 10, 2016

DCAS 2016
Arlington, Texas
Paper Submission Deadline: June 30, 2016

CSICS 2016
Austin, Texas
Paper Submission Deadline (New and Extended Deadline): July 15, 2016

ISSCC 2017
San Francisco, California
Paper Submission Deadline: Sept 12, 2016

PUBLICATIONS

Highlights from the May/June Issue of Design & Test

(Volume 33, Issue 3)

Special Issue on Robust 3-D Stacked ICs

Perspective by Andres Takach, Mentor Graphics, on "High-Level Synthesis: Status, Trends, and Future Directions" - view free access article HERE

The 3-D Interconnect Landscape" by Eric Byne, IMEC - view free access article HERE

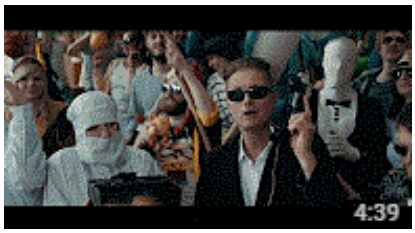
Interview by Gabe Moretti on "Accellera's DVCon Conferences Focus on the Community of Practicing Engineers" - view free access article HERE

Tutorial on "Toward Silicon-Based Cognitive Neuromorphic ICs - A Survey" - view free access article HERE

Tutorial on "PUFs as Promising Tools for Security in Internet of Things" - view free access article HERE

News

PartyProfs - The Circuit Song & Video



To motivate students and teach them the 3 basic analog circuits, Frank Ellinger, Andres Seidel, and Felix Schwarze from TU Dresden wrote a song and produced a music video called "The Circuit Song". The song strives to improve the public awareness of circuit design and understand that as a circuit designer, you can get cool and interesting jobs.

Please **click here** to view!

ISSCC 2017 Call for Papers: New Double-Blind Paper Review

New for ISSCC 2017: Double-Blind Paper Review. The paper selection for ISSCC 2017 will follow a double-blind review process, meaning that both the authors and reviewers will remain anonymous during the paper selection process. The ISSCC 2017 conference theme is "Intelligent Chips for a Smart World".

The Submission Deadline is Monday, September 12, 2016 at 3:00PM Eastern Daylight Time (19:00 GMT).

For more information, please **CLICK HERE.**

Seeking News

Please send any chapter news or happenings (Distinguished Lecturer visits, events hosted by your SSCS chapter, awards received by members, etc) to Abira Sengupta, SSCS Magazine News Editor for inclusion in an upcoming issue of the magazine. Please email - **Abira.Sengupta@ieee.org**. We look forward to receiving your news articles!

For more chapter news, check out the Spring 2016 issue of the Solid-State Circuits Magazine.

Feedback

Let us know what you think! Please **email us** to send us your comments about the newsletter, what you would like to see included each month, or any other comments.

CLICK HERE TO VISIT OUR WEBSITE

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