IEEE SOLID-STATE CIRCUITS SOCIETY

Where ICs are in IEEE

July 2017

NEWS

Upcoming Webinar

Demystifying Linear Time Varying Circuits

Presented by Shanthi Pavan

Friday, August 11 @ 11:00 AM (ET)

Professional Development Hours can be requested for this webinar

CLICK HERE TO REGISTER!

This webinar was prerecorded. Prof. Shanthi Pavan will be available during the presentation to answer questions regarding content, formulas, or theories. Please follow the link to register for the webinar which is free and open to all SSCS members.

Abstract : An analog/mixed-signal designer encounters time varying circuits everywhere - sample-and-holds, chopper stabilised amplifiers, mixers, switched-capacitor amplifiers and filters, discrete and continuous-time delta sigma modulators, N-path filters. The analysis of signals and noise in these circuits is often associated with messy

mathematics and algebra. This talk aims to demystify linear (periodically) time varying circuits. Starting from first principles, intuition behind various aspects of time-varying circuits and systems will be given. This intuition is illustrated with case studies of practical circuits and systems, like chopper-stabilised amplifiers and continuous-time delta-sigma modulators.

Bio : Shanthi Pavan obtained the B.Tech degree in Electronics and Communication Engg from the Indian Institute of Technology, Madras in 1995 and the Masters and Doctoral degrees from Columbia University, New York in 1997 and 1999 respectively. He is now with the Indian Institute of Technology-Madras, where he is a Professor of Electrical Engineering. His research interests are in the areas of high speed analog circuit design and signal processing. Dr.Pavan is the recipient of many awards for teaching and research, including the IEEE Circuits and Systems Society Darlington Best Paper Award and the Shanti Swarup Bhatnagar Award (from the Government of India). He has served as the Editor-in-Chief of the IEEE Transactions on Circuits and Systems: Part I - Regular Papers. He is a Fellow of the Indian National Academy of Engineering.

Are you looking for a way to help the next generation of electrical engineers?

Consider becoming a mentor through the IEEE Solid-State Circuits Society. Coach a student, graduate student, or young professional on entrepreneurship, offer publications advice, career coaching, and more. Shape the leaders of tomorrow. Mentoring can not only help a young professional, but also help you strengthen your leadership skills.

The SSCS Mentoring program will be flexible and cater to your busy schedule. Mentor at your own time, pace, and accord.

If you're interested, please click here to fill out an application. You will be paired with a mentee that shares your interests.

Upcoming ESSCIRC/ESSDERC Women in Circuits Luncheon

DATE: Tuesday, September 12th
TIME: 12 - 1:30 PM
LOCATION: ESSCIRC/ESSDERC Venue, Agora Learning Center, Leuven, Belgium
COST: € 10,00 (VAT included)

The luncheon registration fee can be added to ESSDERC/ESSCIRC registration fee. Register for the event by ticking "IEEE Women in Circuits Luncheon" on the ESSDERC/ESSCIRC Registration Form.

If you've already registered and would like to add the luncheon to your registration, please write an email to registration@sistemacongressi.com.

This luncheon is an opportunity to hear from an accomplished female leader in the field, Francoise Chombar (CEO, Melexis, Belgium) and to get to know fellow women in the profession and discuss a range of topics including leadership, work-life balance, and professional development. Both men and women eager to discuss and stimulate female presence in the field are more than welcome to attend.

For more information, please click here!

Do you Qualify for IEEE Senior Member Grade?

Senior Member is the highest grade for which IEEE members can apply. IEEE members can self-nominate or be nominated for Senior Member grade.

Benefits include professional recognition, a senior member plaque, leadership eligibility to hold executive IEEE volunteer positions, and more.

For more information on IEEE Senior Member Grade, please **click here**. If you have any questions or concerns, or need assistance obtaining references, email **sscs-membership@ieee.org**.

The next Senior Member review panel is in October. Become a Senior Member now!

BEGIN SENIOR MEMBER APPLICATION

The IEEE Design & Test Magazine is Now Available in Digital Version for Subscribers!

The IEEE Design & Test Magazine is now available in digital version for subscribers at no extra cost.

For fast browsing, subscribers also have access to the PDF version of the entire issue. The magazine is available through IEEE Xplore and the print version.

Not a subscriber? The complete electronic, digital, and print subscription is $54 USD a year for IEEE members of select societies (including the Solid-State Circuits Society).

Click here to subscribe!

New offering for SSCS members

In an effort to increase member benefits, SSCS has created the SSCS Resource Center. This informational hub will house technical information such as past webinar videos and slides, ISSCC tutorials and short courses, and more.

Top 5 Downloaded Products on the SSCS Resource Center:

1). ISSCC 2015 Tutorial: High Speed Current Steering DACs, Presented by Jan Mulder

2). Webinar: Trends in Broadband Converters, Presented by David H. Robertson

3). ISSCC 2006 Short Course: Pipelined A/D Converters, Presented by Bang-Sup Song

4). Webinar: Enabling and Exploiting Machine Learning in Ultra-low-power Devices, Presented by Naveen Verma

5). Webinar: The X Files, Sheerluck Ohms and the 33dB Solution, Presented by Paul Brokaw

Click here to visit the SSCS Resource Center.

SSCS Members Can Join Sister Societies for Just $5 Use Code SSCXCAS2017 or SSCXEDS2017

If you have not renewed your SSCS membership for 2017, you can enter the promotion code SSCXCAS2017 at checkout to join the Circuits and Systems Society (CAS) for $5 or SSCXEDS2017 to join the Electron Devices Society (EDS) for $5.

If you have already renewed for 2017, **click here** for more details about the discounted CAS membership and **click here** for more details about the discounted EDS membership.

Earn Continuing Education Hours

Have you attended an SSCS webinar? Attendees of upcoming and past webinars have the opportunity to earn professional development hours. Certificates of completion are offered to participants who view a webinar. A certificate of completion confirms one hour of professional development. After you attend the webinar, you may request a certificate of completion by completing the form **HERE**.

EDUCATION

Upcoming Distinguished Lecturer Events in August

	SPEAKER	CHAPTER	TOPIC
August 1	Naveen Verma	SSCS Tainan	Topic: Exploiting Data-driven Interference Towards Low-energy Implementations in Intelligent Sensors For more information, please click here
August 4	Patrick Yue	SSCS/CAS Central Texas	Topic: LED-Based Visible Light Communication Systems - Driver SoC Design and Practical Applications For more information, please click here
August 4	Naveen Verma	SSCS Taipei	Topic: TBD For more information, please click here
August 7	Naveen Verma	SSCS Singapore	Topic: Exploiting Data-driven Inference Towards Low-energy Implementations in Intelligent Sensors For more information, please click here
August 7	Jerald Yoo	SSCS Singapore	Topic: Body Area (Sensor) Network Topic: Design strategies for wearable sensor interfaces For more information, please click here
August 8	Naveen Verma	SSCS Indonesia	Topic: Making Sense of Medical Sensor Signals: Algorithms and Platforms for Intelligent Medical Devices For more information, please click here Topic: Sensing on a Very Large Scale: Large-Area-Electronics Systems for Extensive Interfacing with the Physical World For more information, please click here

August 10	**Naveen Verma**	**SSCS Indonesia**	**Topic: Sensing on a Very Large Scale: Large-Area-Electronics Systems for Extensive Interfacing with the Physical World** **For more information, please click here**
August 10	**Woogeun Rhee**	**SSCS New South Wales**	**Topic: Phase-Locked Frequency Synthesis and Modulation for Modern Wireless Transceivers** **For more information, please click here**
August 14	**Sorin Voinigescu**	**SSCS DL at Aarhus University**	**Topic: Si-based Transistor and Analog-Mixed Signal Circuit Scaling and the Natural Progression of Moore's Law to Silicon Quantum Computing at the Atomic Scale** **For more information, please click here**

For more information on upcoming Distinguished Lecturer Tours, CLICK HERE.

AWARDS

2018 IEEE Donald O. Pederson Award in Solid-State Circuits

The recipients of the 2018 IEEE Donald O. Pederson Award are William S. Carter, Fellow, Xilinx, San Jose, California and Stephen M. Trimberger, Fellow, Xilinx, San Jose, California for "Contriutions to field-programmable gate array technology". The award will be presented at the Plenary Session at the 2018 International Solid-State Circuits Conference (ISSCC) in San Francisco, California.

CONFERENCES

Upcoming Conferences

2017 European Solid-State Circuits Conference (ESSCIRC) Belgium	**Sept 11 - 14, 2017**
2017 IEEE Biomedical Circuits and Systems Conference (BioCAS) Italy	**October 19 - 21, 2017**
2017 IEEE Bipolar/BiCMOS Circuits and Technology Meeting - BCTM Florida	**October 19 - 21, 2017**
2017 IEEE Asian Solid-State Circuits Conference (A-SSCC) Korea (South)	**November 6 - 8, 2017**
2018 International Solid-State Circuits	**February 11 - 15, 2018**

Conference (ISSCC) San Francisco, CA	

CALL FOR PAPERS

2018 IEEE International Solid-State Circuits Conference (ISSCC) - Call for Papers

Continued advances in solid-state circuits and systems have brought evermore powerful communication and computation capabilities into mobile form factors. These ubiquitous smart devices lie at the heart of a revolution shaping how we connect, collaborate, build relationships, and share information. Such social technology allows people to maintain connections and support networks that otherwise would not be possible; it provides the ability to access information instantaneously and from any location, helping to shape the world's events and culture. Thereby, citizens of all nations are more empowered than ever before, and social networks allow worldwide communities to develop and bond through common interests. ISSCC 2018 is seeking innovations that will bring further progress in developing a truly-connected social world.

Innovative and original papers are solicited in subject areas including (but not limited to) the following:

ANALOG: Amplifiers, comparators, oscillators, filters, references; nonlinear analog circuits; digitally-assisted analog circuits; sensor interface circuits.

DATA CONVERTERS: Nyquist-rate and oversampling A/D and D/A converters.

DIGITAL ARCHITECTURES & SYSTEMS: Microprocessors, micro-controllers, applications processors, graphics processors; systems for communications, video and multimedia, machine-learning, deep-learning, neuromorphism, cryptographics, special function acceleration, processing-in-memory, FPGA/reconfigurable systems, system-level power management, near-threshold/subthreshold systems, digital architectures and systems for emerging applications (e.g. virtual reality, autonomous vehicles).

DIGITAL CIRCUITS: Building blocks for 2D/3D SoC, including: special-purpose digital circuits, intra-chip communication circuits, clock-distribution techniques, soft-error and variation-tolerant circuits; Circuits for power management in digital applications, including, digital/synthesizable voltage regulators and PLLs, digital sensors, adaptive circuits; Subthreshold and Near-threshold circuits; Circuits for neuro-computing; Hardware-security circuits including PUFs, TRNGs, crypto-circuits, side-channel-attacks mitigation.

IMAGERS, MEMS, MEDICAL, & DISPLAY: Image sensors and companion chips; image-sensor SoCs; MEMS-based integrated systems; ultrasonic sensors, neural interfaces and closed-loop systems; biosensors, microarrays, and lab-on-a-chip; wearable electronics; biomedical SoCs; display and touch electronics, flexible displays, and displays with integrated sensing functionality.

MEMORY: Static, dynamic, and non-volatile memories for stand-alone and embedded applications; memory/SSD controllers; high-bandwidth I/O interfaces; memories based on phase-change, magnetic, spin-transfer-torque, ferroelectric, and resistive materials; array architectures and circuits to improve low-voltage operation, power reduction, bit-error management, reliability, and fault tolerance; memory-subsystem enhancements, including in-memory logic functions.

POWER MANAGEMENT: Power control and management circuits, regulators; switched-mode power supplies, using inductive, capacitive, and hybrid techniques; energy harvesting circuits and systems; circuits for lighting.

RF CIRCUITS and WIRELESS SYSTEMS: Building blocks and complete solutions at RF, mm-Wave and THz frequencies for receivers, transmitters, frequency synthesizers, transceivers, SoCs and SiPs; Innovative circuit-level and system architecture solutions for

established wireless standards and future systems or applications, including wireless sensing, radar and localization.

TECHNOLOGY DIRECTIONS: Emerging IC and system solutions for: biomedical applications, sensor interfaces, analog signal processing, power management, computation, data storage, security, and communication; non-silicon, carbon, organic, metal-oxide-, compound, wide-bandgap-semiconductor. and nano electronics circuits; flexible, large-area, stretchable, and printable electronics; 3D integration; spintronics; quantum, optical, new-device, and non-transistor-based circuits.

WIRELINE: Receivers/transmitters/transceivers for wireline systems, including backplane transceivers, optical links, chip-to-chip communications, 2.5/3D interconnect, copper cable links, and equalizing on-chip links; exploratory I/O circuits for advancing data rates, power efficiency, and equalization; building blocks for wireline transceivers (such as AGCs, analog and ADC/DAC-based front ends, equalizers, clock generation and distribution circuits including PLLs, line drivers, and hybrids).

NEW FIRM DEADLINE FOR REGISTERING INTENT TO SUBMIT: Thursday, September 7, 2017, 3:00 PM ET

FIRM DEADLINE FOR PAPER SUBMISSION: Monday, September 11, 2017, 3:00 PM ET

Authors should submit 2 items for review: 1) An informative and quantitative Abstract; 2) A Draft Manuscript for the Digest of Technical Papers. Also, read the Pre-Publication Guidelines (summarized below) carefully!

The submission Website is now available.

To submit a paper, go to: http://submissions.mirasmart.com/ISSCC2018 to upload the manuscript and provide the requested additional information. Authors must register their intent to submit on the website by September 7, 2017, this will require upload of an abstract and completion of a submission questionnaire. The full manuscript must be submitted by September 11, 2017. During the submission process you will be asked for a suggested subject area, however this subject area may be changed by the ISSCC organization to streamline the review process.

A sample abstract and draft Digest paper can be found at the ISSCC Website (single-column double-spaced format is required for the paper-review process).

PUBLICATIONS

The latest in SSCS Flagship Publications...

IEEE Journal of Solid-State Circuits

Vol. 52, Issue 8, August

Frequency Reconfigurable mm-Wave Power Amplifier With Active Impedance Synthesis in an Asymmetrical Non-Isolated Combiner: Analysis and Design **Chandrakanth R. Chappidi ; Kaushik Sengupta**

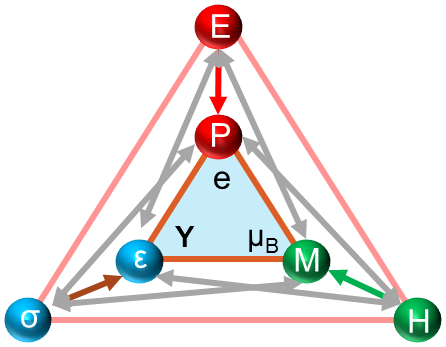
Design and Analysis of an 8 mW, 1 GHz Span, Passive Spectrum Scanner With >+31 dBm Out-of-Band IIP3 Using Periodically Time-Varying Circuit Components Neha Sinha ; Mansour Rachid ; Shanthi Pavan ; Sudhakar Pamarti
Current-Mode Full-Duplex Transceiver for Lossy On-Chip Global Interconnects Nijwm Wary ; Pradip Mandal
Analysis and Design of Integrated Active Cancellation Transceiver for Frequency Division Duplex Systems Lucas Calderin ; Sameet Ramakrishnan ; Antonio Puglielli ; Elad Alon ; Borivoje Nikolić ; Ali M. Niknejad
A 0.038-mm2 SAW-Less Multiband Transceiver Using an N-Path SC Gain Loop Gengzhen Qi ; Pui-In Mak ; Rui P. Martins
On the Design of Wideband Transformer-Based Fourth Order Matching Networks for E -Band Receivers in 28-nm CMOS Marco Vigilante ; Patrick Reynaert
Distributed Injection-Locked Frequency Dividers Alireza Imani ; Hossein Hashemi
A 190-GHz VCO With 20.7% Tuning Range Employing an Active Mode Switching Block in a 130 nm SiGe BiCMOS Rouzbeh Kananizadeh ; Omeed Momeni
On-Chip Two-Tone Synthesizer Based on a Mixing-FIR Architecture Congyin Shi ; Edgar Sánchez-Sinencio
A 2.4-GHz 6.4-mW Fractional-N Inductorless RF Synthesizer Long Kong ; Behzad Razavi
A Spur-and-Phase-Noise-Filtering Technique for Inductor-Less Fractional-N Injection-Locked PLLs Alvin Li ; Yue Chao ; Xuan Chen ; Liang Wu ; Howard C. Luong
A Mostly Digital VCO-Based CT-SDM With Third-Order Noise Shaping Amir Babaie-Fishani ; Pieter Rombouts
A Fully Passive Compressive Sensing SAR ADC for Low-Power Wireless Sensors Wenjuan Guo ; Youngchun Kim ; Ahmed H. Tewfik ; Nan Sun
A 25 GS/s 6b TI Two-Stage Multi-Bit Search ADC With Soft-Decision Selection Algorithm in 65 nm CMOS Shengchang Cai ; Ehsan Zhian Tabasy ; Ayman Shafik ; Shiva Kiran ; Sebastian Hoyos ; Samuel Palermo
A 2-GHz Bandwidth, 0.25-1.7 ns True-Time-Delay Element Using a Variable-Order All-Pass Filter Architecture in 0.13 Î¼m CMOS Imon Mondal ; Nagendra Krishnapura
A ReRAM-Based Nonvolatile Flip-Flop With Self-Write-Termination Scheme for Frequent-OFF Fast-Wake-Up Nonvolatile Processors Albert Lee ; Chieh-Pu Lo ; Chien-Chen Lin ; Wei-Hao Chen ; Kuo-Hsiang Hsu ; Zhibo Wang ; Fang Su ; Zhe Yuan ; Qi Wei ; Ya-Chin King ; Chrong-Jung Lin ; Hochul Lee ; Pedram Khalili Amiri ; Kang-Lung Wang ; Yu Wang ; Huazhong Yang ; Yongpan Liu ; Meng-Fan Chang
A Voltage Multiplier With Adaptive Threshold Voltage Compensation Ye-Sing Luo ; Shen-Iuan Liu
A 140-mV Variation-Tolerant Deep Sub-Threshold SRAM in 65-nm CMOS Khawar Sarfraz ; Jin He ; Mansun Chan

IEEE Journal on Exploratory Solid-State Computational Devices and

Circuits

Mid-Year Highlights

In the first half of 2017, the Journal on Exploratory Solid-State Computational Devices and Circuits had top five of the papers published which already appear in the top 8 of the journal's most accessed papers. These papers include:



[An Energy-Efficient Digital ReRAM-Crossbar-Based CNN With Bitwise Parallelism]
Leibin Ni ; Zichuan Liu ; Hao Yu ; Rajiv V. Joshi

[Nonboolean Pattern Recognition Using Chains of Coupled CMOS Oscillators as Discriminant Circuits]
Vahnood Pourahmad ; Sasikanth Manipatruni ; Dmitri Nikonov ; Ian Young ; Ehsan Afshari

[Compact Modeling of Distributed Effects in 2-D Vertical Tunnel FETs and Their Impact on DC and RF Performances]
Jie Min ; Peter M. Asbeck

[Nonvolatile Spintronic Memory Array Performance Benchmarking Based on Three-Terminal Memory Cell]
Chenyun Pan ; Azad Naeemi

[CoMET: Composite-Input Magnetoelectric- Based Logic Technology]
Meghna G. Mankalale ; Zhaoxin Liang ; Zhengyang Zhao ; Chris H. Kim ; Jian-Ping Wang ; Sachin S. Sapatnekar

JxCDC papers listed in order of popularity can be found online **HERE**.

For paper submission details, click **HERE**.

Seeking News

Please send any chapter news or happenings (Distinguished Lecturer visits, events hosted by your SSCS chapter, awards received by members, etc) to Abira Sengupta, SSCS Magazine News Editor, for inclusion in an upcoming issue of the magazine. Please email - **Abira.Sengupta@ieee.org**. We look forward to receiving your news articles!

For more chapter news, check out the Spring 2017 issue of the Solid-State Circuits Magazine.

FEEDBACK

Let us know what you think! Please **email us** to send us your comments about the newsletter, what you would like to see included each month, or any other comments.

CLICK HERE TO VISIT OUR WEBSITE

CONNECT WITH SSCS: