IEEE SOLID-STATE CIRCUITS SOCIETY

Where ICs are in IEEE

February 2018

NEWS

UPCOMING WEBINAR

Channel Selection at RF - Presented by Professor Behzad Razavi

Wednesday, March 7th @ 12 PM ET

CLICK HERE TO REGISTER!

This webinar is pre-recorded. Prof. Razavi will be available during the webinar to answer any questions about formulas, theories, etc.

Abstract: A holy grail in RF design has been to perform channel selection at RF, i.e., remove strong interferers and even out-of-channel noise at the receiver input rather than in the baseband. Such an approach is attractive for it obviates the need for SAW filters and greatly relaxes the linearity requirements of the receiver chain, ultimately leading to a lower power consumption and a more compact design. This research demonstrates a universal CMOS receiver employing RF channel selection and meeting the exacting demands of GSM and WCDMA. Drawing upon commutated networks, we introduce the concept of the "Miller bandpass filter" and several of its variants so as to create a receiver that achieves a narrow channel bandwidth and can withstand large blockers. Realized in 65-nm technology, the prototype provides a programmable bandwidth from 350 kHz to 20 MHz and draws 20 mW.The noise figure is 2.9 dB in the absence of blockers and 5 dB with a 0-dBm

blocker at 20-MHz offset.

Bio: Behzad Razavi is Professor of Electrical Engineering at UCLA, where he conducts research on analog and RF integrated circuits. An IEEE Fellow, Prof. Razavi has served as an IEEE Distinguished Lecturer and has published more than 180 papers and seven books. He has received eight IEEE best paper awards and four teaching awards, and his books have been published in seven languages. He received the 2012 IEEE Pederson Award in Solid-State Circuits and was recognized as one of the top ten authors in the 50-year history of the IEEE International Solid-State Circuits Conference. He is a member of the National Academy of Engineering and the recipient of the 2017 IEEE CAS John Choma Education Award.

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If you have not yet renewed for 2018, join CASS for just $5 by entering promotion code SSCXCAS2018 at checkout. If you have already renewed for 2018, sign in with your **IEEE account** and the discounted CASS membership will be present in your cart.

IEEE Data Port

IEEE has developed a new data repository called IEEE DataPort™ that offers the following benefits to the global technical community at large:

- Accepts and stores datasets up to 2TB in size and can accept multiple file uploads
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- Retains referenceable datasets that can support research reproducibility
- Supports government or other funder mandates for open access to research data
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Download the SSCS Mobile App

VOLTA is now available for download via the Apple Store and GooglePlay

Integrated Circuits (ICs) are at the core of our hi-tech world. They are inside everything electronics. In the coming robot/IoT/AR/VR era, the application and deployment of ICs will become even more prolific and widespread. IEEE Volta is an app developed by IEEE Solid-State Circuits Society (SSCS) aiming at educating the general public about the importance and the history of ICs over the years.

The application is named after Alessandro Volta, a pioneer of electricity and power. The puzzle themes feature the most significant ICs that have changed our way of living. Through learning about these ICs, users gain the historic perspective about this fascinating field and shed some light on what the future ICs may bring for us.

- **Click here** to download via the Apple App Store
- **Click here** to download via GooglePlay

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Top 3 Downloaded Products on the SSCS Resource Center:

1). Demystifying Linear Time Varying Circuits by Shanthi Pavan

2). Enabling and Exploiting Machine Learning in Ultra-low-power Devices by Naveen Verma

3). Bringing Flexibility to Ultra Low Energy IoE Circuits and Systems by Edith Beigne

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EDUCATION

March 2018 Distinguished Lectures

CHAPTER	TALK DETAILS	DATE	LOCATION
Qualcomm San Diego (Sorrento Vallet)	Design Techniques for Scalable, Sub-pJ/b Serial I/O Transceivers - Presented by Sam Palermo	March 8, 2018	Qualcomm San Diego Campus View More Details
SSCS Vancouver Chapter	Energy Efficient Computing in Nanoscale CMOS - Presented by Vivek De	March 9, 2018	TBD View More Details
SSCS Japan Chapter + SSCS Kansai Chapter	Talk Title TBD - Jun Ohta	March 19, 2018	University of Tokyo View More Details
SSCS Tunisia	On-Chip Epilepsy Detection: Where Machine Learning	March 19, 2018	Hammamet, Nabeul View More Details

Meets Patient-Specific Wearable Healthcare - Presented by Jerald Yoo

CONFERENCES

Upcoming Conferences

2018 Design, Automation & Test in Europe Conference and Exhibition (DATE) Dresden, Germany	**March 19 - 23, 2018**
2018 IEEE Custom Integrated Circuits Conference (CICC) San Diego, CA	**April 8 - 11, 2018**
2018 International Symposium on VLSI Technology, Systems and Application (VLSI-TSA) Hsinchu, Taiwan	**April 16 - April 19, 2018**
2018 International Symposium on VLSI Design, Automation and Test (VLSI-DAT) Hsinchu, Taiwan	**April 16-19, 2018**
2018 IEEE Radio Frequency Integrated Circuits Symposium (RFIC) Philadelphia, PA	**June 10 - 12, 2018**
2018 IEEE Symposium on VLSI Technology Honolulu, HI	**June 18 - 22, 2018**
2018 IEEE Symposium on VLSI Circuits Honolulu, HI	**June 18 - 22, 2018**
2018 IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED) Seattle, WA	**July 23 - 25, 2018**
ESSCIRC/ESSDERC 2018 - 44th European Solid-State Circuits Conference/44th European Solid-State Device Research Conference Dresden, Germany	**September 3 - 6, 2018**
2**018 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)** San Diego, CA	**October 14 - 17, 2018**
2018 IEEE Biomedical Circuits and Systems Conference (BioCAS) Cleveland, OH	**October 17 - 19, 2018**
2018 IEEE Asian Solid-State Circuits Conference (A-SSCC) Tainan, Taiwan	**November 5 - 7, 2018**

CALL FOR PAPERS

ISLPED 2018: Call for Papers

International Symposium on Low Power Electronics and Design

July 23 - 25, 2018
Seattle, WA

The International Symposium on Low Power Electronics and Design (ISLPED) is the premier forum for presentation of innovative research in all aspects of low power electronics and design, ranging from process technologies and analog/digital circuits, simulation and synthesis tools, system-level design and optimization, to system software and applications. Specific topics include, but are not limited to, the following three main tracks and sub-areas:

1. Technology, Circuits and Architecture

1.1. Technologies
Low-power technologies for device, interconnect, logic, memory, 2.5/3D, cooling, harvesting, sensors, optical, printable, biomedical, battery, and alternative energy storage devices.

1.2. Circuits
Low-power digital circuits for logic, memory, reliability, clocking, power gating, resiliency, near-threshold and sub-threshold, variability, and digital assist schemes; Low-power analog/mixed-signal circuits for wireless, RF, MEMS, AD/DA Converters, I/O, PLLs/DLLS, imaging, DC-DC converters, and analog assist schemes.

1.3. Logic and Architecture
Low-power logic and microarchitecture for SoC designs, processor cores (compute, graphics and other special purpose cores), cache, memory, arithmetic/Signal processing, cryptography, variability, asynchronous design, and non-conventional computing.

2. CAD, Systems, and Software

2.1. CAD Tools and Methodologies
CAD tools and methodologies for low-power and thermal-aware design addressing power estimation, optimization, reliability and variation impact on power, and power-down approaches at all levels of design abstraction: physical, circuit, gate, register transfer, behavior, and algorithm.

2.2. Systems and Platforms
Low-power, power-aware, and thermal-aware system design including data-center power delivery and cooling, Platforms for SoCs, embedded systems, approximate and brain-inspired computing, the Internet-of-Things (IoT), wearable computing, body-area networks, wireless sensor networks, and system-level power implications due to reliability and variability.

2.3. Software and Applications
Energy-efficient, energy-aware, and thermal-aware software and application design including scheduling and management, power optimizations through HW/SW interactions, and emerging software low-power applications.

3. Industrial Design Track

ISLPED'18 solicits papers for an "Industrial Design" track to reinforce interaction between the academic research community and industry. Industrial Design track papers have the same submission deadline as regular papers and should focus on similar topics, but are expected to provide a complementary perspective to academic research by focusing on challenges, solutions, and lessons learnt while implementing industrial-scale designs. Industrial design papers that focus on any of the topics mentioned in the tracks above are welcome.

Submissions on new topics: emerging technologies, architectures/platforms, and applications are particularly encouraged.

Important Deadlines:
Technical Paper Submission Deadlines: Abstract registration by February 26, 2018 at 11:59 PST, Full paper due by March 5, 2018 at 11:59 PST
Invited Talk, Panel, and Embedded Tutorial Proposals Deadline: April 16, 2018
Notification of Paper Acceptance: May 7, 2018
Submission of Camera-Ready Papers: June 4, 2018

Submissions should be full-length papers up to 6 pages (PDF format, double column, US letter size, using the IEEE conference format).

More information can be found here: **http://www.islped.org/2018/**

BioCAS 2018: Call for Papers
Biomedical Circuits and Systems Conference

October 17 - 19, 2018
Cleveland, OH

BioCAS 2018 is a premier international forum for presenting the interdisciplinary research and development activities at the crossroads of medicine, life sciences, physical sciences and engineering that shape tomorrow's medical devices and healthcare systems.
This conference brings together members of our communities to broaden their knowledge in emerging areas of research at the interface of the life sciences and the circuits and systems engineering. The three-day single-track program for BioCAS 2018 is multidisciplinary in topics including but not limited to:

Biomedical Technologies
* Assistive, Rehabilitation, and Quality of Life Technologies
* Biofeedback, Neuromodulation, and Closed-Loop Systems
* Bio-Inspired and Neuromorphic Circuits and Systems
* Biosensor Devices and Interface Circuits
* Biotelemetry and Energy Harvesting/Scavenging Circuits and Systems
* Body Area/Sensor Network and Wireless/Wearable Health Monitoring
* Electronics for Neuroscience
* Implantable Medical Electronics
* Lab-on-Chip and BioMEMS

Biomedical Applications
* Point-of-Care Technologies for Healthcare
* Biomedical Imaging and Image Processing
* Biosignal Recording, Processing, and Machine Learning
* Genomics and Systems Biology
* Human-Machine Interfaces
* Medical Information Systems and Bioinformatics

Submission Guidelines
The complete 4-page paper (in standard IEEE double-column format), including the title, authors' names, affiliations and e-mail addresses, as well as a short abstract and an optional demonstration video link (3 minute max) are requested. Papers must be submitted electronically in PDF format through **www.biocas2018.org.**

Important Dates
Monday, April 23, 2018: Special Session Proposal Deadline
Monday, June 11, 2018: Regular Paper Submission Deadline
Monday, July 16, 2018: Live Demo Session deadline
Monday, August 13, 2018: Author Notification Date
Friday, August 31, 2018: Author Registration/Final Paper Submission Deadline

ESSCIRC/ESSDERC 2018: Call for Papers
European Solid-State Device Research Conference
European Solid-State Circuits Conference

September 3-6, 2018

Dresden, Germany

The aim of **ESSDERC and ESSCIRC** is to provide an annual European forum for the presentation and discussion of recent advances in solid-state devices and circuits. The level of integration for system-on-chip design is rapidly increasing. This is made available by advances in semiconductor technology. Therefore, more than ever before, a deeper interaction among technologists, device experts, IC designers and system designers is necessary. While keeping separate Technical Program Committees, ESSDERC and ESSCIRC are governed by a common Steering Committee and share Plenary Keynote Presentations and Joint Sessions bridging both communities. Attendees registered for either conference are encouraged to attend any of the scheduled parallel sessions, regardless to which conference they belong.

Although not limited, papers are solicited for the following main topics:

ESSDERC

CMOS Devices and Technology - CMOS scaling, Novel MOS device architectures; Circuit/device interaction and co-optimization; High-mobility channel devices; CMOS front-end or back-end processes; Interconnects; Integration of RF or photonic devices; 3D integration. Frontend and back-end manufacturing processes; 3D integration and wafer-level packaging; Reliability and characterization of materials, processes and devices; Advanced interconnects; ESD, latch-up, soft errors, noise and mismatch behavior, hot carrier effects, bias temperature instabilities, and EMI; Defect monitoring and control; Metrology; Test structures and methodologies; Manufacturing yield modeling, analysis and testing.

Opto-, Power and Microwave Devices - New device or process architectures; New phenomena and performance improvement of optoelectronic, high voltage, smart power, IGBT, microwave devices; Passive devices, antennas and filters (including Si, Ge, SiC, GaN); Optoelectronic devices including sensors, LEDs, semiconductor lasers; Photovoltaic devices; Studies of high temperature operation; IC cooling and packaging aspects. Reliability and characterization of materials, processes and devices.

Physical Modeling of Materials and Devices - Numerical, analytical and statistical modeling and simulation of electronic, optical or hybrid devices, the interconnect, isolation and 2D or 3D integration; Aspects of materials, fabrication processes and devices e.g. advanced physical phenomena (quantum mechanical and non-stationary transport phenomena, ballistic transport, ...); Mechanical or electrothermal modeling and simulation; DfM. Reliability of materials and devices

Compact Modeling of Devices and Circuits - Compact/SPICE modeling of electronic, optical, organic, and hybrid devices and their IC implementation and interconnection. Topics include compact/SPICE models and their Verilog-A standardization of the semiconductor devices (including Bio/Med sensors, MEMS, Microwave, RF, High voltage and Power), parameter extraction, compact models for emerging technologies and novel devices, performance evaluation, reliability, variability, and open source benchmarking/implementation methodologies. Modeling of interactions between process, device, and circuit design as well Foundry/Fabless Interface Strategies

Memory Devices and Technology - Embedded and stand-alone memories; DRAM, FeRAM, MRAM, ReRAM, PCRAM, Flash, Nanocrystal and single/few-electron memories, Organic memories, NEMS-based devices, Selectors; Novel memory cell concepts and architectures, covering device physics, reliability, process integration and manufacturability issues and including 3D NAND Flash, crosspoint arrays, and 3D systems integration; Devices and concepts for neuromorphic computing, memory-enabled logic and security applications.

Sensor Devices and Technology - Design, fabrication, modeling, reliability, packaging and smart systems integration of actuators (discrete SoC, SiP, or heterogenous 3D integration); MEMS, NEMS, optical, chemical or biological sensors; Display technologies; High-speed imagers; TFTs; Organic and flexible substrate electronics.

Emerging non-CMOS Devices and Technologies - Novel non-CMOS materials, processes and devices, (carbonnanotubes, nanowires and nanoparticles, 2D materials, graphene, metal

oxides, ...) for electronic, optoelectronic, sensor & actuator applications; Reliability and characterization of materials, processes and devices; Molecular and quantum devices; Nanophotonics, plasmonics, spintronics, selfassembling methods; Energy harvesters; High frequency digital and analog devices including THz; New high-mobility channels (strained Si, Ge, SiGe).

ESSCIRC

Analog - OP-Amps and instrumentation amplifiers; CT and DT filters; SC circuits, Comparators; Voltage and current references; high voltage circuits; Nonlinear analog circuits; Digitally assisted analog circuits.

Data Converters - Nyquist-rate and oversampling A/D and D/A converters; Sample-hold circuits; Time-to-digital converters; ADC and DAC calibration/error correction circuits

RF and mm-Wave - RF/IF building blocks like LNAs, mixers, power amplifiers, IF amplifiers; Power detectors; Subsystems for RF, mm-wave and THz design

Frequency Generation - Modulators/demodulators; VCOs; PLLs; DLLs; Frequency synthesizers; Frequency dividers; Integrated passive components.

Wireless and Wireline Systems - Receivers/transmitters/transceivers for wireless/wireline systems Gigabit serial links; Clock and data recovery; Equalization; Advanced modulation systems; Base station and handset applications; TV/radio/satellite receivers and transmitters; Radars.

Sensors, Imager and Biomedical - Sensor subsystems and interfaces; Accelerometers; Temperature sensing; Imaging and smart imaging chips; AMOLED; MEMs subsystems; RF MEMs; Implantable electronic ICs; Biomedical imagers; Bio-MEMs integrated systems; Labon-chip; Organic LED and liquid-crystal-display interface circuits; Flat panel and projection display.

Digital, Security and Memory - Techniques for energy efficient and high performance digital circuits; I/O and inter-chip communication; Reconfigurable digital circuits; Security and encryption circuits; Clocking; Arithmetic building blocks; Memories; Microprocessors; DSPs; Memory interfacing; Bus interfacing; Many core and multirate ICs; 3D integration.

Power Management - Energy transducers; Power regulators; DC-DC converters; Energy-scavenging circuits; LDOs Boost-buck-converters; LED and gate drivers; Sequencers and supervisors; Green circuits.

Important Information

Manuscript guidelines as well as instructions on how to submit electronically will be available on the **conference website**. Papers must not exceed four A4 pages with all illustrations and references included.

All submissions must be received by 3 April 2018.

A-SSCC 2018: Call for Papers
IEEE Asian Solid-State Circuits Conference

Conference Theme: Silicon Enabling Mobile Intelligence

The miniaturized silicon technology enabled big success in the realization of software solutions such as machine learning, big data, virtual and augmented realty in the image and

speech recognition, the medical diagnosis and the autonomous driving automobiles. The current software solutions, however, consume huge power by employing cloud computers along with many graphic processing units and a large amount of memory. Nowadays, the integrated circuit design community tries to develop efficient low-power mobile intelligence solutions by taking challenges in the design of digital and analog circuits, processor architecture, and system for compact IoT devices.

Prospective authors are invited to submit four-page or two page (NEW) manuscripts, including figures, tables, and references to the official A-SSCC 2018 website. The two-page submission can include two-page supplements with figures and figure captions. All papers will be handled and reviewed electronically.

Papers are solicited in the following categories:

Regular Session

1. **Analog Circuits & Systems:** Amplifiers, comparators, switched capacitor circuits, continuous-time & discrete-time filters, voltage/current references;DC- DC converters, power-control circuits; IF/baseband analog circuits, AGC/VGA; non-linear analog circuits.

2. **Data Converters**: Nyquist-rate and oversampling A/D and D/A converters, time-to-digital converters, and capacitance-to-digital converters; sub-circuits for data converters including sample-and-hold circuits, calibration circuits, etc.

3. **Digital Circuits & Systems**: Design, fabrication, and test of digital VLSI systems; high-speed low-power digital circuits, power-reduction and management methods for digital VLSI, ultra-low-voltage and sub-threshold logic design; leakage reduction techniques; clock distribution, I/O circuits, reconfigurable logic-array circuits; supply/substrate noise measurement and cancellation for digital VLSI, variation and fault-tolerant circuits.

4. **SoC & Signal Processing Systems:** System-on-chip(including 3D integration), microprocessors, network processors, baseband communication processing system & architectures, system-level power management; multimedia and recognition processing systems; cryptographic, security, machine-learning, deep-learning, and neuromorphic circuits and systems; bio-medical/neural-network processors and sensor network systems.

5. **RF:** Receivers/transmitters/transceivers for wireless systems; narrowband RF, ultra-wideband and millimeter-wave circuits; circuits and building-blocks including RF front-end, LNA, mixer, power amplifiers, VCOs, frequency synthesizers, RF filters, RF switches, power detectors, active antennas.

6. **Wireline:** Receivers/transmitters/transceivers for wireline systems; optical/electrical data links and backplane transceivers; power-line communication; clock generation circuits, PLL, DLL, spread-spectrum clock generation; building blocks for high-speed wireline communication; analog-digital mixed-mode circuits.

7. **Emerging Technologies and Applications:** Advanced system designs and circuit solutions for technologies and applications including state-of-the-art devices and packaging technologies; flexible and printable electronics; smart sensors and transducers; MEMS for analog, RF, and sensor applications; image sensors and displays; energy harvesting systems; transceiver systems; medical/bio-electronics/bio-inspired chip design and silicon systems.

8. **Memory**: Volatile and Non-volatile memory; new memory designs for 3D/2D architectures, emerging devices such as resistive-/phase change-/magnetic-/ferro-electric- memory devices; data storage and multi-bit-cell memory design; cache-memory system, multi-port memory, memory subsystem, processing in memory, and CAM design; yield-enhancing and ECC techniques; memory testing and built-in self-test.

Special Session

1. Industry Program: This special category accepts only papers based on state-of-the-art industrial products. Strong emphasis on systems realized by silicon chips is encouraged. The

papers should cover architecture, circuits, process technology, packaging and testing, including characterization results, die and system photos, as well as product demos.

2. Student Design Contest: A student design contest is held among the accepted papers with system prototypes or measurement results of which operations can be demonstrated on-site. Refer to the web for further information.

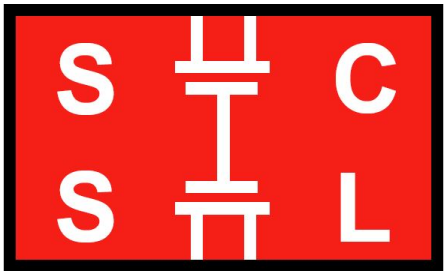
3. FPGA Session (NEW) : This session accepts papers describing FPGA implementation with novel algorithm and/or architecture. The demo results(eg. video or slide) must be included in the paper submission. The authors of accepted papers are required to participate in demo sessions.

Papers related to integrated circuits for intelligent systems are highly solicited. Papers on low-power and/or low-voltage approaches, signal integrity, noise, test, and manufacturability for all the above categories are welcomed. Measurement results are highly recommended, especially for analog, and RF categories. Design methodologies for SiP, and SoC are included in the scope of the conference; the papers only describing CAD tools and CAD algorithms are not considered. Authors must follow detailed instructions provided within the "Authors" section of the website, including the Authors' Guide and Pre-publication Policy. The technical content beyond the abstract of the accepted paper must not be announced, published, or in any way put in the public domain prior to the Conference. Extended versions of selected papers from the Conference will be published in a Special Issue of the IEEE Journal of Solid-State Circuits.

Important Dates

Paper Submission: June 3, 2018 (20:00 GMT)
Acceptance Notification: August 6, 2018
Final Paper Submission: September 9, 2018

PUBLICATIONS



IEEE Solid-State Circuits Letters - Officially Launches

We're happy to announce that our new publication, IEEE Solid-State Circuits Letters, has launched. We are now accepting paper submissions.

For more information, visit:
http://sscs.ieee.org/publications/ieee-solid-state-circuits-letters-ssc-l

For paper submission, visit:
https://mc.manuscriptcentral.com/ssc-l

The latest in SSCS Flagship Publications...

IEEE Journal of Solid-State Circuits

Vol. 53, Issue 3, March 2018

OPEN ACCESS - **A Digital Filtering ADC With Programmable Blocker Cancellation for Wireless Receivers**
Qiwei Wang ; Hajime Shibata ; Antonio Liscidini ; Anthony Chan Carusone

A Quick Startup Technique for High- Q Oscillators Using Precisely Timed Energy Injection
Hani Esmaeelzadeh ; Sudhakar Pamarti

A Low-Jitter Ring-Oscillator Phase-Locked Loop Using Feedforward Noise Cancellation With a Sub-Sampling Phase Detector
Shravan S. Nagam ; Peter R. Kinget

A 2.4-GHz 16-Phase Sub-Sampling Fractional-N PLL With Robust Soft Loop Switching
Dongyi Liao ; Fa Foster Dai ; Bram Nauta ; Eric A. M. Klumperink

An Area-Efficient Microprocessor-Based SoC With an Instruction-Cache Transformable to an Ambient Temperature Sensor and a Physically Unclonable Function
Jiangyi Li ; Teng Yang ; Minhao Yang ; Peter R. Kinget ; Mingoo Seok

A Reconfigurable Vernier Time-to-Digital Converter With 2-D Spiral Comparator Array and Second-Order Î"Î£ Linearization
Hechen Wang ; Fa Foster Dai ; Hua Wang

On-Chip Jitter Measurement Using Jitter Injection in a 28 Gb/s PI-Based CDR
Joshua Liang ; Ali Sheikholeslami ; Hirotaka Tamura ; Hisakatsu Yamaguchi

A Broadband Class-AB Power Amplifier With Instantaneous Supply-Switching Efficiency Enhancement for Cable TV Application
Jeffrey Lee ; Ray Gomez ; Sudhakar Pamarti

Channel-Adaptive ADC and TDC for 28 Gb/s PAM-4 Digital Receiver
Aurangozeb ; AKM Delwar Hossain ; Maruf Mohammad ; Masum Hossain

A 6-bit 0.81-mW 700-MS/s SAR ADC With Sparkle-Code Correction, Resolution Enhancement, and Background Window Width Calibration
Yeonam Yoon ; Nan Sun

A 50 MHz BW 76.1 dB DR Two-Stage Continuous-Time Delta-Sigma Modulator With VCO Quantizer Nonlinearity Cancellation
Siladitya Dey ; Karthikeyan Reddy ; Kartikeya Mayaram ; Terri S. Fiez

A 10-MHz 2-800-mA 0.5-1.5-V 90% Peak Efficiency Time-Based Buck Converter With Seamless Transition Between PWM/PFM Modes
Seong Joong Kim ; Woo-Seok Choi ; Robert Pilawa-Podgurski ; Pavan Kumar Hanumolu

An Injection Frequency-Locked Loop-Autonomous Injection Frequency Tracking Loop With Phase Noise Self-Calibration for Power-Efficient mm-Wave Signal Sources
Dongseok Shin ; Kwang-Jin Koh

A 9-bit 215 MS/s Folding-Flash Time-to-Digital Converter Based on Redundant Remainder Number System in 45-nm CMOS
Bo Wu ; Shuang Zhu ; Yuan Zhou ; Yun Chiu

A Two-Way Interleaved 7-b 2.4-GS/s 1-Then-2 b/Cycle SAR ADC With Background Offset Calibration
Chi-Hang Chan ; Yan Zhu ; Wai-Hong Zhang ; Seng-Pan U ; Rui Paulo Martins

An Eight-Lane 7-Gb/s/pin Source Synchronous Single-Ended RX With Equalization and Far-End Crosstalk Cancellation for Backplane Channels
Cosimo Aprile ; Alessandro Cevrero ; Pier Andrea Francese ; Christian Menolfi ; Matthias Braendli ; Marcel Kossel ; Thomas Morf ; Lukas Kull ; Ilter Oezkaya ; Yusuf Leblebici ; Volkan Cevher ; Thomas Toifl

A 10-Gb/s/ch, 0.6-pJ/bit/mm Power Scalable Rapid-ON/OFF Transceiver for On-Chip Energy Proportional Interconnects
Da Wei ; Tejasvi Anand ; Guanghua Shu ; José E. Schutt-Ainé ; Pavan Kumar Hanumolu

A 0.45-0.7 V 1-6 Gb/s 0.29-0.58 pJ/b Source-Synchronous Transceiver Using Near-Threshold Operation
Woo-Seok Choi ; Guanghua Shu ; Mrunmay Talegaonkar ; Yubo Liu ; Da Wei ; Luca Benini ; Pavan Kumar Hanumolu

A 1-V 0.25- Î¼W Inverter Stacking Amplifier With 1.07 Noise Efficiency Factor
Linxiao Shen ; Nanshu Lu ; Nan Sun

A 0.8-V Resistor-Based Temperature Sensor in 65-nm CMOS With Supply Sensitivity of 0.28 Â°C/V
Hyunmin Park ; Jintae Kim

An Auto-Zero-Voltage-Switching Quasi-Resonant LED Driver With GaN FETs and Fully Integrated LED Shunt Protectors
Lisong Li ; Yuan Gao ; Huaxing Jiang ; Philip K. T. Mok ; Kei May Lau

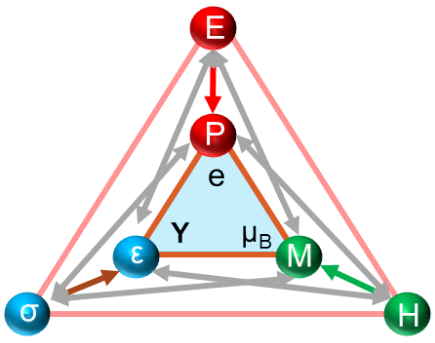
Quasi-Resonant Clocking: Continuous Voltage-Frequency Scalable Resonant Clocking System for Dynamic Voltage-Frequency Scaling Systems
Fahim ur Rahman ; Visvesh Sathe

A 9-mm2 Ultra-Low-Power Highly Integrated 28-nm CMOS SoC for Internet of Things
Yu Pu ; Chunlei Shi ; Giby Samson ; Dongkyu Park ; Ken Easton ; Rudy Beraha ; Adam Newham ; Mark Lin ; Venkat Rangan ; Karam Chatha ; Danny Butterfield ; Rashid Attar

80-kb Logic Embedded High-K Charge Trap Transistor-Based Multi-Time-Programmable Memory With No Added Process Complexity
Balaji Jayaraman ; Derek Leu ; Janakiraman Viraraghavan ; Alberto Cestero ; Ming Yin ; John Golz ; Rajesh Reddy Tummuru ; Ramesh Raghavan ; Dan Moy ; Thejas Kempanna ; Faraz Khan ; Toshiaki Kirihata ; Subramanian S. Iyer

IEEE Journal on Exploratory Solid-State Computational Devices and Circuits

2018 Highlights



An Expanded Benchmarking of Beyond-CMOS Devices Based on Boolean and Neuromorphic Representative Circuits
Chenyun Pan; Azad Naeemi

JxCDC papers listed in order of popularity can be found online **HERE**.

For paper submission details, click **HERE**.

Seeking News

Please send any chapter news or happenings (Distinguished Lecturer visits, events hosted by your SSCS chapter, awards received by members, etc) to Abira Sengupta, SSCS Magazine News Editor, for inclusion in an upcoming issue of the magazine. Please email - **Abira.Sengupta@ieee.org**. We look forward to receiving your news articles!

For more chapter news, check out the Winter 2018 issue of the Solid-State Circuits Magazine.

FEEDBACK

Place article copy here. Be sure to make the articles short and concise as people tend not to read much more than a couple of paragraphs. Place article copy here.

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