IEEE SOLID-STATE CIRCUITS SOCIETY

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October 2019

UPCOMING SSCS WEBINAR

Basics of Jitter in Wireline Communications

Presenter: Prof. Ali Sheikholeslami, University of Toronto, Canada
Friday, November 22nd, 2019
12:00 PM ET

Abstract: Jitter refers to deviation from ideal timing in clock and data transitions. In wireline communications, jitter reduces the timing margin available for clock and data recovery (CDR) circuits and poses significant challenges to signal integrity as the data rates march towards 100Gb/s/lane and beyond. In this talk, we first review the basic definitions of jitter and its properties, the relationship between jitter and phase noise, and the effects of jitter on CDR and other building blocks of a wireline system. We then describe the concept of jitter transfer, jitter generation, and jitter tolerance curves, and the methods of characterizing, modeling, and simulating jitter. Finally, we present some recent works on jitter measurement and jitter mitigation techniques that are used to optimize the link performance.

Bio: Ali Sheikholeslami has been a professor at the University of Toronto, Canada, since 1999. His research interests are jitter, analog and digital integrated circuits, high-speed signaling, and memory design. He has published over 70 journal and conference articles including several on jitter. He has served as the ISSCC Education Chair since 2013, and as a member of its wireline committee from 2007 to 2013. Since 2016, he has been the Education Chair and the Distinguished Lecturer Program Chair for the Solid-State Circuits Society. Prof. Sheikholeslami has received numerous teaching awards from the Faculty of Applied Science and Engineering at the University of Toronto. He is a co-author of a book entitled Understanding Jitter and Phase Noise, published by Cambridge University Press.

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NEWS

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IEEE SSCS is now accepting paper submissions for its new gold fully open access **IEEE Open Access Journal of Solid-State Circuits**, spanning the full scope of the SSCS' fields of interest. The new journal will have an independent editorial board, established peer-review process, is targeting a ten-week rapid publishing schedule and will be fully compliant with funder mandates, including Plan S. SSCS members receive a discount on Article Processing Charges. For more information or to submit a paper, **click here.**

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All IEEE members are encouraged to submit a nomination for a worthy candidate within their technical fields. Nomination guidelines, award-specific criteria, and components of a nomination form can be downloaded from **https://www.ieee.org/about/awards/information.html** and **http://www.ieee.org/about/awards/recognitions/recognitions_herz.html.** All nominations must be submitted through the online nomination portal.

Since 1917, the IEEE Awards Program has paid tribute to technical professionals whose exceptional achievements and contributions have made a lasting impact on technology, society, the engineering profession, and humanity.By this means, the image and prestige of the organization, its members, and the profession are all enhanced.

For more information visit **www.ieee.org/awards** or e-mail **awards@ieee.org**.

PUBLICATIONS

The latest in SSCS Flagship Publications...

IEEE Journal of Solid-State Circuits

Vol. 54, Issue 11, November 2019

Special Section on the 2019 IEEE International Solid-State Circuits Conference (ISSCC)

Introduction to the Special Section on the 2019 IEEE International Solid-State Circuits Conference (ISSCC) **Pedram Mohseni ; Sriram R. Vangal**
Energy-Efficient Motion-Triggered IoT CMOS Image Sensor With Capacitor Array-Assisted Charge-Injection SAR ADC **Kyojin David Choo ; Li Xu ; Yejoong Kim ; Ji-Hwan Seol ; Xiao Wu ; Dennis Sylvester ; David Blaauw**
A Data-Compressive 1.5/2.75-bit Log-Gradient QVGA Image Sensor With Multi-Scale Readout for Always-On Object Detection **Christopher Young ; Alex Omid-Zohoor ; Pedram Lajevardi ; Boris Murmann**

A Reconfigurable 3-D-Stacked SPAD Imager With In-Pixel Histogramming for Flash LIDAR or High-Speed Time-of-Flight Imaging
Sam W. Hutchings ; Nick Johnston ; Istvan Gyongy ; Tarek Al Abbas ; Neale A. W. Dutton ; Max Tyler ; Susan Chan ; Jonathan Leach ; Robert K. Henderson

A 512-Pixel, 51-kHz-Frame-Rate, Dual-Shank, Lens-Less, Filter-Less Single-Photon Avalanche Diode CMOS Neural Imaging Probe
Jaebin Choi ; Adriaan J. Taal ; Eric H. Pollmann ; Changhyuk Lee ; Kukjoo Kim ; Laurent C. Moreaux ; Michael L. Roukes ; Kenneth L. Shepard

A Bio-Impedance Readout IC With Digital-Assisted Baseline Cancellation for Two-Electrode Measurement
Hyunsoo Ha ; Wim Sijbers ; Roland Van Wegberg ; Jiawei Xu ; Mario Konijnenburg ; Peter Vis ; Arjan Breeschoten ; Shuang Song ; Chris Van Hoof ; Nick Van Helleputte

A CMOS Electrochemical Biochip With 32 Ã- 32 Three-Electrode Voltammetry Pixels
Arun Manickam ; Kae-Dyi You ; Nicholas Wood ; Lei Pei ; Yang Liu ; Rituraj Singh ; Nader Gamini ; Mark W. McDermott ; Davood Shahrjerdi ; Robert G. Kuimelis ; Arjang Hassibi

A 47.14- uW 200-MHz MOS/MTJ-Hybrid Nonvolatile Microcontroller Unit Embedding STT-MRAM and FPGA for IoT Applications
Masanori Natsui ; Daisuke Suzuki ; Akira Tamakoshi ; Toshinari Watanabe ; Hiroaki Honjo ; Hiroki Koike ; Takashi Nasuno ; Yitao Ma ; Takaho Tanigawa ; Yasuo Noguchi ; Mitsuo Yasuhira ; Hideo Sato ; Shoji Ikeda ; Hideo Ohno ; Tetsuo Endoh ; Takahiro Hanyu

A Sub-mm3 Ultrasonic Free-Floating Implant for Multi-Mote Neural Recording
Mohammad Meraj Ghanbari ; David K. Piech ; Konlin Shen ; Sina Faraji Alamouti ; Cem Yalcin ; Benjamin C. Johnson ; Jose M. Carmena ; Michel M. Maharbiz ; Rikky Muller

Design and Characterization of a 28-nm Bulk-CMOS Cryogenic Quantum Controller Dissipating Less Than 2 mW at 3 K
Joseph C. Bardin ; Evan Jeffrey ; Erik Lucero ; Trent Huang ; Sayan Das ; Daniel Thomas Sank ; Ofer Naaman ; Anthony Edward Megrant ; Rami Barends ; Ted White ; Marissa Giustina ; Kevin J. Satzinger ; Kunal Arya ; Pedram Roushan ; Benjamin Chiaro ; Julian Kelly ; Zijun Chen ; Brian Burkett ; Yu Chen ; Andrew Dunsworth ; Austin Fowler ; Brooks Foxen ; Craig Gidney ; Rob Graff ; Paul Klimov ; Josh Mutus ; Matthew J. McEwen ; Matthew Neeley ; Charles J. Neill ; Chris Quintana ; Amit Vainsencher ; Hartmut Neven ; John Martinis

A 31- u W, 148-fs Step, 9-bit Capacitor-DAC-Based Constant-Slope Digital-to-Time Converter in 28-nm CMOS
Peng Chen ; Feifei Zhang ; Zhirui Zong ; Suoping Hu ; Teerachot Siriburanon ; Robert Bogdan Staszewski

A 22-bit Read-Out IC With 7-ppm INL and Sub-100-u Hz 1/ f Corner for DC Measurement Systems
Jaehoon Jun ; Soungchul Park ; Junho Kang ; Suhwan Kim

A Sub-nW/kHz Relaxation Oscillator With Ratioed Reference and Sub-Clock Power Gated Comparator
Anand Savanth ; Alex S. Weddell ; James Myers ; David Flynn ; Bashir M. Al-Hashimi

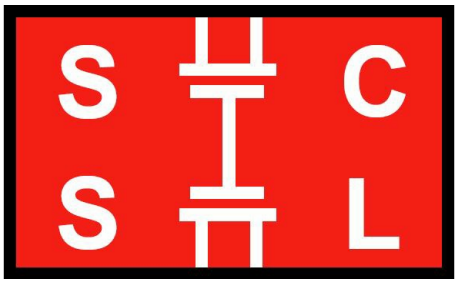
ULPAC: A Miniaturized Ultralow-Power Atomic Clock
Haosheng Zhang ; Hans Herdian ; Aravind Tharayil Narayanan ; Atsushi Shirane ; Mitsuru Suzuki ; Kazuhiro Harasaka ; Kazuhiko Adachi ; Shigeyoshi Goka ; Shinya Yanagimachi ; Kenichi Okada

A 1.6-to-3.0-GHz Fractional- N MDLL With a Digital-to-Time Converter Range-Reduction Technique Achieving 397-fs Jitter at 2.5-mW Power
Alessio Santiccioli ; Mario Mercandelli ; Andrea L. Lacaita ; Carlo Samori ; Salvatore Levantino

Analysis and Design of High-Order QAM Direct-Modulation Transmitter for High-Speed Point-to-Point mm-Wave Wireless Links
Huan Wang ; Hossein Mohammadnezhad ; Payam Heydari

A Process and Temperature Insensitive CMOS Linear TIA for 100 Gb/s/ Î» PAM-4 Optical Links
Kadaba R. Lakshmikumar ; Alexander Kurylak ; Manohar Nagaraju ; Richard

Booth ; Romesh Kumar Nandwana ; Joe Pampanin ; Vito Boccuzzi
A Modular, Direct Time-of-Flight Depth Sensor in 45/65-nm 3-D-Stacked CMOS Technology Augusto Ronchini Ximenes ; Preethi Padmanabhan ; Myung-Jae Lee ; Yuichiro Yamashita ; Dun-Nian
An All-Digital Fused PLL-Buck Architecture for 82% Average Vdd-Margin Reduction in a 0.6-to-1.0-V Cortex-M0 Processor Xun Sun ; Fahim ur Rahman ; Venkata Rajesh Pamula ; Sung Kim ; Xi Li ; Naveen John ; Visvesh S. Sathe
A Time-Domain Computing Accelerated Image Recognition Processor With Efficient Time Encoding and Non-Linear Logic Operation Zhengyu Chen ; Jie Gu



IEEE Solid-State Circuits Letters

Issue 9, September 2019

Special Issue on the 2019 IEEE European Solid-State Circuits Conference (ESSCIRC)

Introduction to the Special Issue on the 2019 IEEE European Solid-State Circuits Conference (ESSCIRC) Ping Lu ; Jens Anders ; Georges Gielen ; Eric Klumperink ; Filip Tavernier ; Robert Henderson ; Tobias Gemmeke ; Joseph Shor
A No-Trim, Scaling-Friendly Thermal Sensor in 16nm FinFET Using Bulk Diodes as Sensing Elements M. Eberlein ; H. Pretl
A 5800- u m2 Resistor-Based Temperature Sensor With a One-Point Trimmed Inaccuracy of ±1.2 °C (3o) From -50 °C to 105 °C in 65-nm CMOS Yongtae Lee ; Woojun Choi ; Taewoong Kim ; Seungwoo Song ; Kofi A. A. Makinwa ; Youngcheol Chae
A 5-Channel Unipolar Fetal-ECG Readout IC for Patch-Based Fetal Monitoring Roland van Wegberg ; Wim Sijbers ; Shuang Song ; Arjan Breeschoten ; Peter Vis ; Mario Konijnenburg ; Hui Jiang ; Michiel Rooijakkers ; Torfinn Berset ; Julien Penders ; Chris Van Hoof ; Nick Van Helleputte
A 16x8 Digital-SiPM Array With Distributed Trigger Generator for Low SNR Particle Tracking Enrico Manuzzato ; Leonardo Gasparini ; Matteo Perenzoni ; Yu Zou ; Luca Parmesan ; G. Battistoni ; M. De Simoni ; Y. Dong ; M. Fischetti ; E. Gioscio ; I. Mattei ; R. Mirabelli ; V. Patera ; A. Sarti ; A. Schiavi ; A. Sciubba ; S. M. Valle ; G. Traini ; M. Marafini
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An 8-bit 10-GHz 21-mW Time-Interleaved SAR ADC With Grouped DAC Capacitors and Dual-Path Bootstrapped Switch Eric Swindlehurst ; Hunter Jensen ; Alexander Petrie ; Yixin Song ; Yen-Cheng Kuan ; Mau-Chung Frank Chang ; Jieh-Tsorng Wu ; Shiuh-Hua Wood Chiang
A 94.3-dB SFDR, 91.5-dB DR, and 200-kS/s CT Incremental Delta-Sigma Modulator With Differentially Reset FIR Feedback Mohamed A. Mokhtar ; Patrick Vogelmann ; Michael Haas ; Maurits Ortmanns

A Simultaneous Multiband Continuous-Time Delta Sigma ADC With 90-MHz Aggregate Bandwidth in 40-nm CMOS
John Bell ; Michael P. Flynn

A Capacitor Dielectric Relaxation Effect Cancellation Circuit in a 12-Bit, 1-MSps, 5.0-V SAR ADC on a 28-nm Embedded Flash Memory Microcontroller
Tetsuo Matsui ; Keisaku Sento ; Tomohiko Ebata ; Atsuhiko Ishibashi

A 1-GS/s 8-Bit 12.01-fJ/conv.-step Two-Step SAR ADC in 28-nm FDSOI Technology
Qingjun Fan ; Jinghong Chen

A 184.6-dBc/Hz FoM 100-kHz Flicker Phase Noise Corner 30-GHz Rotary Traveling-Wave Oscillator Using Distributed Stubs in 22-nm FD-SOI
Mohamed Atef Shehata ; Mike Keaveney ; Robert Bogdan Staszewski

A 39-GHz Frequency Tripler With >40-dBc Harmonic Rejection for 5G Communication Systems in 28-nm Bulk CMOS
Matteo Bassi ; Giovanni Boi ; Fabio Padovan ; Jonas Fritzin ; Stefano Di Martino ; Daniel Knauder

A 22.5-27.7-GHz Fast-Lock Bang-Bang Digital PLL in 28-nm CMOS for Millimeter-Wave Communication With 220-fs RMS Jitter
Cheng-Hsueh Tsai ; Federico Pepe ; Giovanni Mangraviti ; Zhiwei Zong ; Jan Craninckx ; Piet Wambacq

A 57-74-GHz Tail-Switching Injection-Locked Frequency Tripler in 28-nm CMOS
Lorenzo Iotti ; Greg LaCaille ; Ali M. Niknejad

A 8.93-TOPS/W LSTM Recurrent Neural Network Accelerator Featuring Hierarchical Coarse-Grain Sparsity With All Parameters Stored On-Chip
Deepak Kadetotad ; Visar Berisha ; Chaitali Chakrabarti ; Jae-Sun Seo

A 213.7- u W Gesture Sensing System-On-Chip With Self-Adaptive Motion Detection and Noise-Tolerant Outermost-Edge-Based Feature Extraction in 65 nm
Van Loi Le ; Taegeun Yoo ; Ju Eon Kim ; Kwang-Hyun Baek ; Tony Tae-Hyoung Kim

A 354 Mb/s 0.37 mm2 151 mW 32-User 256-QAM Near-MAP Soft-Input Soft-Output Massive MU-MIMO Data Detector in 28nm CMOS
Charles Jeon ; Oscar Castañeda ; Christoph Studer

C3SRAM: In-Memory-Computing SRAM Macro Based on Capacitive-Coupling Computing
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2-Mb Embedded Phase Change Memory With 16-ns Read Access Time and 5-Mb/s Write Throughput in 90-nm BCD Technology for Automotive Applications
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A 20F2 Area-Efficient Differential NAND-Structured Physically Unclonable Function for Low-Cost IoT Security
Jongmin Lee ; Minsun Kim ; Gicheol Shin ; Yoonmyung Lee

An All-Digital, V MAX-Compliant, and Stable Distributed Charge Injection Scheme for Fast Mitigation of Voltage Droop
Suyoung Bang ; Minki Cho ; Pascal Meinerzhagen ; Andres Malavasi ; Muhammad Khellah ; James Tschanz ; Vivek De

Min-Delay Margin/Error Detection and Correction for Flip-Flops and Pulsed Latches in 10-nm CMOS
Pascal A. Meinerzhagen ; Sandip Kundu ; Andres Malavasi ; Trang Nguyen ; Muhammad M. Khellah ; James W. Tschanz ; Vivek De

A Hybrid THz Imaging System With a 100-Pixel CMOS Imager and a 3.25-3.50 THz Quantum Cascade Laser Frequency Comb
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70-90-GHz Self-Tuned Polyphase Filter for Wideband I/Q LO Generation in a 55-nm BiCMOS Transmitter
Farshad Piri ; Elham Rahimi ; Matteo Bassi ; Francesco Svelto ; Andrea Mazzanti

Broadband Fully Integrated GaN Power Amplifier With Embedded Minimum Inductor Bandpass Filter and AM-PM Compensation
Gholamreza Nikandish ; Robert Bogdan Staszewski ; Anding Zhu

A 4-GS/s 39.9-dB SNDR 11.7-mW Hybrid Voltage-Time Two-Step ADC With Feed-Forward

Ring Oscillator-Based TDCs
Yifan Lyu ; Filip Tavernier

A 13.5-Gb/s 5-mV-Sensitivity 26.8-ps-CLK-OUT Delay Triple-Latch Feedforward Dynamic Comparator in 28-nm CMOS
Athanasios T. Ramkaj ; Michiel S. J. Steyaert ; Filip Tavernier

A 0.06-3.4-MHz 92- uW Analog FIR Channel Selection Filter With Very Sharp Transition Band for IoT Receivers
Bart J. Thijssen ; Eric A. M. Klumperink ; Philip Quinlan ; Bram Nauta

A 0.98-nW/kHz 33-kHz Fully Integrated Subthreshold-Region Operation RC Oscillator With Forward-Body-Biasing
Philex Ming-Yan Fan ; Anand Savanth ; Benoît Labbé ; Pranay Prabhat ; James Myers

A Cellular Multiband DTC-Based Digital Polar Transmitter With âˆ'153 dBc/Hz Noise in 14-nm FinFET
Y. Palaskas ; P. Madoglio ; J. Angel ; J. Tomasik ; S. Hampel ; P. Schubert ; P. Preyler ; T. Mayer ; T. Bauernfeind ; P. Plechinger ; A. Ravi ; O. Degani ; R. Banin ; E. Gordon ; Z. Boos

A 260-MHz RF Bandwidth Mixer-First Receiver With Third-Order Current-Mode Filtering TIA
Giacomo Pini ; Danilo Manstretta ; Rinaldo Castello

A 26-Gb/s 3-D-Integrated Silicon Photonic Receiver in BiCMOS-55 nm and PIC25G With âˆ'15.2-dBm OMA Sensitivity
Farhad Bozorgi ; Melchiorre Bruccoleri ; Matteo Repossi ; Enrico Temporiti ; Andrea Mazzanti ; Francesco Svelto

A 19-GHz Pulsed-Coherent ToF Receiver With 40- Î¼m Precision for Laser Ranging Systems
Li-Yang Chen ; Chih-Kong Ken Yang

A 112-Gb/s PAM-4 Transmitter With a 2-Tap Fractional-Spaced FFE in 65-nm CMOS
Hao Ding ; Xuqiang Zheng ; Danyu Wu ; Lei Zhou ; Jin Wu ; Fangxu Lv ; Jianye Wang ; Xinyu Liu

Adaptive Peak Average Current Control LED Driver for Automotive Lighting
Pavel Horsky ; Jan Plojhar ; Jiri Daniel

A Temperature Compensated 61-W Class-E Soft-Switching GaN-Based Active Diode Rectifier for Wireless Power Transfer Applications
Shang-Hsien Yang ; Ke-Horng Chen ; Ying-Hsi Lin ; Shian-Ru Lin ; Tsung-Yen Tsai

An Energy Harvester Using Image Sensor Pixels With Cold Start and Over 96% MPPT Efficiency
Nishit Shah ; Pedram Lajevardi ; Ken Wojciechowski ; Christoph Lang ; Boris Murmann

A 130-nm CMOS Dual Input-Polarity DC-DC Converter for Low-Power Applications
Alberto Gatti ; Giorgio Spiazzi ; Andrea Gerosa ; Andrea Neviani ; Andrea Bevilacqua

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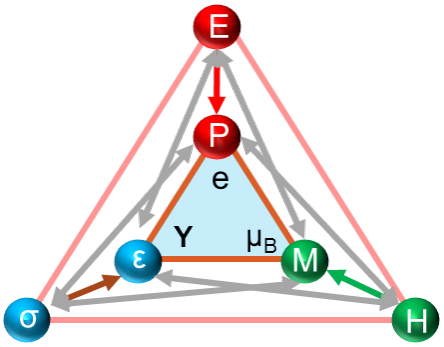
IEEE Journal on Exploratory Solid-State Computational Devices and Circuits



Issue 2, Part 1 - December 2019

Nonvolatile Spintronic Memory Cells for Neural Networks
Andrew W. Stephan ; Qiuwen Lou ; Michael T. Niemier ; Xiaobo Sharon Hu ; Steven J. Koester

JxCDC papers listed in order of popularity can be found online HERE.

For paper submission details, click HERE.

EDUCATION

November 2019 Distinguished Lectures

SSCS Montreal	Basics of Jitter and Phase Noise and Their Effects on Wireline Communications - Presented by Ali Sheikholeslami	November 4, 2019	Concordia University, Canada **For more information, click here**.
SSCS Seattle	Adaptive and Resilient Circuits for Processors - Presented by Keith Bowman	November 5, 2019	University of Washington, Seattle **For more information, click here**
SSCS Oregon	Adaptive and Resilient Circuits for Processors - Presented by Keith Bowman	November 6, 2019	Hillsboro, Oregon **For more information, click here**
SSCS Utah	Digitally-Assisted Data Converters - Presented by Ahmed Ali	November 8, 2019	Brigham Young University, Utah **For more information, click here**
SSCS Thailand	Analog IP: Pipe-line or Pipe-dream - Presented by Matt Straayer	November 15, 2019	Kasetsart University, Thailand **For more information, click here**
SSCS Delhi	Implantable electronics for highly parallel neural interfaces - Presented by Maurits Ortmanns	November 15, 2019	IIT Delhi **For more information, click here**
SSCS Southern Alberta	Circuit Intuitions - Presented by Ali Sheikholeslami	November 19, 2019	University of Calgary, Canada **For more information, click here**
SSCS Houston	Millimeter-Scale Nano-Optical Systems for Future Diagnostics and Sensing: Merging Nanophotonics in Embedded Electronics in the Visible Range - Presented by Kaushik Sengupta	November 25, 2019	Rice University, Texas **For more information, click here**

CALL FOR PAPERS

Call for Papers: CICC 2020

IEEE Custom Integrated Circuits Conference

March 22 - 25, 2019

Boston, MA

http://ieee-cicc.org/

The IEEE Custom Integrated Circuits Conference is a premier conference devoted to IC development. The conference program is a blend of oral presentations, exhibits, panels and forums. The conference sessions present original first published technical work and innovative circuit techniques that tackle practical problems. CICC is the conference to find out how to solve design problems, improve circuit design techniques, get exposure to new technology areas, and network with peers, authors and industry experts.

There are 3 days of Technical Sessions that include lecture presentations addressing state of the art developments in integrated circuit design. The Educational Sessions are a full day of tutorials instructed by recognized invited speakers. The Panels, and Forums are presented throughout the conference to enrich the learning experience of the attendees. The Panel Discussions and Forums are presented by leaders from the IC industry. CICC includes an Exhibits Hall that is open in the evenings where Semiconductor manufacturers, software tool suppliers, silicon IP providers, design-service houses, and technical book publishers offer displays and demonstrations of their products. CICC is sponsored by the IEEE Solid-State Circuits Society and technically co-sponsored by the IEEE Electron Devices Society.

Submission of original and unpublished work is being solicited in the following areas:

- **Analog Circuits and Techniques** for areas such as communications, biomedical, aerospace, automotive, energy, environment, analog computing and security applications, ranging from building blocks to silicon sensors, interfaces, and novel clock generation architectures.
- **Data Converters** including but not limited to A/D, D/A, time-to-digital, frequency-to-digital and analog to information converters of all types enabled by new techniques, architectures, or technologies.
- **Design Foundations** for novel digital, analog, mixed-signal, and memory circuit techniques for present and emerging applications (deep learning, autonomous vehicles, IoT, security, quantum computing). Modeling and simulation of advanced CMOS (FinFET, UTTB-SOI) and beyond-CMOS devices (MEMS, GaN, Non-Volatile Memories, STT) to improve design quality, efficiency, and reliability. Design for manufacturing, test, aging, security, and reliability (novel DFT circuits, system-level testing). High-level system modeling, digital/analog design infrastructure, and verification and emulation for complex SoCs.
- **Digital Circuits, SoCs, and Systems** solicit hardware-based papers in technologies that enhance integrated systems including processors, accelerators, memory systems, with applications in artificial intelligence, security, autonomous transportation, cloud computing, sensing, and communication.
- **Emerging Technologies, Systems, and Applications** solicit hardware focused papers in the technologies of tomorrow extending from new device to system integration and applications with focus on, but not limited to:
    - **Next-generation technology and sensors** including devices, integration, and packaging including nano-primitives, non-silicon based technology, and advanced assembly. Sensor interfaces for MEMS, mm-wave/THz, flexible, printed, large-area and organic electronics, electronic-photonic co-design, and silicon photonics.
    - **Biomedical circuits, systems, and applications** including neural interfaces, microarrays, lab-on-a-chip, bio-inspired circuits, implantable and/or wearable systems, closed-loop systems with sensing and actuation, medical imaging, and other biosensors including biomedical signal processing SoCs.

- **Power Management** circuits and design techniques including DCDC converters, control and management circuits, linear regulators, wireless power transfer, and other methods for improvements in overall system efficiency and performance.

- **Wireless Transceivers and RF/mm-Wave Circuits and Systems** for low-power, energy-efficient and high performance wireless links, biomedical and sensing networks, IoT applications, cellular connectivity including M2M applications (LTE-M, NB-IoT), emerging broadband and MIMO networks (5G, WLAN), vehicle-to-vehicle (V2V), millimeter-wave & THz systems (radar, sensing and imaging), frequency synthesis and LO generation.

- **Wireline and Optical Communications Circuits and Systems** for electrical and optical communications, including serial links for intra-chip and chip-to-chip interconnections, high-speed memory and graphics interfaces, backplanes, long-haul, and power line communications; novel I/O circuits for advancing data rates, improving power efficiency, and supporting extended voltage applications; clocking techniques including PLLs and CDRs; components such as equalizers, high-speed ADC-RX/DAC-TX, silicon photonic and optical interface circuitry.

Important Dates:
Paper Submission Deadline: November 1, 2019
Paper Acceptance Notification: January 31, 2020

Click here for more information

Call for Tutorial Proposals: AICAS 2020

2nd IEEE Conference on Artificial Intelligence Circuits and Systems

March 23rd - 25th, 2020

Genova, Italy

www.aicas2020.eu

The objective of the AICAS 2020 Tutorial Program is to provide participants with an inspiring and informative selection of tutorials that reflect current topics in AI circuits and systems related research and development.

Tutorials will cover a one to three-hour period with ten minutes at the end for questions. They will be held in the morning before the technical sessions.

We encourage submissions of tutorial proposals on the topics including but not limited to:

- Circuits and systems for AI
- Deep learning/machine learning/AI algorithms
- Tools/Platforms for AI
- Architecture for AI computing
- Edge and cloud AI computing platforms
- Hardware accelerators
- Neuromorphic processors and computing
- Hardware/software co-design and design automation for AI systems
- Advanced neural network design
- Emerging applications: Deep learning for Internet-of-Things
- Emerging applications of AI: Medical AI
- Emerging applications of AI: Autonomous Vehicle
- Emerging applications of AI: Smart Factory and Environment
- Emerging applications of AI: Robotics

Prospective organizers of tutorial program should submit proposals to the Tutorial Chair indicating: Title of the tutorial, Area of the tutorial (refer to the above topics), Presenter(s) and their CV, Target audience and prerequisite knowledge of audience, 300 words abstract (for inclusion on webpage and in registration materials), Full description (1-2 pages to be used for evaluation),Keywords, Detailed contact information of all presenters (and indication of the main contact person).

Contact tutorial chair, email: tutorials@aicas2020.eu

Deadline for Proposals: November 10th, 2019

The regular papers (4 pages) and live demo (1 page) submission deadline for AICAS 2020 has been extended by one week to Monday, October 7th midnight CET (GMT+1, central European time). Submission instructions can be found at: https://aicas2020.eu/submissions.

Call for Papers: RFIC 2020

2020 IEEE Radio Frequency Integrated Circuits Symposium
June 21-23, 2020
Los Angeles, CA
https://www.rfic-ieee.org/

NEW for RFIC 2020: The RFIC symposium is expanding its scope to include System Applications and Interactive Demonstrations. This includes systems and applications in 5G, radar, imaging, terahertz, biomedical, and optoelectronic areas. In addition to the Emerging Circuit Technology area introduced in RFIC 2019, this year the symposium has introduced a completely new System Applications area and sub-committee that targets advanced system presentations in a range of topics related to communication, radar, imaging, sensing, and biomedical. To further highlight the systems aspects and enrich our attendees' experience, selected papers from this area will also be presented in a new Interactive Demonstration session.

The symposium starts on Sunday, 21 June 2020 with workshops and short courses, followed by two exciting plenary talks. Immediately following the plenary session, we will be holding an RFIC 'interactive' Sunday reception that will highlight our industry show-case and student papers finalists for an engaging social and technical evening event. Monday, 22 June and Tuesday, 23 June will be comprised of oral paper presentations, an interactive demonstration, and entertaining panel sessions.

We invite authors to submit their technical papers via the RFIC 2020 website; author's guidelines and **Call for Papers can be found here** . Complete information on how and when to submit a paper will be posted on the RFIC 2020 website. The conference will solicit papers describing original work in RFIC circuits, systems engineering, design methodology, RF modeling and CAD simulation, RFIC technologies, device technologies, fabrication, testing, reliability, packaging, and modules to support RF applications in areas such as Wireless Cellular and Connectivity, Low Power Transceivers, Receiver Sub-Systems and Circuits, Mixed-Signal RF and Data Converters, Reconfigurable and Tunable Front-Ends, Transmitter Sub-Systems and Power Amplifiers, Oscillators, Frequency Synthesis, Millimeter- and Sub-Millimeter Wave Systems, and High-Speed Data Transceivers.

Same as last year, a double-blind review process will be adopted to ensure anonymity for both authors and reviewers. Detailed instructions on how to submit a paper compliant with double-blind rules will be posted on the RFIC 2020 website.

Electronic Submission Deadlines:
Technical Paper Summaries in PDF format: 10 January 2020
Final Manuscripts for the Digest and Attendee Download: 23 March 2020

All submissions must be made at rfic-ieee.org in pdf form. Hard Copies are not accepted.

DOWNLOAD the RFIC 2020 Call for Papers

Call for Papers: 2020 Symposia on VLSI Technology and Circuits

June 14-19, 2020

Honolulu, Hawaii

https://vlsisymposium.org

Celebrating its 40th edition in 2020, the VLSI Symposia is the premier international conference on semiconductor technology and circuits. It offers a superb opportunity to interact and synergize on topics spanning the range from new neuromorphic devices, to beyond-the-state-of-the-art process technology to systems-on-chip and AI accelerators.

The circuits symposium is placing special emphasis on several innovation system focus areas, and encourages paper submissions on:

- Machine and deep learning
- FPGA-based accelerators
- Internet of Things
- Industrial electronics
- Big Data management
- Biomedical applications
- Robotics and autonomous transportation

In addition, submissions are welcomed in all of the following circuits areas:

- Processors, SoCs, and Machine Learning
- Digital circuits, signal integrity, and IOs
- Hardware security
- Memory circuits, architectures, and interfaces
- Biomedical circuits
- Sensors, imagers, and display circuits
- Power conversion circuits
- Analog, amplifier and filter circuits
- Wireless receivers and transmitters
- Data converters
- Frequency generation and clock circuits
- Wireline and optical transceivers

The technology symposium calls for papers in the following areas:

- Technologies for "Internet of Things"
- Technologies for Artificial Intelligence and Machine Learning Applications
- Stand-Alone and Embedded Static, Dynamic, non-Volatile and Emerging Memory
- Technologies
- CMOS Technology for Microprocessors and SoCs
- RF / Analog / Digital and Sensors Technologies
- New Process Technologies and Electronic Materials
- Advanced Packaging, System-in-Package (SiP) and 3D Technologies
- Photonics and Imaging Technologies
- Beyond CMOS Devices and Technologies for Heterogeneous Integration

Papers will be selected based on technical innovation, advances relative to previously published work, credibility of claims, and quality of writing and illustrations

Submission Information
Paper Submission Deadline: Monday, February 10, 2020, 23:59 PST

For more information, click here.

CONFERENCES

Upcoming 2019 SSCS-Sponsored Conferences

2019 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS) Nashville, Tennessee	**November 3 - 6, 2019**
2019 IEEE Asian Solid-State Circuits Conference (A-SSCC) Macau, China	**November 4 - 6, 2019**

SSCS-Sponsored Conferences: Proceedings

Click the links below to access the latest SSCS-Sponsored conference proceedings.

2018

2018 IEEE International Solid-State Circuits Conference (ISSCC)
2018 IEEE Custom Integrated Circuits Conference (CICC)
2018 IEEE Symposium on VLSI Circuits (VLSI)
2018 IEEE 44th European Solid-State Circuits Conference (ESSCIRC)
2018 IEEE Asian Solid-State Circuits Conference (A-SSCC)

2019

2019 IEEE International Solid-State Circuits Conference (ISSCC)
2019 IEEE Custom Integrated Circuits Conference (CICC)
2019 Symposium on VLSI Circuits

For Society news and happenings, check out the Summer 2019 issue of the Solid-State Circuits Magazine.

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