IEEE SOLID-STATE CIRCUITS SOCIETY

Where ICs are in IEEE

November 2019

UPCOMING SSCS & EDS JOINT WEBINAR

Emerging Memories and Pathfinding for the Era of Sub-10nm System-on-Chip

Presenter: Dr. Seung Kang, Qualcomm
Wednesday, December 18th, 2019
11:00 AM ET (New York)

Abstract: A semiconductor memory is a ubiquitous component of all electronic systems, coupled with a microprocessor for computing or integrated to store information. As the semiconductor ecosystem expands to such areas like mobile computing, artificial intelligence (AI), Big Data, Internet-of-Things (IOT), life science and healthcare applications, the prevalence of these markets largely depend on memory innovations. This has propelled increasing efforts in researching, developing, and commercializing emerging memory technologies, such as PCM (phase-change memory, or PRAM), MRAM (magnetoresistive RAM), RRAM (resistive RAM), and FRAM (ferroelectric RAM). This presentation overviews these emerging memories from the perspectives of device, design, integration, and application. Also covered is the prospect of embedding these memories into advanced integrated circuits. By far, all emerging memory prototypes and products are built upon relatively mature CMOS technologies such as 22nm and 28nm. For the applications that have traditionally relied on embedded Flash, these nodes are still advanced, and such memories can serve IOT, security, automotive, and some machine learning applications competitively. However, emerging memories have not entered the domain of advanced logic nodes (7nm already in production) and have yet to be proven as a sustainable technology for pervasive applications. This transition necessitates the memory attributes that must go beyond the

specifications of present product offerings. A key challenge is to achieve a combination of high speed and high endurance for high-density arrays compatible with sub-10nm CMOS devices. This requires deeply scaled memory elements with fast switching at low current and high dielectric barrier reliability. Efforts are also desired for custom memories which can be tailored in various densities and form factors for heterogeneously partitioned systems.

Bio: Seung Kang is a recognized semiconductor technologist who has driven holistic system-centric innovations of device, circuit design, and chip architecture. He built and led an advanced memory team at Qualcomm who pioneered embedded STT-MRAM and delivered the industry-first product prototype IP for IOT and wearables. He currently leads a team for developing standard cell architecture, circuit, and co-optimization methodology for Qualcomm's flagship mobile SOCs. Before joining Qualcomm, he had worked on CMOS process technology and reliability at the Bell Laboratories of Lucent Technologies. He received Ph.D. from U.C. Berkeley and both B.S. and M.S. from Seoul National University, Korea. Dr. Kang has published >100 papers and given >70 keynote and invited speeches at international conferences and colloquiums. He served as Distinguished Lecturer for the IEEE Electron Device Society from 2014 to 2018 and as Visiting Professor at the Center for Innovative Integrated Electronic Systems of Tohoku University. He holds >230 granted US patents.

CLICK HERE TO REGISTER

NEWS

SSCS Contests for Students

Calling all students! SSCS is pleased to announce the launch of two contests open to undergraduate and graduate students. Prizes are valued up to $2K.

2019-2020 CIRCUIT ANALYSIS & DESIGN CONTEST
This contest involves solving a thought-provoking circuit analysis and design problem. Submissions are solicited by undergraduate and graduate students who are currently enrolled in a college or university. Win up to $2K towards entering an SSCS-sponsored conference. **Click here for more information** on contest eligibility, how to enter, and more. **Submission Deadline: January 15, 2020 - EXTENDED DEADLINE!**

CIRCUITS VIDEO CONTEST
Create a fun short (5-10 minute) video that explains circuits for high school students. Tell a story about a circuits concept. Videos should motivate a real-world application of circuits. Undergraduate and graduate students who are currently enrolled in a college or university may enter. Win up to $2K towards entering an SSCS-sponsored conference. **Click here for more information** on contest eligibility, how to enter, and more. **Submission Deadline: December 15, 2019**

Call for Papers for NEW IEEE

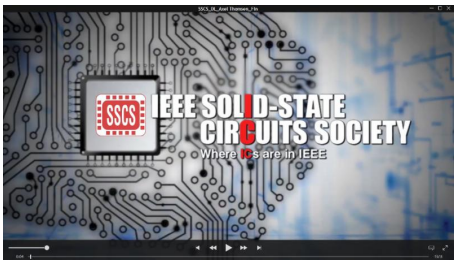
Open Journal of Solid-State Circuits

IEEE SSCS is now accepting paper submissions for its new gold fully open access **IEEE Open Access Journal of Solid-State Circuits**, spanning the full scope of the SSCS' fields of interest. The new journal will have an independent editorial board, established peer-review process, is targeting a ten-week rapid publishing schedule and will be fully compliant with funder mandates, including Plan S. SSCS members receive a discount on Article Processing Charges. For more information or to submit a paper, **click here.**

SSCS YouTube Channel

SSCS now has a YouTube Channel where all CONFedu videos are posted including VLSIx 2016, CICCx 2017, ISSCCedu 2018, and ESSCIRCedu 2018.

Now Available: CICCedu 2019 and VLSIedu 2019.



PUBLICATIONS

The latest in SSCS Flagship Publications...

IEEE Journal of Solid-State Circuits

Vol. 54, Issue 12, December 2019

Special Issue on the 2019 IEEE International Solid-State Circuits Conference (ISSCC)

Introduction to the Special Issue on the 2019 IEEE International Solid-State Circuits Conference (ISSCC) **Youngcheol Chae ; Bernhard Wicht ; Bob Verbruggen ; Payam Heydari ; Howard Luong**
A Sub-nW 32-kHz Crystal Oscillator Architecture Based on a DC-Only Sustaining Amplifier **Hani Esmaeelzadeh ; Sudhakar Pamarti**
A Fast Startup CMOS Crystal Oscillator Using Two-Step Injection **Karim M. Megawer ; Nilanjan Pal ; Ahmed Elkholy ; Mostafa Gamal Ahmed ; Amr Khashaba ; Danielle Griffith ; Pavan Kumar Hanumolu**

[An Energy Measurement Frontend With Integrated Adaptive Background Accuracy Monitoring of the Full System Including the Current and Voltage Sensors]
Seyed Danesh ; William Holland ; George R. Spalding ; Michael Guidry ; J. E. D. Hurwitz

[A 192-pW Voltage Reference Generating Bandgap- Vth With Process and Temperature Dependence Compensation]
Youngwoo Ji ; Jungho Lee ; Byungsub Kim ; Hong-June Park ; Jae-Yoon Sim

[A Flying-Inductor Hybrid DC-DC Converter for 1-Cell and 2-Cell Smart-Cable Battery Chargers]
Casey Hardy ; Yogesh Ramadass ; Kevin Scoones ; Hanh-Phuc Le

[EMI-Regulated GaN-Based Switching Power Converter With Markov Continuous Random Spread-Spectrum Modulation and One-Cycle on-Time Rebalancing]
Yingping Chen ; D. Brian Ma

[A Light-Load Efficient Fully Integrated Voltage Regulator in 14-nm CMOS With 2.5-nH Package-Embedded Air-Core Inductors]
Christopher Schaef ; Nachiket Desai ; Harish K. Krishnamurthy ; Xiaosen Liu ; Khondker Zakir Ahmed ; Suhwan Kim ; Sheldon Weng ; Huong Do ; William J. Lambert ; Kaladhar Radhakrishnan ; Krishnan Ravichandran ; James W. Tschanz ; Vivek De

[A 52% Peak Efficiency > 1-W Isolated Power Transfer System Using Fully Integrated Transformer With Magnetic Core]
Yue Zhuo ; Shaoyu Ma ; Tianting Zhao ; Wenhui Qin ; Yuanyuan Zhao ; Yingjie Guo ; Haiyang Yan ; Baoxing Chen

[Wideband Hybrid Envelope Tracking Modulator With Hysteretic-Controlled Three-Level Switching Converter and Slew-Rate Enhanced Linear Amplifier]
Parisa Mahmoudidaryan ; Debashis Mandal ; Bertan Bakkaloglu ; Sayfe Kiaei

[An Efficient Piezoelectric Energy Harvesting Interface Circuit Using a Sense-and-Set Rectifier]
Yimai Peng ; Kyojin D. Choo ; Sechang Oh ; Inhee Lee ; Taekwang Jang ; Yejoong Kim ; Jongyup Lim ; David Blaauw ; Dennis Sylvester

[A Bipolar-Input Thermoelectric Energy-Harvesting Interface With Boost/Flyback Hybrid Converter and On-Chip Cold Starter]
Peng Cao ; Yao Qian ; Pan Xue ; Danzhu Lu ; Jie He ; Zhiliang Hong

[A Two-Step ADC With a Continuous-Time SAR-Based First Stage]
Linxiao Shen ; Yi Shen ; Zhelu Li ; Wei Shi ; Xiyuan Tang ; Shaolan Li ; Wenda Zhao ; Mantian Zhang ; Zhangming Zhu ; Nan Sun

[A Calibration-Free Time-Interleaved Fourth-Order Noise-Shaping SAR ADC]
Lu Jie ; Boyi Zheng ; Michael P. Flynn

[A 0.6-V 13-bit 20-MS/s Two-Step TDC-Assisted SAR ADC With PVT Tracking and Speed-Enhanced Techniques]
Minglei Zhang ; Chi-Hang Chan ; Yan Zhu ; Rui P. Martins

[A 10-mW 16-b 15-MS/s Two-Step SAR ADC With 95-dB DR Using Dual-Deadzone Ring Amplifier]
Ahmed ElShater ; Praveen Kumar Venkatachala ; Calvin Yoji Lee ; Jason Muhlestein ; Spencer Leuenberger ; Kazuki Sobue ; Koichi Hamashita ; Un-Ku Moon

[A Super-Resolution Mixed-Signal Doherty Power Amplifier for Simultaneous Linearity and Efficiency Enhancement]
Fei Wang ; Tso-Wei Li ; Song Hu ; Hua Wang

[A DC-to-108-GHz CMOS SOI Distributed Power Amplifier and Modulator Driver Leveraging Multi-Drive Complementary Stacked Cells]
Omar El-Aassar ; Gabriel M. Rebeiz

[A Watt-Level Phase-Interleaved Multi-Subharmonic Switching Digital Power Amplifier]
Aoyang Zhang ; Mike Shuo-Wei Chen

[An Ultra-Low-Jitter, mmW-Band Frequency Synthesizer Based on Digital Subsampling PLL Using Optimally Spaced Voltage Comparators]
Juyeop Kim ; Younghyun Lim ; Heein Yoon ; Yongsun Lee ; Hangi Park ; Yoonseo Cho ; Taeho Seong ; Jaehyouk Choi

[A 265- μ W Fractional- *N* Digital PLL With Seamless Automatic Switching Sub-]

Sampling/Sampling Feedback Path and Duty-Cycled Frequency-Locked Loop in 65-nm CMOS **Hanli Liu ; Zheng Sun ; Hongye Huang ; Wei Deng ; Teerachot Siriburanon ; Jian Pang ; Yun Wang ; Rui Wu ; Teruki Someya ; Atsushi Shirane ; Kenichi Okada**
A 30-GHz Digital Sub-Sampling Fractional- N PLL With a -238.6-dB Jitter-Power Figure of Merit in 65-nm LP CMOS **Luca Bertulessi ; Saleh Karman ; Dmytro Cherniak ; Alessandro Garghetti ; Carlo Samori ; Andrea L. Lacaita ; Salvatore Levantino**
A Self-Calibrated 16-GHz Subsampling-PLL-Based Fast-Chirp FMCW Modulator With 1.5-GHz Bandwidth **Qixian Shi ; Keigo Bunsen ; Nereo Markulic ; Jan Craninckx**
Sub-nW Wake-Up Receivers With Gate-Biased Self-Mixers and Time-Encoded Signal Processing **Vivek Mangal ; Peter R. Kinget**
Analysis and Design of a Full-Duplex Two-Element MIMO Circulator-Receiver With High TX Power Handling Exploiting MIMO RF and Shared-Delay Baseband Self-Interference Cancellation **Mahmood Baraani Dastjerdi ; Sanket Jain ; Negar Reiskarimian ; Arun Natarajan ; Harish Krishnaswamy**
A Sub-6-GHz 5G New Radio RF Transceiver Supporting EN-DC With 3.15-Gb/s DL and 1.27-Gb/s UL in 14-nm FinFET CMOS **Jongwoo Lee ; Sangwook Han ; Joonhee Lee ; Byoungjoong Kang ; Jeongyeol Bae ; Jaehyuk Jang ; Seunghyun Oh ; Ji-Soo Chang ; Sanghoon Kang ; Ki Yong Son ; Hyungsun Lim ; Daechul Jeong ; Ilyong Jong ; Sanghyun Baek ; Jae Hoon Lee ; Ronghua Ni ; Yongrong Zuo ; Chih-Wei Yao ; Seungchan Heo ; Thomas Byunghak Cho ; Inyup Kang**
A Mm-Wave Wideband MIMO RX With Instinctual Array-Based Blocker/Signal Management for Ultralow-Latency Communication **Min-Yu Huang ; Hua Wang**
A 42.2-Gb/s 4.3-pJ/b 60-GHz Digital Transmitter With 12-b/Symbol Polarization MIMO **Chintan Thakkar ; Anandaroop Chakrabarti ; Shuhei Yamada ; Debabani Choudhury ; James Jaussi ; Bryan Casper**
An 80-Gb/s 300-GHz-Band Single-Chip CMOS Transceiver **Sangyeop Lee ; Shinsuke Hara ; Takeshi Yoshida ; Shuhei Amakawa ; Ruibing Dong ; Akifumi Kasamatsu ; Junji Sato ; Minoru Fujishima**

IEEE Solid-State Circuits Letters

Issue 9, September 2019

Special Issue on the 2019 IEEE International Solid-State Circuits Conference

Introduction to the Special Issue on the 2019 International Solid-State Circuits Conference Mingoo Soek ; Jason Stauth ; Mike Chen ; Sudhakar Pamarti ; Arun Natarajan
An Energy-Efficient Deep Reinforcement Learning Accelerator With Transposable PE Array and Experience Compression Changhyeon Kim ; Sanghoon Kang ; Sungpill Choi ; Dongjoo Shin ; Youngwoo Kim ; Hoi-Jun Yoo
An Energy-Efficient Sparse Deep-Neural-Network Learning Accelerator With Fine-Grained Mixed Precision of FP8-FP16 Jinsu Lee ; Juhyoung Lee ; Donghyeon Han ; Jinmook Lee ; Gwangtae Park ; Hoi-Jun Yoo
A 3-Ratio 85% Efficient Resonant SC Converter With On-Chip Coil for Li-Ion Battery

Operation
Peter Renz ; Maik Kaufmann ; Michael Lueders ; Bernhard Wicht

A Passive-Stacked Third-Order Buck Converter With Inherent Input Filtering Achieving 0.7-W/mm 2 Power Density and 94% Peak Efficiency
Abdullah Abdulslam ; Patrick P. Mercier

A Current-Mode Digital AOT 4-Phase Buck Voltage Regulator
Minho Choi ; Chan-Ho Kye ; Jonghyun Oh ; Min-Seong Choo ; Deog-Kyoon Jeong

A 1.41-pJ/b 56-Gb/s PAM-4 Receiver Using Enhanced Transition Utilization CDR and Genetic Adaptation Algorithms in 7-nm CMOS
Behzad Dehlaghi ; Shayan Shahramian ; Joshua Liang ; Ryan Bespalko ; Dustin Dunwell ; James Bailey ; Bo Wang ; Alireza Sharif-Bakhtiar ; Michael O'Farrell ; Kerry Tang ; Anthony Chan Carusone ; David Cassan ; Davide Tonietto

A 36-Gb/s Adaptive Baud-Rate CDR With CTLE and 1-Tap DFE in 28-nm CMOS
Danny Yoo ; Mohammad Bagherbeik ; Wahid Rahman ; Ali Sheikholeslami ; Hirotaka Tamura ; Takayuki Shibasaki

An Ultralow Power Burst-Chirp UWB Radar Transceiver for Indoor Vital Signs and Occupancy Sensing in 40-nm CMOS
Yao-Hong Liu ; Sunil Sheelavant ; Marco Mercuri ; Paul Mateman ; Masoud Babaie

A Mixed-Signal Circuit Technique for Cancellation of Multiple Modulated Spurs in 4G/5G Carrier Aggregation Transceivers
Silvester Sadjina ; Ram Sunil Kanumalli ; Krzysztof Dufrêne ; Mario Huemer ; Harald Pretl

4.48-GHz Fractional- N Frequency Synthesizer With Spurious-Tone Suppression via Probability Mass Redistribution
Yann Donnelly ; Michael Peter Kennedy ; James Breslin ; Stefano Tulisi ; Sanganagouda Patil ; Ciarán Curtin ; Stephen Brookes ; Brian Shelly ; Patrick Griffin ; Michael Keaveney

A 13.5-dBm 200-255-GHz 4-Way Power Amplifier and Frequency Source in 130-nm BiCMOS
Mohamed Hussein Eissa ; Andrea Malignaggi ; Dietmar Kissinger

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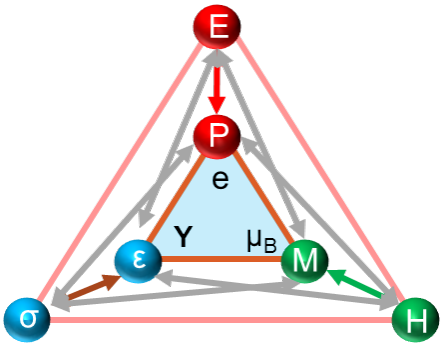
IEEE Journal on Exploratory Solid-State Computational Devices and Circuits

Issue 2, Part 1 - December 2019



Nonvolatile Spintronic Memory Cells for Neural Networks
Andrew W. Stephan ; Qiuwen Lou ; Michael T. Niemier ; Xiaobo Sharon Hu ; Steven J. Koester

JxCDC papers listed in order of popularity can be found online HERE.

For paper submission details, click HERE.

EDUCATION

December 2019 Distinguished Lectures

SSCS Taipei	Binaural Hearing Aid System and the Intelligent Acoustic Signal Processing - Presented by Zhihua Wang	December 3, 2019	National Taiwan University, Taipei, Taiwan **For more information, click here**
SSCS Taiwan	Design Challenges of RF transceiver satisfying the requirements of medical applications - Presented by Zhihua Wang	December 3, 2019	National Chiao Tung University, Hsinchu, Taiwan **For more information, click here**

CALL FOR PAPERS

Call for Papers: RFIC 2020

2020 IEEE Radio Frequency Integrated Circuits Symposium
June 21-23, 2020
Los Angeles, CA
https://www.rfic-ieee.org/

NEW for RFIC 2020: The RFIC symposium is expanding its scope to include System Applications and Interactive Demonstrations. This includes systems and applications in 5G, radar, imaging, terahertz, biomedical, and optoelectronic areas. In addition to the Emerging Circuit Technology area introduced in RFIC 2019, this year the symposium has introduced a completely new System Applications area and sub-committee that targets advanced system presentations in a range of topics related to communication, radar, imaging, sensing, and biomedical. To further highlight the systems aspects and enrich our attendees' experience, selected papers from this area will also be presented in a new Interactive Demonstration session.

The symposium starts on Sunday, 21 June 2020 with workshops and short courses, followed by two exciting plenary talks. Immediately following the plenary session, we will be holding an RFIC 'interactive' Sunday reception that will highlight our industry show-case and student papers finalists for an engaging social and technical evening event. Monday, 22 June and Tuesday, 23 June will be comprised of oral paper presentations, an interactive demonstration, and entertaining panel sessions.

We invite authors to submit their technical papers via the RFIC 2020 website; author's guidelines and **Call for Papers can be found here** . Complete information on how and when to submit a paper will be posted on the RFIC 2020 website. The conference will solicit papers describing original work in RFIC circuits, systems engineering, design methodology, RF modeling and CAD simulation, RFIC technologies, device technologies, fabrication, testing, reliability, packaging, and modules to support RF applications in areas such as Wireless Cellular and Connectivity, Low Power Transceivers, Receiver Sub-Systems and Circuits, Mixed-Signal RF and Data Converters, Reconfigurable and Tunable Front-Ends, Transmitter Sub-Systems and Power Amplifiers, Oscillators, Frequency Synthesis, Millimeter- and Sub-Millimeter Wave Systems, and High-Speed Data Transceivers.

Same as last year, a double-blind review process will be adopted to ensure anonymity for both authors and reviewers. Detailed instructions on how to submit a paper compliant with double-blind rules will be posted on the RFIC 2020 website.

Electronic Submission Deadlines:
Technical Paper Summaries in PDF format: 10 January 2020
Final Manuscripts for the Digest and Attendee Download: 23 March 2020

All submissions must be made at rfic-ieee.org in pdf form. Hard Copies are not accepted.

DOWNLOAD the RFIC 2020 Call for Papers

Call for Papers: IEEE Journal on Exploratory Solid-State Computational Devices and Circuits

Special Topic on "Exploratory Devices and Circuits for Compute-in-Memory"

Aims and Scope:

Deep learning and non-convex optimization problems are well known to be data-intensive applications. While graphic processing units (GPU) have become the mainstream platform to accelerate the algorithms in the cloud, there is a growing interest to develop application-specific integrated-circuit (ASIC) chips for further improving the energy-efficiency for these data-intensive workloads. Digital multiply-and-accumulate (MAC) arrays are generally employed as ASIC solutions, and data flow is often optimized to increase the data reuse on-chip. Nevertheless, most of the inputs and outputs are moved across MAC arrays and from global buffers . Therefore, it is more attractive to embed the MAC computations into the memory array itself, namely compute-in-memory (CiM), to minimize the data transfer. In C iM, the vector-matrix multiplication is executed in parallel (with analog computation) where the input vectors activate multiple rows.The dot-product is obtained as the multiplication of input voltage and cell conductance, and the partial sum is added up by the column current. An analog-to-digital converter (ADC) at the edge of the array generally converts the partial sum to binary bits for further digital processing.

To implement CiM, mature SRAM technologies (possibly with modified bit cells) have been proposed. However, SRAM is inherently volatile, anIEd consumes significant standby leakage power. In this sense, emerging non-volatile memory (eNVM) technologies are better suited for the area/power constraint platforms, as they could be turned on and off instantly without losing the stored weights. eNVMs of industry's interest here include resistive random access memory (RRAM), phase change memory (PCM), spin-transfer-torque magnetic random access memory (STT-MRAM) and ferroelectric field effect transistor (FeFET). In recent years, the industry has heavily invested in the commercialization of eNVM technologies, e.g. TSMC's 40nm RRAM, Intel's 22nm RRAM, TSMC's 40nm PCM, Intel's 22nm STT-MRAM, and Samsung's 28 nm STT-MRAM, while doped HfO2 based FeFET technology is also emerging, e.g. Globalfoundries' FeFET at 22nm.

Capitalizing on these developments, eNVM based CiM designs have also become viable. This special issue of the IEEE Journal on Exploratory Computational Devices and Circuits (JXCDC) aims to call for the recent research advances in the area of the compute-in-memory spanning devices, circuits, and systems. Papers on the interaction and co-optimization of the materials and devices as well as circuits and architecture are solicited.

Topics of Interest include but are not limited to:

Prospective authors are invited to submit original works and/or extended works based on conference presentations on various aspects of compute-in-memory. Memory technologies of interest include (but not limited to) SRAM, DRAM, NOR/NAND Flash, and emerging NVM devices such as PCM, RRAM/CBRAM, STT-MRAM/SOT-MRAM (or other spintronic memories), FeFET (or other ferroelectric memories), etc. The following topics are specifically solicited:

- Materials and devices that can enable compute-in-memory
- Integration of emerging technologies with silicon for compute-in-memory
- Crossbar array design for compute-in-memory
- Array-level demonstration for compute-in-memory
- Peripheral circuit design for compute-in-memory
- Architectural-level design for compute-in-memory
- Algorithms and hardware co-design for compute-in-memory
- Benchmarking simulators for compute-in-memory
- New applications for compute-in-memory beyond deep learning

Submission Guidelines:

The IEEE Journal on Exploratory Solid-State Computational Devices and Circuits (J XCDC) IS AN OPEN ACCESS PUBLICATION: The Open Access Fee is: $1,350 USD per article. Article

submissions must be done through the ScholarOne Manuscripts website:
https://mc.manuscriptcentral.com/jxcdc.

View our guidelines for papers and supplementary materials, as well as paper templates.

Important Dates:
Open for Submission: December 1st, 2019
Submission Deadline: February 1st, 2020
First Notification: March 1st, 2020
Revision Submission: April 1st, 2020
Final Decision: May 1st, 2020
Publication Online: June 1st, 2020

Guest Editor:
Shimeng Yu, Georgia Institute of Technology, **shimeng.yu@ece.gatech.edu**

Deputy Editor:
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Inquiries for the JxCDC Journal should be sent to: JXCDC@IEEE.ORG

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- Circuits & Systems Society
- Council on Electronic Design Automation
- Electron Devices Society
- Council on Superconductivity

Call for Papers: 2020 Symposia on VLSI

Technology and Circuits
June 14-19, 2020
Honolulu, Hawaii
https://vlsisymposium.org

Celebrating its 40th edition in 2020, the VLSI Symposia is the premier international conference on semiconductor technology and circuits. It offers a superb opportunity to interact and synergize on topics spanning the range from new neuromorphic devices, to beyond-the-state-of-the-art process technology to systems-on-chip and AI accelerators.

The circuits symposium is placing special emphasis on several innovation system focus areas, and encourages paper submissions on:

- Machine and deep learning
- FPGA-based accelerators
- Internet of Things
- Industrial electronics
- Big Data management
- Biomedical applications
- Robotics and autonomous transportation

In addition, submissions are welcomed in all of the following circuits areas:

- Processors, SoCs, and Machine Learning
- Digital circuits, signal integrity, and IOs
- Hardware security
- Memory circuits, architectures, and interfaces

- Biomedical circuits
- Sensors, imagers, and display circuits
- Power conversion circuits
- Analog, amplifier and filter circuits
- Wireless receivers and transmitters
- Data converters
- Frequency generation and clock circuits
- Wireline and optical transceivers

The technology symposium calls for papers in the following areas:

- Technologies for "Internet of Things"
- Technologies for Artificial Intelligence and Machine Learning Applications
- Stand-Alone and Embedded Static, Dynamic, non-Volatile and Emerging Memory
- Technologies
- CMOS Technology for Microprocessors and SoCs
- RF / Analog / Digital and Sensors Technologies
- New Process Technologies and Electronic Materials
- Advanced Packaging, System-in-Package (SiP) and 3D Technologies
- Photonics and Imaging Technologies
- Beyond CMOS Devices and Technologies for Heterogeneous Integration

Papers will be selected based on technical innovation, advances relative to previously published work, credibility of claims, and quality of writing and illustrations

Submission Information
Paper Submission Deadline: Monday, February 10, 2020, 23:59 PST

For more information, click here.

CONFERENCES

Upcoming 2020 SSCS-Sponsored Conferences

2020 IEEE International Solid-State Circuits Conference (ISSCC) San Francisco, California	**Feb 16 - 20, 2020**
2020 Design, Automation & Test in Europe Conference & Exhibition (DATE) Grenoble Cedex 2, France	**Mar 9 - 13, 2020**
2020 IEEE Custom Integrated Circuits Conference (CICC) Boston, MA	**Mar 22 - 25, 2020**
2020 International Symposium on VLSI Technology, Systems, and Applications (VLSI-TSA) Hsinchu, Taiwan	**Apr 20 - 23, 2020**
2020 International Symposium on VLSI Design, Automation, and Test (VLSI-DAT) Hsinchu, Taiwan	**Apr 20 - 23, 2020**
2020 IEEE Symposia on VLSI Technology and Circuits Honolulu, Hawaii	**Jun 16 - 19, 2020**
2020 IEEE Radio Frequency Integrated Circuits Symposium (RFIC) Los Angeles, California	**Jun 21 - 23, 2020**

SSCS-Sponsored Conferences: Proceedings

Click the links below to access the latest SSCS-Sponsored conference proceedings.

2018

2018 IEEE International Solid-State Circuits Conference (ISSCC)
2018 IEEE Custom Integrated Circuits Conference (CICC)
2018 IEEE Symposium on VLSI Circuits (VLSI)
2018 IEEE 44th European Solid-State Circuits Conference (ESSCIRC)
2018 IEEE Asian Solid-State Circuits Conference (A-SSCC)

2019

2019 IEEE International Solid-State Circuits Conference (ISSCC)
2019 IEEE Custom Integrated Circuits Conference (CICC)
2019 Symposium on VLSI Circuits
2019 IEEE 45th European Solid-State Circuits Conference (ESSCIRC)

For Society news and happenings, check out the Fall 2019 issue of the Solid-State Circuits Magazine.
