IEEE SOLID-STATE CIRCUITS SOCIETY

Where ICs are in IEEE

May 2019

UPCOMING WEBINAR

Cyrogenic CMOS Interfaces for Large-Scale Quantum Computers

Presented by Prof. Fabio Sebastiano
Delft University of Technology
The Netherlands

Thursday, June 27, 2019
10:00 AM Eastern Time (New York)

CLICK HERE TO REGISTER

ABSTRACT: Quantum computers hold the promise to ignite the next technological revolution as the classical computer did for last century's digital revolution, by efficiently solving problems that are intractable by today's computers. By enabling the efficient simulation of quantum systems, quantum computing will allow both the optimization of existing industrial processes and the synthesis of new drugs and materials, thus representing an unprecedented game changer with the potential to disrupt entire industries, create new ones and radically change our lives.
Quantum computers rely on processing the information stored in quantum bits (qubits) that must be typically cooled well below 1 K for proper operation. Performing operations on qubits requires a classical (i.e. non-quantum) electronic interface, which is currently implemented at room temperature for the few qubits available today. However, future quantum processors will comprise thousands or even millions of qubits. To avoid the unpractical requirement of thousands of cables from the cryogenic refrigerator to the room-temperature electronics, the electronic interface must operate at cryogenic temperatures as close as possible to the qubits.

This talk will address the challenges of building such a scalable cryogenic electronic interface, focusing on the use of standard CMOS technology. A brief introduction to quantum computers and their operation will be given, followed by a description of their hardware implementation and their requirements in terms of electronic control and read-out. To enable the reliable design of cryogenic circuits, two main ingredients are required: on one hand, compact models for the cryogenic CMOS devices and, on the other hand, a comprehensive methodology to co-design the electronics and the quantum processor. After addressing those aspects, we will demonstrate the design and the functionality of complex analog and digital systems operating at 4 K, thus showing that cryogenic CMOS is a viable technology to enable large-scale quantum computing.

BIOGRAPHY: Fabio Sebastiano holds degrees from University of Pisa, Italy (B.Sc., 2003, cum laude; M.Sc., 2005, cum laude), from Sant'Anna School of Advanced Studies, Pisa, Italy (M.Sc., 2006, cum laude) and from Delft University of Technology, The Netherlands (Ph.D., 2011). From 2006 to 2013, he was with NXP Semiconductors Research in Eindhoven, The Netherlands, where he conducted research on fully integrated CMOS frequency references, nanometer-CMOS temperature sensors and area-efficient interfaces for magnetic sensors. In 2013, he joined Delft University of Technology, where he is currently an Assistant Professor (tenured). His main research interests are cryogenic electronic interfaces, quantum computation, fully-integrated frequency references and electronic interfaces for smart sensors. Dr. Sebastiano holds 10 patents, and has co-authored 1 book and over 60 technical publications. He has given invited talks and courses at several international conferences including the International Solid-State Circuits Conference (ISSCC). He was co-recipient of the 2008 ISCAS Best Student Paper Award and of the 2017 DATE best IP award. Fabio serves as TPC member of the IEEE RFIC Symposium in the "Emerging technologies" subcommittee and as associate editor of the IEEE Transactions on Very Large Scale Integration Systems (TVLSI). He is a senior member of IEEE and a Distinguished Lecturer of the IEEE Solid-State Circuit Society.

Starting January 1, 2019, SSCS will be charging for CEU's and PDH's. Attendees of webinars will have to pay a fee to obtain CEU's and PDH's. However, webinar attendees can obtain a complimentary certificate of attendance.

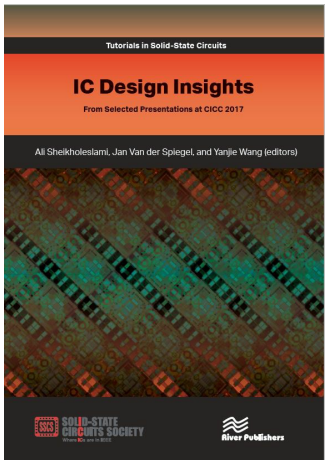
NEWS

Upcoming SSCS AdCom Election and Petition Process for Term 2020-2022

Each year, SSCS rotates out the five Member-at-Larges whose term on the AdCom will be ending in December. This is done through the annual SSCS AdCom Election, which is organized by the SSCS Nominations Committee and Chaired by the current SSCS Past President. This year, the Chair is Jan Van der Spiegel and the election term is 2020-2022. This election will be held around October/November 2019.

The current Nominations Slate for the 2019 SSCS AdCom Election for 2020-2022 Member-at-Large is now posted on the **SSCS website**. At this time, we are opening the Petition Process for this upcoming election to anyone who would like to petition to be a candidate in the election. Please see the **Petition Process information** located below the Slate on the SSCS website, if you would like to be a petitioner.

NEW SSCS MEMBER BENEFITS



IC Design Insights eBook

Now available for download on the SSCS Resource Center!

Click here to download!

This book contains a selection of tutorial and invited presentations that were given at the IEEE CICC 2017 in Austin, TX. The selection of the talks was made to provide a comprehensive coverage of key topics, including Circuits Techniques for mm-wave front-ends, RF and mm-wave receivers and frequency synthesis, data and DC-DC converters, and techniques for IoT security. The book is part of an educational initiative of the IEEE Solid-State Circuits Society to offer its members state of the art educational material.

SSCS YouTube Channel

SSCS now has a **YouTube Channel** where all CONFedu videos are posted including VLSIx 2016, CICCx 2017, and ISSCCedu 2018. **Coming Soon:** ESSCIRCedu 2018, CICCedu 2019, and VLSIedu 2019!

New Episodes - SSCS Chip Chat Podcast

SSCS Chip Chat

SCS' educational programming has expanded to include a podcast called SSCS Chip Chat. This interview style podcast focuses on the stories of engineers and scientists behind the integrated circuits that power the world.

The podcast can be listened to by searching SSCS Chip Chat in the Apple Podcast App or whatever podcast app you use for your mobile device.

You can also listen to the podcast online. **Click here to listen!**

Episode 1: Dr. Gert Cauwenberghs
Episode 2: Albert Theuwissen
Episode 3: Shanthi Pavan
Episode 4: R. Jacob Baker
Episode 5: Shantanu Chakrabartty
Episode 6: Alice Wang - **NEW**

PUBLICATIONS

The latest in SSCS Flagship Publications...

IEEE Journal of Solid-State Circuits

Vol. 54, Issue 6, June 2019

A 1.5-1.9-GHz All-Digital Tri-Phasing Transmitter With an Integrated Multilevel Class-D Power Amplifier Achieving 100-MHz RF Bandwidth Jerry Lemberg ; Mikko Martelius ; Enrico Roverato ; Yury Antonov ; Tero Nieminen ; Kari Stadius
Wide-Band RF Front End for SAW-Less Receivers Employing Active Feedback and Far Out-of-Band Blocker Rejection Circuit Amirhossein Rasekh ; Mehrdad Sharif Bakhtiar
A CMOS MedRadio Transceiver With Supply-Modulated Power Saving Technique for an Implantable Brain-Machine Interface System Mao-Cheng Lee ; Alireza Karimi-Bidhendi ; Omid Malekzadeh-Arasteh ; Po T. Wang ; An H. Do ; Zoran Nenadic ; Payam Heydari
A Multi-Loop-Controlled AC-Coupling Supply Modulator With a Mode-Switching CMOS PA in an EER System With Envelope Shaping Xun Liu ; Heng Zhang ; Philip K. T. Mok ; Howard C. Luong
A Low-Jitter Injection-Locked Multi-Frequency Generator Using Digitally Controlled Oscillators and Time-Interleaved Calibration Heein Yoon ; Suneui Park ; Jaehyouk Choi
A Compact Dual-Band Digital Polar Doherty Power Amplifier Using Parallel-Combining Transformer Yun Yin ; Liang Xiong ; Yiting Zhu ; Bowen Chen ; Hao Min ; Hongtao Xu
A 28-/37-/39-GHz Linear Doherty Power Amplifier in Silicon for 5G Applications Song Hu ; Fei Wang ; Hua Wang
A Millimeter-Wave CMOS Transceiver With Digitally Pre-Distorted PAM-4 Modulation for Contactless Communications Yanghyo Kim ; Boyu Hu ; Yuan Du ; Wei-Han Cho ; Rulin Huang ; Adrian Tang ; Huan-Neng Chen ; Chewnpu Jou ; Jason Cong ; Tatsuo Itoh ; Mau-Chung Frank Chang
A 230-260-GHz Wideband and High-Gain Amplifier in 65-nm CMOS Based on Dual-Peak Gmax -Core Dae-Woong Park ; Dzuhri Radityo Utomo ; Bao Huu Lam ; Sang-Gug Lee ; Jong-Phil Hong
A Calibration-Free 12-bit 50-MS/s Full-Analog SAR ADC With Feedback Zero-Crossing Detectors Kwuang-Han Chang ; Chih-Cheng Hsieh
A Second-Order Noise-Shaping SAR ADC With Passive Integrator and Tri-Level Voting Haoyu Zhuang ; Wenjuan Guo ; Jiaxin Liu ; He Tang ; Zhangming Zhu ; Long Chen ; Nan Sun
A 0.4-V 13-bit 270-kS/s SAR-ISDM ADC With Opamp-Less Time-Domain Integrator

Sung-En Hsieh ; Chih-Cheng Hsieh

Reference-Less Time-Division Duplex Transceiver IC for a Renal Denervation System
Jaehyeok Yang ; Seohyeon Kim ; Gunpil Hwang ; Kyeongha Kwon ; Sejun Jeon ; Hyeon-Min Bae

A Low-Power Bidirectional Link With a Direct Data-Sequencing Blind Oversampling CDR
Sudip Shekhar ; Rajesh Inti ; James Jaussi ; Tzu-Chien Hsueh ; Bryan K. Casper

A 25-Gb/s Avalanche Photodetector-Based Burst-Mode Optical Receiver With 2.24-ns Reconfiguration Time in 28-nm CMOS
Kuan Chang Chen ; Azita Emami

A Mutual Capacitance Touch Readout IC With 64% Reduced-Power Adiabatic Driving Over Heavily Coupled Touch Screen
Jiheon Park ; Young-Ha Hwang ; Jonghyun Oh ; Yoonho Song ; Jun-Eun Park ; Deog-Kyoon Jeong

A CMOS SPAD Line Sensor With Per-Pixel Histogramming TDC for Time-Resolved Multispectral Imaging
Ahmet T. Erdogan ; Richard Walker ; Neil Finlayson ; Nikola Krstajić ; Gareth Williams ; John Girkin ; Robert Henderson

A 14-nA, Highly Efficient Triple-Output Thermoelectric Energy Harvesting System Based on a Reconfigurable TEG Array
Qiping Wan ; Philip K. T. Mok

A Fully Integrated Split-Electrode SSHC Rectifier for Piezoelectric Energy Harvesting
Sijun Du ; Yu Jia ; Chun Zhao ; Gehan A. J. Amaratunga ; Ashwin A. Seshia

A 13.56 MHz, 94.1% Peak Efficiency CMOS Active Rectifier With Adaptive Delay Time Control for Wireless Power Transmission Systems
Zhongming Xue ; Shiquan Fan ; Dan Li ; Lina Zhang ; Wei Gou ; Li Geng

A 25-MHz Four-Phase SAW Hysteretic Control DC-DC Converter With 1-Cycle Active Phase Count
Bumkil Lee ; Min Kyu Song ; Ashis Maity ; D. Brian Ma

Design of an Always-On Deep Neural Network-Based 1- u W Voice Activity Detector Aided With a Customized Software Model for Analog Feature Extraction
Minhao Yang ; Chung-Heng Yeh ; Yiyin Zhou ; Joao P. Cerqueira ; Aurel A. Lazar ; Mingoo Seok

A 3-D IC for Mitigating Energy of Memory Accessing and Data Movement in Accelerator- Based Streaming Architectures
Lung-Yen Chen ; Sen Tao ; Naveen Verma

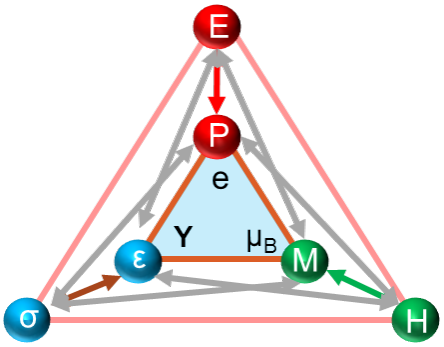
A 64-Tile 2.4-Mb In-Memory-Computing CNN Accelerator Employing Charge-Domain Compute
Hossein Valavi ; Peter J. Ramadge ; Eric Nestler ; Naveen Verma

3-D NAND Flash Value-Aware SSD: Error-Tolerant SSD Without ECCs for Image Recognition
Yoshiaki Deguchi ; Toshiki Nakamura ; Atsuna Hayakawa ; Ken Takeuchi

A Reference-Free Temperature-Dependency-Compensating Readout Scheme for Phase-Change Memory Using Flash-ADC-Configured Sense Amplifiers
Dong-Hwan Jin ; Ji-Wook Kwon ; Min-Jae Seo ; Mi-Young Kim ; Min-Chul Shin ; Seok-Joon Kang ; Jung-Hyuk Yoon ; Taek-Seung Kim ; Seung-Tak Ryu

IEEE Journal on Exploratory Solid-State Computational Devices and Circuits

Early Access Articles



Boosted Spin Channel Networks for Energy-efficient Inference Ameya D. Patil ; Sasikanth Manipatruni ; Dmitri E. Nikonov ; Ian A. Young ; Naresh R. Shanbhag
Using Floating Gate Memory to Train Ideal Accuracy Neural Networks Sapan Agarwal ; Diana Garland ; John Niroula ; Robin B. Jacobs-Gedrim ; Alex Hsia ; Michael S. Van Heukel
Unsupervised learning to overcome catastrophic forgetting in neural networks Irene Muñoz-Martín ; Stefano Bianchi ; Giacomo Pedretti ; Octavian Melnic ; Stefano Ambrogio ; Daniele Ielmini
Performance Estimate of Inverse Rashba-Edelstein Magnetoelectric Devices for Neuromorphic Computing Andrew W. Stephan ; Jiaxi Hu ; Steven J. Koester
Graded-Anisotropy-Induced Magnetic Domain Wall Drift for an Artificial Spintronic Leaky Integrate-and-Fire Neuron Wesley H. Brigner ; Xuan Hu ; Naimul Hassan ; Christopher H. Bennett ; Jean Anne C. Incorvia ; Felipe Garcia-Sanchez ; Joseph S. Friedman
Subthreshold Spintronic Stochastic Spiking Neural Networks with Probabilistic Hebbian Plasticity and Homeostasis Steven D. Pyle ; Ramtin Zand ; Shadi Sheikhfaal ; Ronald F. DeMara

JxCDC papers listed in order of popularity can be found online HERE.

For paper submission details, click HERE.

IEEE Solid-State Circuits Letters

Issue 1, January 2019

A 1-GS/s 20 MHz-BW Capacitive-Input Continuous-Time Delta Sigma ADC Using a Novel Parasitic Pole-Mitigated Fully Differential VCO Abhishek Mukherjee ; Miguel Gandara ; Biying Xu ; Shaolan Li ; Linxiao Shen ; Xiyuan Tang ; David Pan ; Nan Sun
A 0.4-ps-Jitter -52-dBc-Spur Synthesizable Injection-Locked PLL With Self-Clocked Nonoverlap Update and Slope-Balanced Subsampling BBPD Bangan Liu ; Huy Cu Ngo ; Kengo Nakata ; Wei Deng ; Yuncheng Zhang ; Junjun Qiu ; Toru Yoshioka ; Jun Emmei ; Jian Pang ; Aravind Tharayil Narayanan ; Haosheng Zhang ; Dongsheng Yang ; Hanli Liu ; Teruki Someya ; Atsushi Shirane ; Kenichi Okada

EDUCATION

June 2019 Distinguished Lectures

SSCS Kansai	"Adaptive and Resilient Circuits for Processors" - Presented by Keith Bowman	June 14, 2019	Mielparque Kyoto **For more information, please click here.**
SSCS Oregon	Talk Title TBD - Presented by Sudhakar Pamarti	June 26, 2019	Oregon **For more information, please click here**
SSCS Germany	"Implantable electronics with Data and Power Telemetry" - Presented by Maurits Ortmanns	June 26, 2019	University of Rostock **For more information, please click here**

CONFERENCES

Upcoming SSCS-Sponsored Conferences

2019 IEEE Radio Frequency Integrated Circuits Symposium (RFIC) Boston, Massachusetts	**June 2 - 4, 2019**
2019 Symposium on VLSI Circuits Kyoto, Japan	**June 9 - 14, 2019**
2019 IEEE Hot Chips 31 Symposium (HCS) Cupertino, California	**August 18 - 29, 2019**
ESSCIRC/ESSDERC 2019 - IEEE 45th European Solid-State Circuits Conference (ESSCIRC)/49th European Solid-State Device Research Conference Cracow, Poland	**September 23 - 26, 2019**
2019 IEEE Biomedical Circuits and Systems Conference (BioCAS) Nara, Japan	**October 17 - 19, 2019**
2019 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS) Nashville, Tennessee	**November 3 - 6, 2019**
2019 IEEE Asian Solid-State Circuits Conference (A-SSCC) Macau, China	**November 4 - 6, 2019**

SSCS-Sponsored Conferences: Proceedings

Click the links below to access the latest SSCS-Sponsored conference proceedings.

2018

2018 IEEE International Solid-State Circuits Conference (ISSCC)
2018 IEEE Custom Integrated Circuits Conference (CICC)
2018 IEEE Symposium on VLSI Circuits (VLSI)
2018 IEEE 44th European Solid-State Circuits Conference (ESSCIRC)
2018 IEEE Asian Solid-State Circuits Conference (A-SSCC)

2019
2019 IEEE International Solid-State Circuits Conference (ISSCC)

Hot Chips: A Symposium on High Performance Chips

8 - 20 August, 2019

Stanford University Campus, California

Since it started in 1989, HOT CHIPS has been known as one of the semiconductor industry's leading conferences on high-performance microprocessors and related integrated circuits. The conference is held once a year in August in the center of the world's capital of electronics activity, Silicon Valley.

Program At-A-Glance

Sunday, 8/18/2019: Tutorials

- Morning Tutorials: Acceleration in the Cloud
- The Nitro Project - Next Generation AWS Infrastructure
- Microsoft Azure
- TPU V3 in Google Cloud: Architecture and Infrastructure
- Afternoon Tutorial: RISC-V
- Reception

Monday, 8/19/2019: Conference Day 1

- Opening Remarks
- General Purpose Compute
- Memory
- Keynote 1: "Delivering the Future of High-Performance Computing with System, Software and Silicon Co-Optimization" by Dr. Lisa Su, CEO, AMD
- Methodology and ML Systems
- ML Training
- Reception

Tuesday, 8/20/2019: Conference Day 2

- Embedded and Auto
- ML Inference
- Keynote 2: "What Will the Next Node Offer Us?" by Dr. Philip Wong, VP Corporate Research, TSMC
- Interconnects
- Break
- Packaging and Security
- Graphics and AR
- Closing Remarks

Click here to register!

IEEE Radio Frequency Integrated Circuits

Symposium

2-4 June 2019

Boston, Massachusetts

The **2019 IEEE Radio Frequency Integrated Circuits Symposium (RFIC 2019)** will be held in Boston, MA on 2-4 June 2019. The RFIC Symposium is an annual IEEE conference that is combined with the International Microwave Symposium (IMS), ARFTG, and the Industry Exhibition to form the "Microwave Week", the largest worldwide RF/microwave technical meeting of the year. In 2019, the conference will also extend its focus to emerging circuit technologies related to RFIC, such as MEMS sensors and actuators, heterogeneous and 3D ICs, silicon photonics, biomedical applications, quantum computing and more. We cordially invite you to participate in this international symposium.

To encourage student attendance, the IMS'19 is offering deep registration discounts and numerous benefits for student volunteers who are IEEE members and willing to help with conference activities. For more details, visit **https://ims-ieee.org/students-main/student-volunteers.**

For 2019, RFIC is promoting a new educational experience for the attendees: a "Technical Lecture" comprising a 1 ½ hour interactive short course delivered by a distinguished speaker during lunchtime on Sunday, between the AM and PM workshops. For 2019, Prof. Ali Niknejad from University of California, Berkeley, will teach "Fundamentals of mmWave IC Design in CMOS".

The 2019 RFIC Symposium will begin on Sunday, June 2nd 2019, with 12 RFIC focused workshops and one technical lecture. In addition, there will be several joint RFIC/IMS workshops on Sunday and Monday. These workshops cover a wide range of advanced topics in RFIC technology and IC design, including power amplifiers, 5G systems, silicon photonics, quantum computing, hardware security, and beyond. The 2019 RFIC Plenary Session on Sunday will conclude the day with two visionary plenary talks: Dr. Greg Henderson, Senior Vice President, Automotive, Communications and Aerospace/Defense at Analog Devices, will outline "The Digital Future of RFICs", and Dr. Ir. Michael Peeters, Program Director Connectivity and Humanized Technology at IMEC, will address the question "Do the networks of the future care about the materials of the past?". Immediately after the plenary session, the RFIC reception will follow, with highlight from our industry showcase and student paper finalists in an engaging social and technical evening event supported by the RFIC Symposium corporate sponsors. You will not want to miss the RFIC reception!

On Monday and Tuesday, the RFIC Symposium will have multiple tracks of oral technical paper sessions. The 5G Summit technical sessions on Tuesday afternoon will provide high-level 5G overview presentations that will complement the 5G-focused RFIC technical sessions on Tuesday morning. Two enlightening panels will be featured during lunchtime on both days: "The Internet of Things (IoT) - back to the future, or no future?" on Monday and "Will Artificial Intelligence (AI) and Machine Learning (ML) take away my job as an RF/Analog Designer?" on Tuesday.

On behalf of the RFIC Steering and Executive Committees, we welcome you to join us at the 2019 RFIC Symposium in Boston, Massachusetts! Please visit the RFIC 2019 website **(http://rfic-ieee.org/)** for more details and updates.

CALL FOR PAPERS

A-SSCC 2019 : Call for Papers

Asian Solid-State Circuits Conference

November 4 - 6, 2019

Macau, China

The IEEE A-SSCC 2019 (Asian Solid-State Circuits Conference) is an international forum

for presenting the most updated and advanced chips and circuit designs in solid-state and semiconductor fields. The conference is supported by the IEEE Solid-State Circuits Society and will be held in Asia. Further details on the conference and paper submission guidelines and templates will be available at the A-SSCC official website http://www.asscc.org/ (or **http://www.a-sscc2019.org**

Conference Theme: Silicon Systems for Next Smart Society

Solid-state circuits have improved our lives for more than 50 years. There is no doubt that we have benefited from a wide variety of electronic equip-men t such as mobile computing devices, car electronics and digitalized social infrastructures. Rapid progress of artificial intelligence accelerated by deep learning, in conjunction with big data collected by IoT, may change our lives non-linearly. As a consequence, we will use smarter mobile devices, drive or be driven by, smarter cars and live on a smarter infrastructure, leading to totally different quality of life. There, we will face new challenges and opportunities for silicon systems, which our community should overcome and take advantage of.

Prospective authors are invited to submit four-page or two-page manuscripts, including figures, tables and references. A-SSCC papers are solicited in the following categories:

Regular Session

1. **Analog Circuits & Systems:** Amplifiers, comparators, switched capacitor circuits, continuous-time & discrete-time filters, voltage/current references; DC-DC converters, power-control circuits; IF/baseband analog circuits, AGC/VGA; non-linear analog circuits.
2. **Data Converters:** Nyquist-rate and oversampling A/D, D/A converters, time-to-digital converters, and capacitance-to-digital converters; sub-circuits for data converters including sample-and-hold circuits, calibration circuits, etc.
3. **Digital Circuits & Systems:** Design, fabrication, and test of digital VLSI systems; high-speed low-power digital circuits, power-reduction and management methods for digital VLSI, ultra-low-voltage and sub-threshold logic design; leakage reduction techniques; clock distribution, I/O circuits, reconfigurable logic-array circuits; supply/substrate noise measurement and cancellation for digital VLSI, variation and fault-tolerant circuits.
4. **SoC & Signal Processing Systems:** System-on-chip(including 3D integration), microprocessors, network processors, baseband communication processing system & architectures, system-level power management; multimedia and recognition processing systems; cryptographic, security, machinelearning, deep-learning, and neuromorphic circuits and systems; bio-medical/neural-network processors and sensor network systems.
5. **RF:** Receivers/transmitters/transceivers for wireless systems; narrowband RF, ultra-wideband and millimeter-wave circuits; circuits and building-blocks including RF front-end, LNA, mixer, power amplifiers, VCOs, frequency synthesizers, RF filters, RF switches, power detectors, active antennas.
6. **Wireline:** Receivers/transmitters/transceivers for wireline systems; optical/electrical data links and backplane transceivers; power-line communication; clock generation circuits, PLL, DLL, spread-spectrum clock generation; building blocks for high-speed wireline communication; analog-digital mixedmode circuits.
7. **Emerging Technologies and Applications:** Advanced system designs and circuit solutions for technologies and applications including state-of-the-art devices and packaging technologies; flexible and printable electronics;silicon photonices;smart sensors and transducers; MEMS for analog, RF, and sensor applications; image sensors and displays; energy harvesting systems; transceiver systems; medical/bio-electronics/bio-inspired chip design,artificial intelligent system,and cryogenic circuits and systems.
8. **Memory:** Volatile and Non-volatile memory; new memory designs for 3D/2D architectures, emerging devices such as resistive-/phase change-/magnetic- /ferro-electric- memory devices; data storage and multi-bit-cell memory design; cache-memory system, multi-port memory, memory subsystem, processing in memory, and CAM design; yield-enhancing and ECC techniques; memory testing and built-in self-test.
9. **FPGA:** Novel algorithm and/or architecture for integrated circuits validated by FPGA implementation. The authors of accepted papers are required to participate in demo sessions.

Special Session

1. **Industry Program:** This special category accepts only papers based on state-of-

the-art industrial products. Strong emphasis on systems realized by silicon chips is encouraged. The papers should cover architecture, circuits, process technology, packaging and testing, includin g characterization results, die and system photos, as well as product demos.

2. **Student Design Contest:** A student design contest is held among the accepted papers with system prototypes or measurement results of which operations can be demonstrated on-site. Refer to the web for further information.

Papers related to integrated circuits for next smart society are highly solicited. Papers on low-power and/or low-voltage approaches, signal integrity, noise, test, and manufacturability for all the above categories are welcomed. Measurement results are highly recommended, especially for analog, and RF categories. Design methodologies for SiP, and SoC are included in the scope of the conference; the papers only describing CAD tools and CAD algorithms are not considered.

Submission Guidelines:
Papers must be submitted via the **A-SSCC website**. Authors must follow detailed instructions provided within the "Authors" section of the website, including the Authors' Guide and Pre-Publication Policy. Extended versions of selected papers from the Conference will be published in a Special Issue of the IEEE Journal of Solid-State Circuits.

Important Dates:
June 2, 2019: Paper Submission Deadline
August 5, 2019: Acceptance Notification
September 8, 2019: Final Paper Submission

BioCAS 2019 : Call for Papers

Biomedical Circuits and Systems Conference

October 17 - 19, 2019

Nara, Japan

BioCAS 2019 is a premier international forum for presenting the interdisciplinary research and development activities at the crossroads of medicine, life sciences, physical sciences and engineering that shape tomorrow's medical devices and healthcare systems.

This conference brings together members of our communities to broaden their knowledge in emerging areas of research at the interface of the life sciences and the circuits and systems engineering. The three-day single-track program for BioCAS 2019 is multidisciplinary in topics including but not limited to:

Biomedical Technologies:
* Assistive, Rehabilitation, and Quality of Life Technologies
* Biofeedback, Neuromodulation, and Closed-Loop Systems
* Bio-Inspired and Neuromorphic Circuits and Systems
* Biosensor Devices and Interface Circuits
* Biotelemetry and Energy Harvesting/Scavenging Circuits and Systems
* Body Area/Sensor Network and Wireless/Wearable Health Monitoring
* Electronics for Neuroscience
* Implantable Medical Electronics
* Lab-on-Chip and BioMEMS
* Point-of-Care Technologies for Healthcare

Biomedical Applications:
* Biomedical Imaging and Image Processing
* Biosignal Recording, Processing, and Machine Learning
* Human-Machine Interfaces
* Medical Information Systems and Bioinformatics

Submission Guidelines:
The complete 4-page paper (in standard IEEE double-column format), including the title, authors' names, affiliations and e-mail addresses, as well as a short abstract and an

optional demonstration video link (3 minute max) are requested. Papers must be submitted electronically in PDF format through **www.biocas2019.org.**

Important Dates:
Monday, June 10, 2019 - Regular Paper Submission Deadline
Monday, July 15, 2019 - Live Demo Submission Deadline
Monday, August 12, 2019 - Author Notification Date
Sunday, September 15, 2019 - Final Paper Submission Deadline

For Society news and happenings, check out the Winter 2019 issue of the Solid-State Circuits Magazine.