IEEE SOLID-STATE CIRCUITS SOCIETY

Where ICs are in IEEE

March 2019

NEWS

UPCOMING WEBINAR

"Adaptive and Resilient Circuits for Improving Processor Performance, Energy Efficiency, and Yield"

Presented by Keith A. Bowman
Wednesday, April 10th, 2019
11:00 AM ET

CLICK HERE TO REGISTER

ABSTRACT: Dynamic device, circuit, and system parameter variations degrade processor performance, energy efficiency, and yield across all market segments, ranging from small embedded cores in an Internet of Things (IoT) device to large CPUs in multicore servers. This seminar introduces the primary variations during the processor operational lifetime, including supply voltage droops, temperature changes, transistor aging, and workload fluctuations. This presentation then describes the negative impact of these variations on processor performance, energy efficiency, and yield. The wide dynamic voltage-frequency scaling (DVFS) range in today's processors increases these effects. For future IoT edge processors, the low-cost packaging, voltage regulation with time-varying energy harvesters, wide temperature range, and long-lifetime requirements exacerbate these problems further. To mitigate the adverse effects from dynamic variations, this seminar

presents adaptive and resilient circuits while highlighting the key design trade-offs and testing implications for product deployment.

BIOGRAPHY: Keith A. Bowman is a Principal Engineer and Manager in the Processor Research Team at Qualcomm Technologies, Inc. in Raleigh, NC. He is responsible for researching and developing circuit technologies for enhancing the performance and energy efficiency of Qualcomm processors. He pioneered the invention, design, and test of Qualcomm's first commercially successful circuit for mitigating the adverse effects of supply voltage droops on processor performance, energy efficiency, and yield. He received the B.S. degree from North Carolina State University and the M.S. and Ph.D. degrees from the Georgia Institute of Technology, all in electrical engineering. He previously worked in the Technology Computer-Aided Design (CAD) Group and the Circuit Research Lab at Intel Corporation in Hillsboro, OR. Dr. Bowman has published over 75 technical papers in refereed conferences and journals, authored one book chapter, received 17 patents, and presented over 35 tutorials on variation-tolerant circuit designs. He was the Technical Program Committee (TPC) Chair and the General Conference Chair for ISQED in 2012 and 2013, respectively, and for ICICDT in 2014 and 2015, respectively. Since 2016, he has served on the ISSCC TPC.

Starting January 1, 2019, SSCS will be charging for CEU's and PDH's. Attendees of webinars will have to pay a fee to obtain CEU's and PDH's. However, webinar attendees can obtain a complimentary certificate of attendance.

New Episodes - SSCS Chip Chat Podcast

SCS' educational programming has expanded to include a podcast called SSCS Chip Chat. This interview style podcast focuses on the stories of engineers and scientists behind the integrated circuits that power the world.

The podcast can be listened to by searching SSCS Chip Chat in the Apple Podcast App or whatever podcast app you use for your mobile device.

You can also listen to the podcast online. **Click here to listen!**

Episode 1: Dr. Gert Cauwenberghs
Episode 2: Albert Theuwissen
Episode 3: Shanthi Pavan
Episode 4: R. Jacob Baker
Episode 5: Shantanu Chakrabartty

Coming Soon! Episode 6: Alice Wang

PUBLICATIONS

The latest in SSCS Flagship Publications...

IEEE Journal of Solid-State Circuits

Vol. 54, Issue 3, March 2019

Special Section on the 2018 Custom Integrated Circuits Conference

Zhirui Zong ; Peng Chen ; Robert Bogdan Staszewski

Integrated Synthetic Fourth-Order Q -Enhanced Bandpass Filter With High Dynamic Range, Tunable Frequency, and Fractional Bandwidth Control
Farooq Amin ; Sanjay Raman ; Kwang-Jin Koh

Design and Analysis of a DCO-Based Phase-Tracking RF Receiver for IoT Applications
Yao-Hong Liu ; Vijaya Kumar Purushothaman ; Christian Bachmann ; Robert Bogdan Staszewski

A Harmonic-Selective Multi-Band Wireless Receiver With Digital Harmonic Rejection Calibration
Hao Wu ; David Murphy ; Hooman Darabi

A Wake-Up Receiver With a Multi-Stage Self-Mixer and With Enhanced Sensitivity When Using an Interferer as Local Oscillator
Vivek Mangal ; Peter R. Kinget

A 56-GS/s 8-bit Time-Interleaved ADC With ENOB and BW Enhancement Techniques in 28-nm CMOS
Kexu Sun ; Guanhua Wang ; Qing Zhang ; Salam Elahmadi ; Ping Gui

34-GBd Linear Transimpedance Amplifier for 200-Gb/s DP-16-QAM Optical Coherent Receivers
Mostafa G. Ahmed ; Tam N. Huynh ; Christopher Williams ; Yong Wang ; Pavan Kumar Hanumolu ; Alexander Rylyakov

A 53-Gbit/s Optical Receiver Frontend With 0.65 pJ/bit in 28-nm Bulk-CMOS
Laszlo Szilagyi ; Jan Pliva ; Ronny Henker ; David Schoeniger ; Jarosław P. Turkiewicz ; Frank Ellinger

An Energy-Efficient 3.7-nV Hz Bridge Readout IC With a Stable Bridge Offset Compensation Scheme
Hui Jiang ; Stoyan Nihtianov ; Kofi A. A. Makinwa

A Time-Domain-Controlled Current-Mode Buck Converter With Wide Output Voltage Range
Jin-Gyu Kang ; Jeongpyo Park ; Min-Gyu Jeong ; Changsik Yoo

An Inductive Voltage-/Current-Mode Integrated Power Management With Seamless Mode Transition and Energy Recycling
Hesam Sadeghi Gougheri ; Mehdi Kiani

A 130-nm Ferroelectric Nonvolatile System-on-Chip With Direct Peripheral Restore Architecture for Transient Computing System
Yongpan Liu ; Fang Su ; Yixiong Yang ; Zhibo Wang ; Yiqun Wang ; Zewei Li ; Xueqing Li ; Ryuji Yoshimura ; Takashi Naiki ; Takashi Tsuwa ; Takahiko Saito ; Zhongjun Wang ; Koji Taniuchi ; Huazhong Yang

Bitline Charge-Recycling SRAM Write Assist Circuitry for VMIN Improvement and Energy Saving
Hanwool Jeong ; Se Hyeok Oh ; Tae Woo Oh ; Hoonki Kim ; Chang Nam Park ; Woojin Rim ; Taejoong Song ; Seong-Ook Jung

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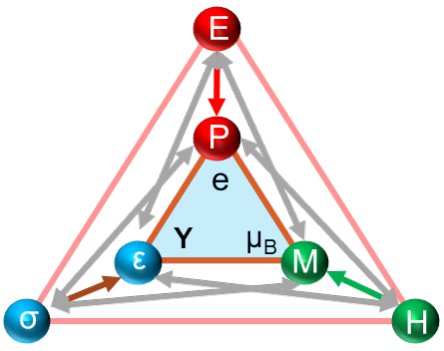
IEEE Journal on Exploratory Solid-State Computational Devices and Circuits

Issue 1, June 2019



Synchronous Circuit Design With Beyond-CMOS Magnetoelectric Spin-Orbit Devices Toward 100-mV Logic

Huichu Liu ; Sasikanth Manipatruni ; Daniel H. Morris ; Kaushik Vaidyanathan ; Dmitri E. Nikonov ; Tanay Karnik ; Ian A. Young

JxCDC papers listed in order of popularity can be found online HERE.

For paper submission details, click HERE.

IEEE Solid-State Circuits Letters

Issue 8, August 2018

An Adaptive-Resolution Quasi-Level-Crossing-Sampling ADC Based on Residue Quantization in 28-nm CMOS
Hongying Wang ; Filippo Schembari ; Marek Miśkowicz ; Robert Bogdan Staszewski

Large-Area Electronics HF RFID Reader Array for Object-Detecting Smart Surfaces
Yoni Mehlman ; Prakhar Kumar ; Murat Ozatay ; Sigurd Wagner ; James C. Sturm ; Naveen Verma

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EDUCATION

April 2019 Distinguished Lectures

SSCS Singapore	THz in CMOS: dream, nightmare or reality? - Presented by Patrick Reynaert	April 18, 2019	A*STAR Institute of Microelectronics, Singapore **For more information, please click here**
SSCS Austin	Talk Title TBD - Presented by Hua Wang	April 18, 2019	UT Austin, Texas **For more information, please click here**
SSCS/CAS Central Texas	Talk Title TBD - Presented by Salvatore Levantino	April 18, 2019	TBD **For more information, please click here**
SSCS/CAS Central Texas	Talk Title TBD - Presented by Timothy Dickson	April 19, 2019	TBD **For more information, please click here**
SSCS Tainan	Image sensors for biomedical applications - Presented by Jun	April 24, 2019	National Chung Cheng University **For more**

	Ohta		information, please click here

CONFERENCES

Upcoming SSCS-Sponsored Conferences

2019 IEEE Custom Integrated Circuits Conference (CICC) Austin, Texas	**April 14 - 17, 2019**
2019 International Symposium on VLSI Design, Automation and Test (VLSI-DAT) Hsinchu, Taiwan	**April 22 - 25, 2019**
2019 International Symposium on VLSI Technology, Systems, and Application (VLSI-TSA) Hsinchu, Taiwan	**April 22 - 25, 2019**
2019 IEEE Radio Frequency Integrated Circuits Symposium (RFIC) Boston, Massachusetts	**June 2 - 4, 2019**
2019 Symposium on VLSI Circuits Kyoto, Japan	**June 9 - 14, 2019**
2019 IEEE Hot Chips 31 Symposium (HCS) Cupertino, California	**August 18 - 29, 2019**
ESSCIRC 2019 - IEEE 45th European Solid-State Circuits Conference (ESSCIRC) Cracow, Poland	**September 23 - 26, 2019**
2019 IEEE Biomedical Circuits and Systems Conference (BioCAS) Nara, Japan	**October 17 - 19, 2019**
2019 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS) Nashville, Tennessee	**November 3 - 6, 2019**

SSCS-Sponsored Conferences: Proceedings

Click the links below to access the latest SSCS-Sponsored conference proceedings.

2018

2018 IEEE International Solid-State Circuits Conference (ISSCC)
2018 IEEE Custom Integrated Circuits Conference (CICC)
2018 IEEE Symposium on VLSI Circuits (VLSI)
2018 IEEE 44th European Solid-State Circuits Conference (ESSCIRC)
2018 IEEE Asian Solid-State Circuits Conference

2019

2019 IEEE International Solid-State Circuits Conference (ISSCC)

Call for Participation:

VLSI Technology, Systems, and Applications
VLSI Design, Automation and Test
22-25 April 2019
Hsinchu, Taiwan

REGISTER NOW!

VLSI-TSA https://expo.itri.org.tw/2019vlsitsa	VLSI-DAT https://expo.itri.org.tw/2019vlsidat
• 40 Selected Top Papers • 4 Special Sessions on - Silicon Photonics, Low Dimensional Devices and Materials, 3D/Heterogeneous Integration and Unconventional Manufacturing, Machine Learning for the Semiconductor Industry • **2 Profound Short Courses** • Best Student Paper Award	• 36 Selected Top Papers • 3 Special Sessions on - Advanced AI Chips and Applications, Silicon Photonics for Next Generation Chips, Heterogeneous Integration/Flexible Hybrid Electronics • 2 Industrial Sessions • **3 Profound Tutorials** • Best Paper Award

Joint Program Highlights

- Six Plenary Talks by Ghavam Shahidi, IBM Research ; Li Fung Chang, Industrial Technology Research Institute ; Winfried Kaiser, Carl Zeiss SMT GmbH ; Peter Hsieh, ARM ; Thomas Ernst, CEA-LETI ; Mike Davies, Intel
- Two Luncheon Keynotes by H-S. Philip Wong, Vice President of Corporate Research, TSMC ;Owain Vaughan, Chief Editor of Nature Electronics
- Two Joint Special Sessions on (5G: From Systems to Device) and (Future of Memory: From Storage to Computing)

IEEE Radio Frequency Integrated Circuits Symposium

2-4 June 2019
Boston, Massachusetts

The **2019 IEEE Radio Frequency Integrated Circuits Symposium (RFIC 2019)** will be held in Boston, MA on 2-4 June 2019. The RFIC Symposium is an annual IEEE conference that is combined with the International Microwave Symposium (IMS), ARFTG, and the Industry Exhibition to form the "Microwave Week", the largest worldwide RF/microwave technical meeting of the year. In 2019, the conference will also extend its focus to emerging circuit technologies related to RFIC, such as MEMS sensors and actuators, heterogeneous and 3D ICs, silicon photonics, biomedical applications, quantum computing and more. We cordially invite you to participate in this international symposium.

To encourage student attendance, the IMS'19 is offering deep registration discounts and numerous benefits for student volunteers who are IEEE members and willing to help with conference activities. For more details, visit **https://ims-ieee.org/students-main/student-volunteers.**

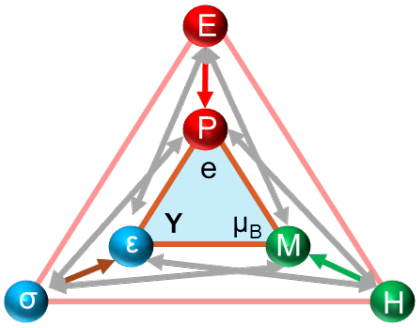
For 2019, RFIC is promoting a new educational experience for the attendees: a "Technical Lecture" comprising a 1 ½ hour interactive short course delivered by a distinguished speaker during lunchtime on Sunday, between the AM and PM workshops. For 2019, Prof. Ali Niknejad from University of California, Berkeley, will teach "Fundamentals of mmWave IC Design in CMOS".

The 2019 RFIC Symposium will begin on Sunday, June 2nd 2019, with 12 RFIC focused workshops and one technical lecture. In addition, there will be several joint RFIC/IMS workshops on Sunday and Monday. These workshops cover a wide range of advanced topics in RFIC technology and IC design, including power amplifiers, 5G systems, silicon photonics, quantum computing, hardware security, and beyond. The 2019 RFIC Plenary Session on Sunday will conclude the day with two visionary plenary talks: Dr. Greg Henderson, Senior Vice President, Automotive, Communications and Aerospace/Defense at Analog Devices, will outline "The Digital Future of RFICs", and Dr. Ir. Michael Peeters, Program Director Connectivity and Humanized Technology at IMEC, will address the question "Do the networks of the future care about the materials of the past?". Immediately after the plenary session, the RFIC reception will follow, with highlight from our industry showcase and student paper finalists in an engaging social and technical evening event supported by the RFIC Symposium corporate sponsors. You will not want to miss the RFIC reception!

On Monday and Tuesday, the RFIC Symposium will have multiple tracks of oral technical paper sessions. The 5G Summit technical sessions on Tuesday afternoon will provide high-level 5G overview presentations that will complement the 5G-focused RFIC technical sessions on Tuesday morning. Two enlightening panels will be featured during lunchtime on both days: "The Internet of Things (IoT) - back to the future, or no future?" on Monday and "Will Artificial Intelligence (AI) and Machine Learning (ML) take away my job as an RF/Analog Designer?" on Tuesday.

On behalf of the RFIC Steering and Executive Committees, we welcome you to join us at the 2019 RFIC Symposium in Boston, Massachusetts! Please visit the RFIC 2019 website **(http://rfic-ieee.org/)** for more details and updates.

CALL FOR PAPERS



CALL FOR PAPERS

IEEE Journal on Exploratory Solid-State Computational Devices and Circuits

Special Issue on "Ferroelectric Transistors for Advanced Logic, Analog, and Memory Applications"

Guest Editor
Azad Naeemi, Georgia Institute of Technology, azad@ece.gatech.edu

Editor-in-Chief
Ian Young, Intel, ian.young@intel.com

Aims and Scope
With recent advancements in the growth and processing of ferroelectric materials and the emergence of CMOS compatible ferroelectrics, major research and development efforts are underway on ferroelectric transistors for logic, analog, and memory applications. With CMOS scaling facing challenges in improving energy efficiency and power density, research in this area is needed to augment the CMOS technology by lowering the required supply voltage or adding new features and functionalities, such as non-volatility or reconfigurability. Ferroelectric transistors also show great promise for non-traditional circuits, such as convolutional and spiking neural networks and in-memory computing. Research in this area spans many levels of abstraction: from fundamental physical properties and material processing and characterization, to various device concepts, and to circuit and system design and benchmarking.

This special issue of the IEEE JXCDC will present the most recent developments in the area of ferroelectric transistors based on experiments and theoretical models. It aims to

feature original papers on various aspects of this emerging technology, its challenges and opportunities, its intrinsic versus practical limits, and the circuits and systems it may enable.

Topics of Interest include but are not limited to:

1. Advanced logic devices, such as negative capacitance transistors (NCFETs).
2. Memory devices, such as single- and multi-state ferroelectric transistors and ferroelectric tunnel junctions.
3. Analog devices, such as binary, multistate, or continuous synapses and oscillatory devices.
4. Ferroelectric switching coupled to other computing variables, such as ferromagnetic, anti-ferromagnetic, and strain.
5. Circuit- and system-level design and performance evaluation with ferroelectric devices.
6. Emerging circuit and system concepts, such as convolutional and spiking neural networks, coupled oscillators, in-memory computing, and instant-on circuits.

Important Dates:
Open for Submission: Feb 15th, 2019
Submission Deadline: April 30th, 2019
First Notification: May 15th, 2019
Revision Submission: June 15th, 2019
Final Decision: July 15th, 2019
Publication Online: August 1st, 2019

Submission Guidelines:
The IEEE Journal on Exploratory Solid-State Computational Devices and Circuits (J XCDC) IS AN OPEN ACCESS PUBLICATION: The Open Access Fee is: $1,350 USD per article.Article submissions must be done through the ScholarOne Manuscripts website: **https://mc.manuscriptcentral.com/jxcdc**.

Inquiries for the JxCDC Journal should be sent to: JXCDC@IEEE.ORG.

ESSCIRC/ESSDERC 2019: Call for Papers

European Solid-State Device Research Conference
European Solid-State Circuits Conference
September 23-26, 2019
Cracow, Poland

The aim of ESSDERC and ESSCIRC is to provide an annual European forum for the presentation and discussion of recent advances in solid-state devices and circuits. The level of integration for system-on-chip design is rapidly increasing. This is made available by advances in semiconductor technology. Therefore, more than ever before, a deeper interaction among technologists, device experts, IC designers and system designers is necessary. While keeping separate Technical Program Committees, ESSDERC and ESSCIRC are governed by a common Steering Committee and share Plenary Keynote Presentations and Joint Sessions bridging both communities. Attendees registered for either conference are encouraged to attend any of the scheduled parallel sessions, regardless to which conference they belong.

Although not limited, papers are solicited for the following main topics:

ESSCIRC

Analog

OP-Amps and instrumentation amplifiers; CT and DT filters; SC circuits, Comparators; Voltage and current references; High voltage circuits; Nonlinear analog circuits; Digitally assisted analog circuits.

Data Converters
Nyquist-rate and oversampling A/D and D/A converters; Sample-hold circuits; Time-to-digital converters; ADC and DAC calibration/error correction circuits.

RF and mm-Wave
RF/IF building blocks like LNAs, mixers, power amplifiers, IF amplifiers; Power detectors; Subsystems for RF, mm-wave and THz design.

Frequency Generation
Modulators/demodulators; VCOs; PLLs; DLLs; Frequency synthesizers; Frequency dividers; Integrated passive components.

Wireless and Wireline Systems
Receivers/transmitters/transceivers for wireless/wireline systems Gigabit serial links; Clock and data recovery; Equalization; Advanced modulation systems; Base station and handset applications; TV/radio/satellite receivers and transmitters; Radars.

Sensors, Imager and Biomedical
Sensor subsystems and interfaces; Accelerometers; Temperature sensing; Imaging and smart imaging chips; AMOLED; MEMs subsystems; RF MEMs; Implantable electronic ICs; Biomedical imagers; Bio-MEMs integrated systems; Lab-on-chip; Organic LED and liquid-crystal-display interface circuits; Flat panel and projection display.

Digital, Security and Memory
Techniques for energy efficient and high performance digital circuits; I/O and inter-chip communication; Reconfigurable digital circuits; Security and encryption circuits; Clocking; Arithmetic building blocks; Memories; Microprocessors; DSPs; Memory interfacing; Bus interfacing; Many core and multirate ICs; 3D integration.

Power Management
Energy transducers; Power regulators; DC-DC converters; Energy scavenging circuits; LDOs Boost-buck-converters; LED and gate drivers; Sequencers and supervisors; Green circuits.

ESSDERC

CMOS Devices and Technology
CMOS scaling; Novel MOS device architectures; Circuit/device interaction and co-optimization; High-mobility channel devices; CMOS front-end or back-end processes; Interconnects; Integration of RF or photonic devices; 3D integration; Front-end and back-end manufacturing processes; 3D integration and wafer-level packaging; Reliability and characterization of materials, processes and devices; Advanced interconnects; ESD, latch-up, soft errors, noise and mismatch behavior, hot carrier effects, bias temperature instabilities, and EMI; Defect monitoring and control; Metrology; Test structures and methodologies; Manufacturing yield modeling, analysis and testing.

Opto-, Power and Microwave Devices
New device or process architectures; New phenomena and performance improvement of optoelectronic, high voltage, smart power, IGBT, microwave devices; Passive devices, antennas and filters (including Si, Ge, SiC, GaN); Optoelectronic devices including sensors, LEDs, semiconductor lasers; Photovoltaic devices; Studies of high temperature operation; IC cooling and packaging aspects; Reliability and characterization of materials, processes and devices.

Physical Modeling of Materials and Devices
Numerical, analytical and statistical modeling and simulation of electronic, optical or hybrid devices, the interconnect, isolation and 2D or 3D integration; Aspects of materials, fabrication processes and devices, e.g. advanced physical phenomena (quantum mechanical and non-stationary transport phenomena, ballistic transport, and other related aspects); Mechanical or electro-thermal modeling and simulation; DfM. Reliability of materials and devices.

Compact Modeling of Devices and Circuits
Compact/SPICE modeling of electronic, optical, organic, and hybrid devices and their IC implementation and interconnection. Topics include compact/SPICE models and their Verilog-A standardization of the semiconductor devices (including Bio/Med sensors, MEMS, Microwave, RF, High voltage and Power), parameter extraction, compact models for emerging technologies

and novel devices, performance evaluation, reliability, variability, and open source benchmarking/implementation methodologies. Modeling of interactions between process, device, and circuit design as well as Foundry/Fabless Interface Strategies.

Memory Devices and Technology
Embedded and stand-alone memories; DRAM, FeRAM, MRAM, ReRAM, PCRAM, Flash, Nanocrystal and single/few-electron memories, Organic memories, NEMS-based devices, Selectors; Novel memory cell concepts and architectures, covering device physics, reliability, process integration and manufacturability issues and including 3D NAND Flash, crosspoint arrays, and 3D systems integration; Devices and concepts for neuromorphic computing, memory-enabled logic and security applications.

Emerging non-CMOS Devices and Technologies
Novel non-CMOS materials, processes and devices, (carbon nanotubes, nanowires and nanoparticles, 2D materials, graphene, metal oxides, etc.) for electronic, optoelectronic, sensor & actuator applications; Reliability and characterization of materials, processes and devices; Molecular and quantum devices; Nanophotonics, plasmonics, spintronics, selfassembling methods; Energy harvesters; High frequency digital and analog devices including THz; New high-mobility channels (strained Si, Ge, SiGe).

Sensor Devices and Technology
Design, fabrication, modeling, reliability, packaging and smart systems integration of actuators (discrete SoC, SiP, or heterogenous 3D integration); MEMS, NEMS, optical, chemical or biological sensors; Display technologies; High-speed imagers; TFTs; Organic and flexible substrate electronics.

POST-CONFERENCE PUBLICATIONS

All accepted ESSDERC and ESSCIRC papers will be included in the conference proceedings and posted on IEEE Xplore after the conference.

Co-publication of qualified papers in SSC-L
Upon acceptance, outstanding ESSCIRC papers will be invited to submit to a Special Issue of IEEE Solid-State Circuit Letters (SSC-L, 4 pages format) on the ESSCIRC, subject to additional editorial and quality reviews. Publication on IEEE Xplore of the SSC-L Special Issue is timed to be September 1, 2019

Special JSSC issue
Authors of outstanding papers will be invited to submit their work to a Special Issue of IEEE Journal of Solid-State Circuits (JSSC, up to 10-12 pages format) on the ESSCIRC to appear in July 2020, with an opportunity to provide additional material, such as mathematical analysis, in-depth circuit description, more experimental results and benchmarking data.

Special J-EDS issue
Authors of selected outstanding ESSDERC papers will be invited to submit their work to the special issue of IEEE Journal of the Electron Devices Society. The authors will be asked to revise the conference version of the paper by adding at least 30% new material. All manuscripts will undergo additional editorial and quality review process.

IMPORTANT INFORMATION
Manuscript guidelines as well as instructions on how to submit electronically will be available on the **conference website**. Papers must not exceed four A4 pages with all illustrations and references included.

Key Dates:

Paper submission Deadline: April 8th, 2019
Paper Selection Meeting: May 20th, 2019
Notification of Acceptance: May 31st, 2019
Early Registration Start: June 3rd, 2019

BioCAS 2019 : Call for Papers

Biomedical Circuits and Systems Conference
October 17 - 19, 2019
Nara, Japan

BioCAS 2019 is a premier international forum for presenting the interdisciplinary research and development activities at the crossroads of medicine, life sciences, physical sciences and engineering that shape tomorrow's medical devices and healthcare systems.

This conference brings together members of our communities to broaden their knowledge in emerging areas of research at the interface of the life sciences and the circuits and systems engineering. The three-day single-track program for BioCAS 2019 is multidisciplinary in topics including but not limited to:

Biomedical Technologies:
* Assistive, Rehabilitation, and Quality of Life Technologies
* Biofeedback, Neuromodulation, and Closed-Loop Systems
* Bio-Inspired and Neuromorphic Circuits and Systems
* Biosensor Devices and Interface Circuits
* Biotelemetry and Energy Harvesting/Scavenging Circuits and Systems
* Body Area/Sensor Network and Wireless/Wearable Health Monitoring
* Electronics for Neuroscience
* Implantable Medical Electronics
* Lab-on-Chip and BioMEMS
* Point-of-Care Technologies for Healthcare

Biomedical Applications:
* Biomedical Imaging and Image Processing
* Biosignal Recording, Processing, and Machine Learning
* Human-Machine Interfaces
* Medical Information Systems and Bioinformatics

Submission Guidelines:
The complete 4-page paper (in standard IEEE double-column format), including the title, authors' names, affiliations and e-mail addresses, as well as a short abstract and an optional demonstration video link (3 minute max) are requested. Papers must be submitted electronically in PDF format through **www.biocas2019.org.**

Important Dates:
Monday, April 22, 2019 - Special Session Proposal Deadline
Monday, June 10, 2019 - Regular Paper Submission Deadline
Monday, July 15, 2019 - Live Demo Submission Deadline
Monday, August 12, 2019 - Author Notification Date
Sunday, September 15, 2019 - Final Paper Submission Deadline

IEEE NEWS

Powered by IEEE TRYEngineering Summer Institute

Register for Summer 2019: TryEngineering Summer Institute

Want to provide the future engineer in your life with an unforgettable summer experience? Look no further than IEEE's TryEngineering Summer Institute.

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across the United States, the TryEngineering Summer Institute unites students aged 12-17 years old from around the world to:

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- discover not just what's happening today, but what's coming tomorrow, through conversations with renowned guest speakers and incredible TryEngineering Summer Institute counselors

Give us two weeks, and we'll give you a new definition of what it means to be an engineer.

Our 2019 sites are:

- Texas A&M University
- University of California, Riverside
- Vaughn College of Engineering (New York)

All sites will run concurrently both Introductory and Advanced-level programs, for the duration of two weeks, for two sessions. The curriculum for Session 1 mirrors the curriculum for Session 2, but students who choose to attend both will have the opportunity to explore the content in new ways.

Session 1: 7 - 20 July 2019
Session 2: 21 July - 3 August 2019

To register and for more information, please click here!

Seeking News

Please send any chapter news or happenings (Distinguished Lecturer visits, events hosted by your SSCS chapter, awards received by members, etc) to Abira Altvater, SSCS Magazine News Editor, for inclusion in an upcoming issue of the magazine. Please email - **Abira.Altvater@ieee.org**. We look forward to receiving your news articles!

For more chapter news, check out the Winter 2019 issue of the Solid-State Circuits Magazine.