IEEE SOLID-STATE CIRCUITS SOCIETY

Where ICs are in IEEE

June 2019

UPCOMING SSCS WEBINARS

Faster, Higher, Stronger - Efficient Energy Conversion with GaN

Presenter: Dr. Bernhard Wicht, Leibniz University, Hannover, Germany

Tuesday, July 9, 2019 at 12:00 PM ET

Abstract: Efficient conversion of energy is one of the megatrends, enabled by advanced semiconductors and microelectronics. As a wide-band gap material, GaN (gallium nitride) offers a huge potential to reduce the overall power electronics system size and cost. GaN technology is faster, smaller, more efficient than silicon power MOSFETs. Dedicated control circuits enable to leverage the potential of GaN power switches with a minimum of parasitic effects. This webinar gives an introduction into circuit and system design aspects related to GaN power transistors with a particular focus on gate drivers. Small solutions are achieved by increasing the switching frequency as it scales down passive components. The concept of high-voltage charge and energy storing enables highly integrated gate driver designs with a minimum of external components. Multi-level gate drivers increase the robustness under extremely fast switching transitions up to 500V/ns. Concepts for common-mode transient immunity (CMTI) are discussed.

Bio: Bernhard Wicht has 20+ years of experience in analog and smart power IC design. He received the Dipl. Ing. degree in electrical engineering from University of Technology Dresden, Germany, in 1996 and the Ph.D. degree from University of Technology Munich, Germany, in 2002. Between 2003 and 2010, he was with Texas Instruments, Freising, responsible for the design of automotive power management ICs. In September 2010, he became a full professor for integrated circuit design and a member of the Robert Bosch Center for Power Electronics at Reutlingen University, Germany. Since April 2017, he has been heading the Chair for Mixed-Signal IC Design at Leibniz University Hannover, Germany. His research interest includes IC design with focus on power management, gate drivers and high-voltage. Dr. Wicht was co-recipient of the 2015 ESSCIRC Best Paper Award. He invented seventeen patents with several more pending. In 2018, he received the faculty award for excellent teaching at his university. He currently serves as a member of the Technical Program Committees of ESSCIRC and ISSCC.

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REGISTER

1+1=3:The Power of Groups: From Tiny Chips to Space Super-Structures

Presenter: Prof. Ali Hajimiri, California Institute of Technology, California, USA

Tuesday, July 16, 2019 at 4:00 PM ET

Abstract: Many of today's technological marvels have emerged from putting apparently unrelated ideas together and creating something more than the sum of the parts. Silicon integrated chips have come a long way from the days of first transistors. Nowadays, we can place billions of transistors operating at extremely high frequencies on a single chip as well as optical component. This offers a plethora of new opportunities that prior silicon chips could not address. In this talk, I will discuss a holistic design approach to integrated circuits leading to yet further proliferation of such technologies into our daily lives. We will discuss some of its exciting results, including low-cost tera-hertz imagers, nano-photonic coherent cameras capable of forming 3D images, optical phased arrays, space-based solar power transfer, self-healing circuits that repair themselves, and medical diagnostic and therapeutic devices solutions based on electromagnetic sensing and manipulation.

Bio: Professor Hajimiri's group does research on electronics and photonics integrated circuits and their applications in various disciplines, including high-frequency and high-speed communications, sensing, imaging, and bio-sensing. His research group engages in both the theoretical analysis of the problems in integrated circuits as well as practical implementations of new systems.

Prof. Ali Hajimiri received his B.S. degree in Electronics Engineering from the Sharif University of Technology, and M.S. and Ph.D. degrees in electrical engineering from the Stanford University.

Before joining the Faculty of Caltech, he worked at Philips Semiconductors, where he worked on a BiCMOS chipset for GSM and cellular units, at Sun Microsystems working on the UltraSPARC microprocessor's cache RAM design methodology, and with Lucent Technologies (Bell Labs), Murray Hill, NJ, where he investigated low-phase-noise integrated oscillators. In 1998, he joined the Faculty of the California Institute of Technology, Pasadena, where he is Bren Professor of Electrical Engineering and Medical Engineering, Director of Caltech Holistic Integrated Circuit Laboratory, and co-Director of the Space-based Solar Power Project. His research interests are high-speed and high-frequency electronics and photonics integrated circuits for applications in sensors, biomedical devices, photonics, and communication systems.

Prof. Hajimiri is the author of The Design of Low Noise Oscillators (Boston, MA: Springer) and has authored and coauthored close to 200 refereed journal and conference technical articles. He has been granted more than 90 U.S. patents and has many more pending applications. He has served on the Technical Program Committee of the International Solid-State Circuits Conference (ISSCC), as an Associate Editor of the IEEE Journal of Solid-State Circuits (JSSC), as an Associate Editor of IEEE Transactions on Circuits and Systems (TCAS): Part-II, a member of the Technical Program Committees of the International Conf erence on Computer Aided Design (ICCAD), Guest Editor of the IEEE Transactions on Microwave Theory and Techniques, and Guest Editorial Board of Transactions of Institute of Electronics, Information and Communication Engineers of Japan (IEICE).

He is a Fellow of National Academy of Inventors (NAI). Prof. Hajimiri was selected to the TR35 top innovator's list. He is also a Fellow of IEEE and has served as a Distinguished Lecturer of the IEEE Solid-State and Microwave Societies. He is the recipient of Caltech's Graduate Students Council Teaching and Mentoring award as well as the Associated Students of Caltech Undergraduate Excellence in Teaching Award. He was the Gold medal winner of the National Physics Competition and the Bronze Medal winner of the 21st International Physics Olympiad, Groningen, Netherlands. He was a co-recipient of the IEEE Journal of Solid-State Circuits Best Paper Award of 2004, the International Solid-State Circuits Conference (ISSCC) Jack Kilby

Outstanding Paper Award, a co-recipient of RFIC best paper award, a two-time co-recipient of CICC best paper award, and a three-time winner of the IBM faculty partnership award as well as National Science Foundation CAREER award and Okawa Foundation award. In 2002, he co-founded Axiom Microdevices Inc., whose fully-integrated CMOS PA has shipped more than 250,000,000 units, and was acquired by Skyworks Inc. in 2009.

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NEWS

CALL FOR PAPERS

IEEE Journal on Exploratory Solid-State Computational Devices and Circuits

Special Topic on "Spin-Orbit Coupling Effects for Advanced Logic and Memory"

Guest Editor:
Dmitri Nikonov, Intel Corporation, dmitri.e.nikonov@intel.com

Editor-in-Chief:
Azad Naeemi, Georgia Institute of Technology, azad@ece.gatech.edu

Aims and Scope:
In the past few years, fascinating progress was made in the science of spin-orbit coupling effects; and fundamental research in this field is continuing vigorously. On the other hand, information technology is facing a crisis of increasing power dissipation as computing devices are being scaled to ever smaller dimensions according to the Moore's law. Every promising solid-state technology is being tried as the possible solution for this crisis. The time has come for spin-orbit physics to make an impact on practical computing applications.

For this to happen, challenges such as the following must be addressed:

Is spin-orbit torque memory competitive with spin-transfer torque memory?
Can logic circuits with spin-orbit be demonstrated?
What is the unique advantage of spin-orbit devices for non-traditional computing?

The editors will favor papers answering these questions.

This special topic of the IEEE JXCDC will present original recent research involving spin-orbit coupling effects and span at least two levels of hierarchies like:
materials - devices - circuits - computing architectures; or
design - fabrication - measurement - simulation.

Topics of Interest include but are not limited to:
1. Spin-orbit torque memory development.
2. Spin-orbit logic devices - proposals and demonstrations.
3. Spin-orbit and orbit-spin conversion in logic devices.
4. Processional spin-orbit switching.
5. Electric control of spin-orbit coupling.
6. Coupling of strain with spin-orbit effects.
7. Thermal effect in spin-orbit devices.
8. Unidirectional spin Hall magnetoresistance effect.
9. Circuits for spin-orbit logic.
10. Spin-orbit devices for analog, probabilistic, and neuromorphic computing.
11. Spin-orbit effects for spin waves.

12. Spin-orbit applications to anti-ferromagnets.

Review papers on the topic are also welcome.

Important Dates:
Open for Submission: June 15th, 2019
Submission Deadline: August 31st, 2019
First Notification: September 15th, 2019
Revision Submission: October 15, 2019
Final Decision: November 15th, 2019
Publication Online: December 1st, 2019

Submission Guidelines:
The IEEE Journal on Exploratory Solid-State Computational Devices and Circuits (JXCDC) IS AN OPEN ACCESS PUBLICATION.

The Open Access Fee is: $1,350 USD per article. Article submissions must be done through the ScholarOne Manuscripts website: https://mc.manuscriptcentral.com/jxcdc.
Guidelines for papers and supplementary materials, as well as a paper template, are provided at this website.

Additional Information can be found here: **https://sscs.ieee.org/publications/ieee-journal-on-exploratory-solid-state-computational-devices-and-circuits-jcdc**

Inquiries for the JxCDC Journal should be sent to: JXCDC@IEEE.ORG.

JxCDC is sponsored by:
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Electron Devices Society
Council on Superconductivity

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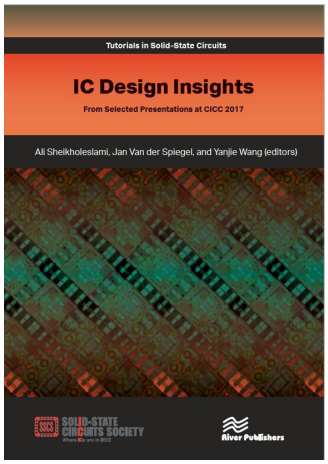
FEATURED SSCS MEMBER BENEFITS

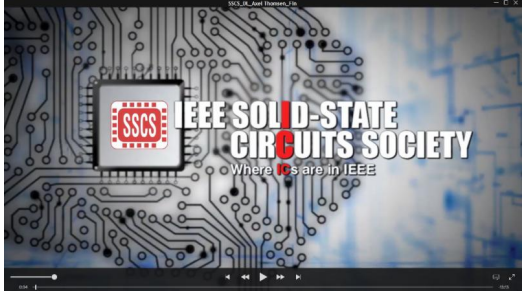


IC Design Insights eBook

Now available for download on the SSCS Resource Center!

Click here to download!

This book contains a selection of tutorial and invited presentations that were given at the IEEE CICC 2017 in Austin, TX. The selection of the talks was made to provide a comprehensive coverage of key topics, including Circuits Techniques for mm-wave front-ends, RF and mm-wave receivers and frequency synthesis, data and DC-DC converters, and techniques for IoT security. The book is part of an educational initiative of the IEEE Solid-State Circuits Society to offer its members state of the art educational material.



SSCS YouTube Channel

SSCS now has a **YouTube Channel** where all CONFedu videos are posted including VLSIx 2016, CICCx 2017, ISSCCedu 2018, and ESSCIRCedu 2018. **Coming Soon:** CICCedu 2019, and VLSIedu 2019!

New Episodes - SSCS Chip Chat Podcast

SCS' educational programming has expanded to include a podcast called SSCS Chip Chat. This interview style podcast focuses on the stories of engineers and scientists behind the integrated circuits that power the world.

The podcast can be listened to by searching SSCS Chip Chat in the Apple Podcast App or whatever podcast app you use for your mobile device.

You can also listen to the podcast online. **Click here to listen!**

Episode 1: Dr. Gert Cauwenberghs
Episode 2: Albert Theuwissen
Episode 3: Shanthi Pavan
Episode 4: R. Jacob Baker
Episode 5: Shantanu Chakrabartty
Episode 6: Alice Wang - **NEW**

PUBLICATIONS

The latest in SSCS Flagship Publications...

IEEE Journal of Solid-State Circuits

Vol. 54, Issue 6, June 2019

A 1.5-1.9-GHz All-Digital Tri-Phasing Transmitter With an Integrated Multilevel Class-D Power Amplifier Achieving 100-MHz RF Bandwidth
Jerry Lemberg ; Mikko Martelius ; Enrico Roverato ; Yury Antonov ; Tero Nieminen ; Kari Stadius

Wide-Band RF Front End for SAW-Less Receivers Employing Active Feedback and

Far Out-of-Band Blocker Rejection Circuit
Amirhossein Rasekh ; Mehrdad Sharif Bakhtiar

A CMOS MedRadio Transceiver With Supply-Modulated Power Saving Technique for an Implantable Brain-Machine Interface System
Mao-Cheng Lee ; Alireza Karimi-Bidhendi ; Omid Malekzadeh-Arasteh ; Po T. Wang ; An H. Do ; Zoran Nenadic ; Payam Heydari

A Multi-Loop-Controlled AC-Coupling Supply Modulator With a Mode-Switching CMOS PA in an EER System With Envelope Shaping
Xun Liu ; Heng Zhang ; Philip K. T. Mok ; Howard C. Luong

A Low-Jitter Injection-Locked Multi-Frequency Generator Using Digitally Controlled Oscillators and Time-Interleaved Calibration
Heein Yoon ; Suneui Park ; Jaehyouk Choi

A Compact Dual-Band Digital Polar Doherty Power Amplifier Using Parallel-Combining Transformer
Yun Yin ; Liang Xiong ; Yiting Zhu ; Bowen Chen ; Hao Min ; Hongtao Xu

A 28-/37-/39-GHz Linear Doherty Power Amplifier in Silicon for 5G Applications
Song Hu ; Fei Wang ; Hua Wang

A Millimeter-Wave CMOS Transceiver With Digitally Pre-Distorted PAM-4 Modulation for Contactless Communications
Yanghyo Kim ; Boyu Hu ; Yuan Du ; Wei-Han Cho ; Rulin Huang ; Adrian Tang ; Huan-Neng Chen ; Chewnpu Jou ; Jason Cong ; Tatsuo Itoh ; Mau-Chung Frank Chang

A 230-260-GHz Wideband and High-Gain Amplifier in 65-nm CMOS Based on Dual-Peak Gmax -Core
Dae-Woong Park ; Dzuhri Radityo Utomo ; Bao Huu Lam ; Sang-Gug Lee ; Jong-Phil Hong

A Calibration-Free 12-bit 50-MS/s Full-Analog SAR ADC With Feedback Zero-Crossing Detectors
Kwuang-Han Chang ; Chih-Cheng Hsieh

A Second-Order Noise-Shaping SAR ADC With Passive Integrator and Tri-Level Voting
Haoyu Zhuang ; Wenjuan Guo ; Jiaxin Liu ; He Tang ; Zhangming Zhu ; Long Chen ; Nan Sun

A 0.4-V 13-bit 270-kS/s SAR-ISDM ADC With Opamp-Less Time-Domain Integrator
Sung-En Hsieh ; Chih-Cheng Hsieh

Reference-Less Time-Division Duplex Transceiver IC for a Renal Denervation System
Jaehyeok Yang ; Seohyeon Kim ; Gunpil Hwang ; Kyeongha Kwon ; Sejun Jeon ; Hyeon-Min Bae

A Low-Power Bidirectional Link With a Direct Data-Sequencing Blind Oversampling CDR
Sudip Shekhar ; Rajesh Inti ; James Jaussi ; Tzu-Chien Hsueh ; Bryan K. Casper

A 25-Gb/s Avalanche Photodetector-Based Burst-Mode Optical Receiver With 2.24-ns Reconfiguration Time in 28-nm CMOS
Kuan Chang Chen ; Azita Emami

A Mutual Capacitance Touch Readout IC With 64% Reduced-Power Adiabatic Driving Over Heavily Coupled Touch Screen
Jiheon Park ; Young-Ha Hwang ; Jonghyun Oh ; Yoonho Song ; Jun-Eun Park ; Deog-Kyoon Jeong

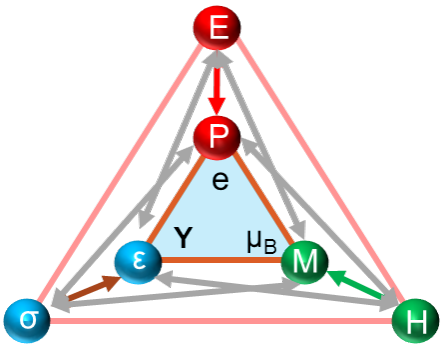
A CMOS SPAD Line Sensor With Per-Pixel Histogramming TDC for Time-Resolved Multispectral Imaging
Ahmet T. Erdogan ; Richard Walker ; Neil Finlayson ; Nikola Krstajić ; Gareth Williams ; John Girkin ; Robert Henderson

A 14-nA, Highly Efficient Triple-Output Thermoelectric Energy Harvesting System Based on a Reconfigurable TEG Array
Qiping Wan ; Philip K. T. Mok

A Fully Integrated Split-Electrode SSHC Rectifier for Piezoelectric Energy Harvesting
Sijun Du ; Yu Jia ; Chun Zhao ; Gehan A. J. Amaratunga ; Ashwin A. Seshia

A 13.56 MHz, 94.1% Peak Efficiency CMOS Active Rectifier With Adaptive Delay Time Control for Wireless Power Transmission Systems Zhongming Xue ; Shiquan Fan ; Dan Li ; Lina Zhang ; Wei Gou ; Li Geng
A 25-MHz Four-Phase SAW Hysteretic Control DC-DC Converter With 1-Cycle Active Phase Count Bumkil Lee ; Min Kyu Song ; Ashis Maity ; D. Brian Ma
Design of an Always-On Deep Neural Network-Based 1- u W Voice Activity Detector Aided With a Customized Software Model for Analog Feature Extraction Minhao Yang ; Chung-Heng Yeh ; Yiyin Zhou ; Joao P. Cerqueira ; Aurel A. Lazar ; Mingoo Seok
A 3-D IC for Mitigating Energy of Memory Accessing and Data Movement in Accelerator- Based Streaming Architectures Lung-Yen Chen ; Sen Tao ; Naveen Verma
A 64-Tile 2.4-Mb In-Memory-Computing CNN Accelerator Employing Charge-Domain Compute Hossein Valavi ; Peter J. Ramadge ; Eric Nestler ; Naveen Verma
3-D NAND Flash Value-Aware SSD: Error-Tolerant SSD Without ECCs for Image Recognition Yoshiaki Deguchi ; Toshiki Nakamura ; Atsuna Hayakawa ; Ken Takeuchi
A Reference-Free Temperature-Dependency-Compensating Readout Scheme for Phase-Change Memory Using Flash-ADC-Configured Sense Amplifiers Dong-Hwan Jin ; Ji-Wook Kwon ; Min-Jae Seo ; Mi-Young Kim ; Min-Chul Shin ; Seok-Joon Kang ; Jung-Hyuk Yoon ; Taek-Seung Kim ; Seung-Tak Ryu

IEEE Journal on Exploratory Solid-State Computational Devices and Circuits



Issue 1, Part 2 - June 2019

Boosted Spin Channel Networks for Energy-efficient Inference Ameya D. Patil ; Sasikanth Manipatruni ; Dmitri E. Nikonov ; Ian A. Young ; Naresh R. Shanbhag
Using Floating Gate Memory to Train Ideal Accuracy Neural Networks Sapan Agarwal ; Diana Garland ; John Niroula ; Robin B. Jacobs-Gedrim ; Alex Hsia ; Michael S. Van Heukel
Unsupervised learning to overcome catastrophic forgetting in neural networks Irene Muñoz-Martín ; Stefano Bianchi ; Giacomo Pedretti ; Octavian Melnic ; Stefano Ambrogio ; Daniele Ielmini
Performance Estimate of Inverse Rashba-Edelstein Magnetoelectric Devices for Neuromorphic Computing Andrew W. Stephan ; Jiaxi Hu ; Steven J. Koester
Graded-Anisotropy-Induced Magnetic Domain Wall Drift for an Artificial Spintronic Leaky Integrate-and-Fire Neuron Wesley H. Brigner ; Xuan Hu ; Naimul Hassan ; Christopher H. Bennett ; Jean Anne C. Incorvia ; Felipe Garcia-Sanchez ; Joseph S. Friedman
Subthreshold Spintronic Stochastic Spiking Neural Networks with Probabilistic Hebbian Plasticity and Homeostasis Steven D. Pyle ; Ramtin Zand ; Shadi Sheikhfaal ; Ronald F. DeMara

JxCDC papers listed in order of popularity can be found online HERE.

For paper submission details, click HERE.

IEEE Solid-State Circuits Letters

Issue 5, May 2019

A Ka-Band Compact Active Switch With Broadband Amplifiers for Phased-Array Transceiver in 65-nm CMOS Mengru Yang ; Bingyang Wu ; Dixian Zhao
A 6.5 x 7um2 0.98-to-1.5 mW Nonself-Oscillation-Mode Frequency Divider-by-2 Achieving a Single-Band Untuned Locking Range of 166.6% (4-44 GHz) Yong Chen ; Zunsong Yang ; Xiaoteng Zhao ; Yunbo Huang ; Pui-In Mak ; Rui P. Martins

EDUCATION

August 2019 Distinguished Lectures

There are no scheduled SSCS DL talks in July 2019

SSCS Taipei	Injecting Digital into Power Electronics: Programmable Digital Gate Driver IC for Power Transistors - Presented by Makoto Takamiya	August 6, 2019	NCTU, Hsinchu, Taiwan **For more information, please click here**
SSCS Tainan	Integrated Power Management Circuits for Energy-Efficient IoT Systems - Presented by Makoto Takamiya	August 8, 2019	EDA Royal Hotel, Kaohsiung City, Taiwan **For more information, please click here**

CONFERENCES

Upcoming 2019 SSCS-Sponsored Conferences

2019 IEEE Hot Chips 31 Symposium (HCS) Cupertino, California	**August 18 - 20, 2019**
ESSCIRC/ESSDERC 2019 - IEEE 45th European Solid-State Circuits Conference (ESSCIRC)/49th European Solid-State Device Research Conference Cracow, Poland	**September 23 - 26, 2019**
2019 IEEE Biomedical Circuits and Systems Conference (BioCAS) Nara, Japan	**October 17 - 19, 2019**

2019 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS) Nashville, Tennessee	**November 3 - 6, 2019**
2019 IEEE Asian Solid-State Circuits Conference (A-SSCC) Macau, China	**November 4 - 6, 2019**

CALL FOR PAPERS

ISSCC 2020: Call for Papers

IEEE International Solid-State Circuits Conference

February 16 - 20, 2020

San Francisco, California

www.isscc.org

ISSCC 2020 Conference There: Integrated Circuits Powering the AI Era"

The steady advancement of solid-state circuits has led to technological betterment in our daily living, demonstrated by exploding applications ranging from medical, wearable and mobile electronics to IoT, virtual reality, autonomous driving and robotics. While the widespread excitement resides in the applications where end-users touch and feel, the systems are enabled by integrated circuits engines that are woven into this technological fabric of our lives. Galvanized by this reality, the solid-state circuits community is driven to enhance the platform that continues to evolve. With much enthusiasm and anticipation, and even uncertainty, we look onward to this emerging AI era. Consequently, ISSCC 2020 seeks contributions that will continue to enhance and reshape the future.

Innovative and original papers are solicited in subject areas including (but not limited to) the following:

ANALOG: Amplifiers, comparators, oscillators, filters, references; nonlinear analog circuits; digitally-assisted analog circuits; MEMS/sensor interface circuits.
DATA CONVERTERS: Nyquist-rate and oversampling A/D and D/A converters; embedded and application-specific A/D and D/A converters; analog to information conversion; time-to-digital converters.
DIGITAL CIRCUITS and ARCHITECTURES & SYSTEMS: Digital circuits, building blocks, and complete systems for microprocessors, micro-controllers, application processors, graphics processors; digital systems for communications, video and multimedia, cryptography, smart cards, security and trusted computing, accelerators, reconfigurable systems, near- and sub-threshold systems, emerging applications. Digital circuits for intra-chip communication, clock distribution, soft-error and variation-tolerant design, power management (i.e. voltage regulators, adaptive digital circuits, digital sensors), PLLs for digital clocking applications, and security circuits (i.e. PUFs, TRNG, side-channel attack countermeasures, and attack-detection sensors).
IMAGERS, MEMS, MEDICAL, & DISPLAY: Image sensors and SoCs; automotive, LIDAR, and ultrasonic sensors; MEMS sensor systems; wearable, implantable, ingestible electronics, biomedical SoCs, neural interfaces and closed-loop systems; biosensors, microarrays, and lab-on-a-chip; display electronics, displays with sensing functionality; sensing for AR/VR.
MACHINE LEARNING and AI: Chips demonstrating system, architecture and circuit innovations for machine learning and artificial intelligence: processor architectures, accelerators and digital circuits; mixed-signal, analog, near-sensor and in-sensor processing schemes; architectures leveraging near-memory and in-memory computation, using volatile or non-volatile memories.
MEMORY: Static, dynamic, and non-volatile memories for stand-alone and embedded applications; memory/SSD controllers; high-bandwidth I/O interfaces; memories based on phase-change, magnetic, spin-transfer-torque, ferroelectric, and resistive materials; array architectures and circuits to improve low-voltage operation, power reduction, reliability, and fault tolerance; application-specific circuit enhancements within the memory subsystem, including in-memory logic functions and compute.
POWER MANAGEMENT: Power management and control circuits, regulators; switched-mode power converter ICs using inductive, capacitive, and hybrid techniques; energy harvesting circuits and systems; wide-bandgap topologies and gate-drivers; power and signal isolators; robust power management circuits for automotive and other harsh environments; circuits for lighting,

wireless power and envelope modulators.
RF CIRCUITS and WIRELESS SYSTEMS: Building blocks and complete solutions at RF, mm-Wave and THz frequencies for receivers, transmitters, frequency synthesizers, transceivers, SoCs, and SiPs. Innovative circuit-level and system-architecture solutions for established wireless standards and future systems or applications such as radar, sensing, and imaging.
TECHNOLOGY DIRECTIONS: Emerging IC and system solutions for: biomedical, sensor interfaces, analog signal processing, power management, computation (including non-CMOS machine learning), data storage, and communication; non-silicon-, carbon-, organic-, metal-oxide-, compound-semiconductor- and new-device-based circuits; nano, flexible, large-area, stretchable, printable, spintronics, quantum, optical, integrated photonics, and 3D-integrated electronics.
WIRELINE: Receivers/transmitters/transceivers for wireline systems, including backplane transceivers, optical links, chip-to-chip communications, 2.5/3D interconnect, copper-cable links, and equalizing on-chip links; exploratory I/O circuits for advancing data rates, power efficiency, equalization, robustness, adaptation capability, and design methodology; building blocks for wireline transceivers (such as AGCs, analog and ADC/DAC-based front ends, equalizers, clock generation and distribution circuits including PLLs, line drivers, and hybrids).

Deadline for Paper Submission: Monday, September 9, 2019, 3:00 PM Eastern Daylight Time

The ISSCC 2020 Paper Submission Site Opens July 1st!

Click here for more information

SSCS-Sponsored Conferences: Proceedings

Click the links below to access the latest SSCS-Sponsored conference proceedings.

2018
2018 IEEE International Solid-State Circuits Conference (ISSCC)
2018 IEEE Custom Integrated Circuits Conference (CICC)
2018 IEEE Symposium on VLSI Circuits (VLSI)
2018 IEEE 44th European Solid-State Circuits Conference (ESSCIRC)
2018 IEEE Asian Solid-State Circuits Conference (A-SSCC)

2019
2019 IEEE International Solid-State Circuits Conference (ISSCC)

Hot Chips: A Symposium on High Performance Chips
8 - 20 August, 2019
Stanford University Campus, California

Since it started in 1989, HOT CHIPS has been known as one of the semiconductor industry's leading conferences on high-performance microprocessors and related integrated circuits. The conference is held once a year in August in the center of the world's capital of electronics activity, Silicon Valley.

Program At-A-Glance

Sunday, 8/18/2019: Tutorials

- Morning Tutorials: Acceleration in the Cloud

- Morning Tutorials: Acceleration in the Cloud
- The Nitro Project - Next Generation AWS Infrastructure
- Microsoft Azure
- TPU V3 in Google Cloud: Architecture and Infrastructure
- Afternoon Tutorial: RISC-V
- Reception

Monday, 8/19/2019: Conference Day 1

- Opening Remarks
- General Purpose Compute
- Memory
- Keynote 1: "Delivering the Future of High-Performance Computing with System, Software and Silicon Co-Optimization" by Dr. Lisa Su, CEO, AMD
- Methodology and ML Systems
- ML Training
- Reception

Tuesday, 8/20/2019: Conference Day 2

- Embedded and Auto
- ML Inference
- Keynote 2: "What Will the Next Node Offer Us?" by Dr. Philip Wong, VP Corporate Research, TSMC
- Interconnects
- Break
- Packaging and Security
- Graphics and AR
- Closing Remarks

Click here to register!

For Society news and happenings, check out the Spring 2019 issue of the Solid-State Circuits Magazine.
