IEEE SOLID-STATE CIRCUITS SOCIETY

Where ICs are in IEEE

July 2019

UPCOMING SSCS WEBINAR

RF Harmonic Oscillators Integrated in Silicon Technologies

Presenter: Prof. Pietro Andreani
Thursday, August 29, 2019 at 11:00 AM ET

Abstract: As one of the truly fundamental analog functions in any wireless/wireline application, the voltage-controlled oscillator keeps attracting a great deal of well-deserved attention. In this presentation, we will investigate the mechanisms of phase noise generation in harmonic oscillators, including some recently published general results, after which we will analyze both classical and emergent oscillator architectures, describing pros and cons for each. Various techniques to achieve a very wide oscillator tuning range will be illustrated as well.

Bio: Pietro Andreani received the M.S.E.E. degree from the University of Pisa, Italy, in 1988, and the Ph.D. degree from Lund University, Sweden, in 1999. Between 2001 and 2007 he was chair professor at the Center for Physical Electronics, Technical University of Denmark. From 2005 to 2014 he had a 20% position as analog/RF designer at Ericsson AB in Lund, Sweden. Since 2007, he has been associate professor at the dept. of Electrical and Information Technology (EIT), Lund University, working in analog/mixed-mode/RF IC design. He has also been the head of the VINNOVA Center for System Design on Silicon, hosted by EIT, between 2014 and 2016. He has been a TPC member of ISSCC (2007-2012), is a TPC member of ESSCIRC (chair of the Frequency Generation subcommittee since 2012, TPC chair in 2014) and RFIC, and Associate Editor of JSSC. He has been an IEEE SSCS Distinguished Lecturer since 2017. He has authored numerous papers on

harmonic oscillators and phase noise, for which he was elevated to IEEE Fellow in 2018.

CLICK HERE TO REGISTER

NEWS

NEW - SSCS Open Access Journal

The IEEE Solid-State Circuits Society (SSCS) is launching a new gold fully open access journal, IEEE Open Journal of Solid-State Circuits, spanning the full scope of the SSCS' fields of interest. The new journal, which will be fully compliant with funder mandates, including Plan S, will begin accepting submissions in fall 2019 and publish its first articles in early 2020.

An Independent editorial board will drive SSCS' commitment to publish high-quality articles including cutting-edge studies and breakthroughs in integrated circuits. The new journal will follow IEEE's established high standard of peer review, drawing on experts in the field to continue to publish the most highly cited content in field of interests.

The journal will be led by Jan Craninckx, imec, Leuven, Belgium.

For more information, please visit **open.ieee.org** or complete the **form** to receive an email when the journal will begin accepting submissions.

SSCS Contests for Students

Calling all students! SSCS is pleased to announce the launch of two contests open to undergraduate and graduate students. Prizes are valued up to $2K.

CIRCUITS VIDEO CONTEST
Create a fun short (5-10 minute) video that explains circuits for high school students. Tell a story about a circuits concept. Videos should motivate a real-world application of circuits. Undergraduate and graduate students who are currently enrolled in a college or university may enter. Win up to $2K towards entering an SSCS-sponsored conference. **Click here for more information** on contest eligibility, how to enter, and more. **Submission Deadline: December 15, 2019**

2019 STUDENT CIRCUITS CONTEST
This contest involves solving a thought-provoking circuit analysis and design problem. Submissions are solicited by undergraduate and graduate students who are currently enrolled in a college or university. Win up tp $2K towards entering an SSCS-sponsored conference. **Click here for more information** on contest eligibility, how to enter, and more. **Submission Deadline: September 15, 2019**

NEW! Get your SSCS Membership Certificate

Steps to download and print your certificate

1). **Log into Collabratec**
2). Click your name in the top right of the screen and select "Member Certificates" from the drop-down menu
3). From the "Member Certificates" page, click on the "Download PDF" link to the right of "IEEE Solid-State Circuits Society Membership"
4). Open the PDF and print it

Machine Learning and AI Track at ISSCC

The ISSCC (International Solid State Circuits Conference) is the venue where the world's prime silicon implementations are published. This conference takes place yearly in February, located in the heart of Silicon Valley, San Francisco.

ISSCC now added an additional track to its conference focusing entirely on Machine Learning and AI. ISSCC ambitions to attract cutting edge AI chips, to innovate across the complete technology-circuit-architecture design space. To this end, a new dedicated conference subcommittee groups experts from all areas of machine learning, across different design levels.

With this email, we invite you to submit a paper on your next AI chip to ISSCC. Papers can be submitted here before September 9th, 2019. For more information, please consult the **ISSCC website** and **call for papers**.

UPCOMING SSCS-SPONSORED EVENTS

Save the date for these upcoming Society-sponsored events.

The IEEE Solid-State Circuits Society will be sponsoring two exciting events at ESSCIRC/ESSDERC 2019. ESSCIRC/ESSDERC is an annual European forum for the presentation and discussion of recent advances in solid-state devices and circuits. **The conference will be held in Krakow, Poland, September 23-26, 2019 at the Conference Center of the Jagiellonian University.**

For more information about the conference, **please click here**.

SSCS Diversity Luncheon: Cultivating Engineering Confidence
Tuesday, September 24, 2019
12:40 - 2:00 PM
Bistro Room, Level 0

Pick up your lunch from the cafeteria and bring it to the room. Drinks, coffee, and dessert will be provided.

The luncheon will feature talks by industry and academic professionals sharing their experiences in their careers where a challenge, project, or a mentor helped them become a better engineer and problem solver. There will be a group discussion about mentoring.

Tickets for this event will be distributed on a first come, first serve basis. Pick up your ticket at the ESSCIRC/ESSDERC registration desk. This event is open to everyone of all ages and genders.

Young Professionals and Students Micro-Mentoring and Career Coaching Session
Monday, September 23, 2019
6:30 PM - 8:30 PM
Exhibition Room

Complimentary event with light refreshments for all students, faculty, and engineers within 15 years of their first degree. Leading experts from industry and academia, IEEE SSCS executives, and Distinguished Lecturers will share their experiences. One-on-one answers to all your questions on publications, entrepreneurship, industry vs. academia and career coaching.

Click here to register for the event. **On-site registration is also available.**

PUBLICATIONS

CALL FOR PAPERS

IEEE Journal on Exploratory Solid-State Computational Devices and Circuits

Special Topic on "Spin-Orbit Coupling Effects for Advanced Logic and Memory"

Guest Editor:
Dmitri Nikonov, Intel Corporation, dmitri.e.nikonov@intel.com

Editor-in-Chief:
Azad Naeemi, Georgia Institute of Technology, azad@ece.gatech.edu

Aims and Scope:
In the past few years, fascinating progress was made in the science of spin-orbit coupling effects; and fundamental research in this field is continuing vigorously. On the other hand, information technology is facing a crisis of increasing power dissipation as computing devices are being scaled to ever smaller dimensions according to the Moore's law. Every promising solid-state technology is being tried as the possible solution for this crisis. The time has come for spin-orbit physics to make an impact on practical computing applications.

For this to happen, challenges such as the following must be addressed:

Is spin-orbit torque memory competitive with spin-transfer torque memory?
Can logic circuits with spin-orbit be demonstrated?
What is the unique advantage of spin-orbit devices for non-traditional computing?

The editors will favor papers answering these questions.

This special topic of the IEEE JXCDC will present original recent research involving spin-orbit coupling effects and span at least two levels of hierarchies like:
materials - devices - circuits - computing architectures; or
design - fabrication - measurement - simulation.

Topics of Interest include but are not limited to:
1. Spin-orbit torque memory development.
2. Spin-orbit logic devices - proposals and demonstrations.
3. Spin-orbit and orbit-spin conversion in logic devices.
4. Processional spin-orbit switching.
5. Electric control of spin-orbit coupling.
6. Coupling of strain with spin-orbit effects.
7. Thermal effect in spin-orbit devices.

8. Unidirectional spin Hall magnetoresistance effect.
9. Circuits for spin-orbit logic.
10. Spin-orbit devices for analog, probabilistic, and neuromorphic computing.
11. Spin-orbit effects for spin waves.
12. Spin-orbit applications to anti-ferromagnets.

Review papers on the topic are also welcome.

Important Dates:
Submission Deadline: August 31st, 2019
First Notification: September 15th, 2019
Revision Submission: October 15, 2019
Final Decision: November 15th, 2019
Publication Online: December 1st, 2019

Submission Guidelines:
The IEEE Journal on Exploratory Solid-State Computational Devices and Circuits (JXCDC) IS AN OPEN ACCESS PUBLICATION.

The Open Access Fee is: $1,350 USD per article. Article submissions must be done through the ScholarOne Manuscripts website: https://mc.manuscriptcentral.com/jxcdc.
Guidelines for papers and supplementary materials, as well as a paper template, are provided at this website.

Additional Information can be found here: **https://sscs.ieee.org/publications/ieee-journal-on-exploratory-solid-state-computational-devices-and-circuits-jcdc**

Inquiries for the JxCDC Journal should be sent to: JXCDC@IEEE.ORG.

JxCDC is sponsored by:
Solid-State Circuits Society
Magnetics Society
Circuits & Systems Society
Council on Electronic Design Automation
Electron Devices Society
Council on Superconductivity

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The latest in SSCS Flagship Publications...

IEEE Journal of Solid-State Circuits

Vol. 54, Issue 8, August 2019

A General Theory of Injection Locking and Pulling in Electrical Oscillators-Part I:

Time-Synchronous Modeling and Injection Waveform Design
Brian Hong ; Ali Hajimiri

A General Theory of Injection Locking and Pulling in Electrical Oscillators-Part II: Amplitude Modulation in LC Oscillators, Transient Behavior, and Frequency Division
Brian Hong ; Ali Hajimiri

A Broadband CMOS RF Front End for Direct Sampling Satellite Receivers
Jie Fang ; Chaoming Zhang ; Frank W. Singor ; Jacob A. Abraham

Interference Robust Detector-First Near-Zero Power Wake-Up Receiver
Jesse Moody ; Pouyan Bassirian ; Abhishek Roy ; Ningxi Liu ; N. Scott Barker ; Benton H. Calhoun ; Steven M. Bowers

An IR-UWB CMOS Transceiver for High-Data-Rate, Low-Power, and Short-Range Communication
Geunhaeng Lee ; Jungwoon Park ; Junyoung Jang ; Taekhyun Jung ; Tae Wook Kim

High-Efficiency SiGe-BiCMOS E -Band Power Amplifiers Exploiting Current Clamping in the Common-Base Stage
Elham Rahimi ; Junlei Zhao ; Francesco Svelto ; Andrea Mazzanti

A 0.016 mm2 0.26- u W/MHz 60-240-MHz Digital PLL With Delay-Modulating Clock Buffer in 65 nm CMOS
Junheng Zhu ; Woo-Seok Choi ; Pavan Kumar Hanumolu

5-31-Hz 188- u W Light-Sensing Oscillator With Two Active Inductors Fully Integrated on Plastic
Tilo Meister ; Koichi Ishida ; Stefan Knobelspies ; Giuseppe Cantarella ; Niko Münzenrieder ; Gerhard Tröster ; Corrado Carta ; Frank Ellinger

A 12-b 1-GS/s 31.5-mW Time-Interleaved SAR ADC With Analog HPF-Assisted Skew Calibration and Randomly Sampling Reference ADC
Yuan Zhou ; Benwei Xu ; Yun Chiu

A 600-MS/s DAC With Over 87-dB SFDR and 77-dB Peak SNDR Enabled by Adaptive Cancellation of Static and Dynamic Mismatch Error
Derui Kong ; Kevin Rivas-Rivera ; Ian Galton

A Differential Optical Receiver With Monolithic Split-Microring Photodetector
Nandish Mehta ; Chen Sun ; Mark Wade ; Vladimir Stojanović

A 25-Gb/s, 2.1-pJ/bit, Fully Integrated Optical Receiver With a Baud-Rate Clock and Data Recovery
Yuan-Sheng Lee ; Wei-Hsiang Ho ; Wei-Zen Chen

A Low-Noise Chopper Amplifier Designed for Multi-Channel Neural Signal Acquisition
Deng Luo ; Milin Zhang ; Zhihua Wang

A Wireless Multi-Channel Peripheral Nerve Signal Acquisition System-on-Chip
Kian Ann Ng ; Chao Yuan ; Astrid Rusly ; Anh-Tuan Do ; Bin Zhao ; Shih-Chiang Liu ; Wendy Yen Xian Peh ; Xin Yuan Thow ; Kai Voges ; Sanghoon Lee ; Gil Gerald Lasam Gammad ; Khay-Wai Leong ; John S. Ho ; Silvia Bossi ; Gemma Taverni ; Annarita Cutrone ; Shih-Cheng Yen ; Yong Ping Xu

A 763 pW 230 pJ/Conversion Fully Integrated CMOS Temperature-to-Digital Converter With +0.81 Â°C/0.75 °C Inaccuracy
Hui Wang ; Patrick P. Mercier

A Sub-100 u m-Range-Resolution Time-of-Flight Range Image Sensor With Three-Tap Lock-In Pixels, Non-Overlapping Gate Clock, and Reference Plane Sampling
Keita Yasutomi ; Yushi Okura ; Keiichiro Kagawa ; Shoji Kawahito

Self-Timed Pulsed Latch for Low-Voltage Operation With Reduced Hold Time
Hanwool Jeong ; Juhyun Park ; Seung Chul Song ; Seong-Ook Jung

A 1.06- u W Smart ECG Processor in 65-nm CMOS for Real-Time Biometric Authentication and Personal Cardiac Monitoring
Shihui Yin ; Minkyu Kim ; Deepak Kadetotad ; Yang Liu ; Chisung Bae ; Sang Joon Kim ; Yu Cao ; Jae-Sun Seo

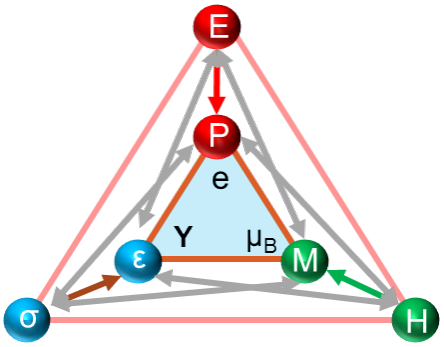
An Instruction-Driven Adaptive Clock Management Through Dynamic Phase Scaling and Compiler Assistance for a Low Power Microprocessor

Tianyu Jia ; Russ Joseph ; Jie Gu

An Energy-Efficient Reconfigurable DTLS Cryptographic Engine for Securing Internet-of-Things Applications
Utsav Banerjee ; Andrew Wright ; Chiraag Juvekar ; Madeleine Waller ; Arvind ; Anantha P. Chandrakasan

IEEE Journal on Exploratory Solid-State Computational Devices and Circuits

Issue 1, Part 2 - June 2019



Boosted Spin Channel Networks for Energy-efficient Inference
Ameya D. Patil ; Sasikanth Manipatruni ; Dmitri E. Nikonov ; Ian A. Young ; Naresh R. Shanbhag

Using Floating Gate Memory to Train Ideal Accuracy Neural Networks
Sapan Agarwal ; Diana Garland ; John Niroula ; Robin B. Jacobs-Gedrim ; Alex Hsia ; Michael S. Van Heukel

Unsupervised learning to overcome catastrophic forgetting in neural networks
Irene Muñoz-Martín ; Stefano Bianchi ; Giacomo Pedretti ; Octavian Melnic ; Stefano Ambrogio ; Daniele Ielmini

Performance Estimate of Inverse Rashba-Edelstein Magnetoelectric Devices for Neuromorphic Computing
Andrew W. Stephan ; Jiaxi Hu ; Steven J. Koester

Graded-Anisotropy-Induced Magnetic Domain Wall Drift for an Artificial Spintronic Leaky Integrate-and-Fire Neuron
Wesley H. Brigner ; Xuan Hu ; Naimul Hassan ; Christopher H. Bennett ; Jean Anne C. Incorvia ; Felipe Garcia-Sanchez ; Joseph S. Friedman

Subthreshold Spintronic Stochastic Spiking Neural Networks with Probabilistic Hebbian Plasticity and Homeostasis
Steven D. Pyle ; Ramtin Zand ; Shadi Sheikhfaal ; Ronald F. DeMara

JxCDC papers listed in order of popularity can be found online HERE.

For paper submission details, click HERE.

IEEE Solid-State Circuits Letters

Issue 6, June 2019

Low-Noise Integrated Potentiostat for Affinity-Free Protein Detection With 12 nV/rt-Hz at 30 Hz and 1.8 pArms Resolution
Sean Fischer ; Dante Muratore ; Stephen Weinreich ; Aldo Peña-Perez ; Ross M. Walker ; Chaitanya Gupta ; Roger T. Howe ; Boris Murmann

EDUCATION

August 2019 Distinguished Lectures

SSCS Shanghai	Millimeter-wave MIMO Transceivers for Beyond-5G Wireless Networks - Presented by Jeyanandh Paramesh	August 2, 2019	Shanghai Jiao Tong University, China **For more information, please click here**
SSCS Taipei	Injecting Digital into Power Electronics: Programmable Digital Gate Driver IC for Power Transistors - Presented by Makoto Takamiya	August 6, 2019	NCTU, Hsinchu, Taiwan **For more information, please click here**
SSCS Tainan	Integrated Power Management Circuits for Energy-Efficient IoT Systems - Presented by Makoto Takamiya	August 8, 2019	EDA Royal Hotel, Kaohsiung City, Taiwan **For more information, please click here**
SSCS San Diego	Talk Title TBD - Presented by Ali Sheikholeslami	August 23, 2019	Qualcomm San Diego **For more information, please click here**

CALL FOR PAPERS

ISSCC 2020: Call for Papers

IEEE International Solid-State Circuits Conference

February 16 - 20, 2020

San Francisco, California

www.isscc.org

ISSCC 2020 Conference There: Integrated Circuits Powering the AI Era"

The steady advancement of solid-state circuits has led to technological betterment in our daily living, demonstrated by exploding applications ranging from medical, wearable and mobile electronics to IoT, virtual reality, autonomous driving and robotics. While the widespread excitement resides in the applications where end-users touch and feel, the systems are enabled by integrated circuits engines that are woven into this technological fabric of our lives. Galvanized by this reality, the solid-state circuits community is driven to enhance the platform that continues to evolve. With much enthusiasm and anticipation, and even uncertainty, we look onward to this emerging AI era. Consequently, ISSCC 2020 seeks contributions that will continue to enhance and reshape the future.

Innovative and original papers are solicited in subject areas including (but not limited to) the following:

ANALOG: Amplifiers, comparators, oscillators, filters, references; nonlinear analog circuits; digitally-assisted analog circuits; MEMS/sensor interface circuits.
DATA CONVERTERS: Nyquist-rate and oversampling A/D and D/A converters; embedded and application-specific A/D and D/A converters; analog to information conversion; time-to-digital converters.
DIGITAL CIRCUITS and ARCHITECTURES & SYSTEMS: Digital circuits, building blocks, and

complete systems for microprocessors, micro-controllers, application processors, graphics processors; digital systems for communications, video and multimedia, cryptography, smart cards, security and trusted computing, accelerators, reconfigurable systems, near- and sub-threshold systems, emerging applications. Digital circuits for intra-chip communication, clock distribution, soft-error and variation-tolerant design, power management (i.e. voltage regulators, adaptive digital circuits, digital sensors), PLLs for digital clocking applications, and security circuits (i.e. PUFs, TRNG, side-channel attack countermeasures, and attack-detection sensors).
IMAGERS, MEMS, MEDICAL, & DISPLAY: Image sensors and SoCs; automotive, LIDAR, and ultrasonic sensors; MEMS sensor systems; wearable, implantable, ingestible electronics, biomedical SoCs, neural interfaces and closed-loop systems; biosensors, microarrays, and lab-on-a-chip; display electronics, displays with sensing functionality; sensing for AR/VR.
MACHINE LEARNING and AI: Chips demonstrating system, architecture and circuit innovations for machine learning and artificial intelligence: processor architectures, accelerators and digital circuits; mixed-signal, analog, near-sensor and in-sensor processing schemes; architectures leveraging near-memory and in-memory computation, using volatile or non-volatile memories.
MEMORY: Static, dynamic, and non-volatile memories for stand-alone and embedded applications; memory/SSD controllers; high-bandwidth I/O interfaces; memories based on phase-change, magnetic, spin-transfer-torque, ferroelectric, and resistive materials; array architectures and circuits to improve low-voltage operation, power reduction, reliability, and fault tolerance; application-specific circuit enhancements within the memory subsystem, including in-memory logic functions and compute.
POWER MANAGEMENT: Power management and control circuits, regulators; switched-mode power converter ICs using inductive, capacitive, and hybrid techniques; energy harvesting circuits and systems; wide-bandgap topologies and gate-drivers; power and signal isolators; robust power management circuits for automotive and other harsh environments; circuits for lighting, wireless power and envelope modulators.
RF CIRCUITS and WIRELESS SYSTEMS: Building blocks and complete solutions at RF, mm-Wave and THz frequencies for receivers, transmitters, frequency synthesizers, transceivers, SoCs, and SiPs. Innovative circuit-level and system-architecture solutions for established wireless standards and future systems or applications such as radar, sensing, and imaging.
TECHNOLOGY DIRECTIONS: Emerging IC and system solutions for: biomedical, sensor interfaces, analog signal processing, power management, computation (including non-CMOS machine learning), data storage, and communication; non-silicon-, carbon-, organic-, metal-oxide-, compound-semiconductor- and new-device-based circuits; nano, flexible, large-area, stretchable, printable, spintronics, quantum, optical, integrated photonics, and 3D-integrated electronics.
WIRELINE: Receivers/transmitters/transceivers for wireline systems, including backplane transceivers, optical links, chip-to-chip communications, 2.5/3D interconnect, copper-cable links, and equalizing on-chip links; exploratory I/O circuits for advancing data rates, power efficiency, equalization, robustness, adaptation capability, and design methodology; building blocks for wireline transceivers (such as AGCs, analog and ADC/DAC-based front ends, equalizers, clock generation and distribution circuits including PLLs, line drivers, and hybrids).

Deadline for Paper Submission: Monday, September 9, 2019, 3:00 PM Eastern Daylight Time

The ISSCC 2020 Paper Submission Site Opens July 1st!

Click here for more information

CONFERENCES

Upcoming 2019 SSCS-Sponsored Conferences

2019 IEEE Hot Chips 31 Symposium (HCS) Cupertino, California	**August 18 - 20, 2019**
ESSCIRC/ESSDERC 2019 - IEEE 45th European Solid-State Circuits Conference (ESSCIRC)/49th European Solid-State Device Research Conference Cracow, Poland	**September 23 - 26, 2019**
2019 IEEE Biomedical Circuits and Systems Conference (BioCAS) Nara, Japan	**October 17 - 19, 2019**

2019 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS) Nashville, Tennessee	**November 3 - 6, 2019**
2019 IEEE Asian Solid-State Circuits Conference (A-SSCC) Macau, China	**November 4 - 6, 2019**

SSCS-Sponsored Conferences: Proceedings

Click the links below to access the latest SSCS-Sponsored conference proceedings.

2018

2018 IEEE International Solid-State Circuits Conference (ISSCC)
2018 IEEE Custom Integrated Circuits Conference (CICC)
2018 IEEE Symposium on VLSI Circuits (VLSI)
2018 IEEE 44th European Solid-State Circuits Conference (ESSCIRC)
2018 IEEE Asian Solid-State Circuits Conference (A-SSCC)

2019

2019 IEEE International Solid-State Circuits Conference (ISSCC)

Hot Chips: A Symposium on High Performance Chips

8 - 20 August, 2019

Stanford University Campus, California

Since it started in 1989, HOT CHIPS has been known as one of the semiconductor industry's leading conferences on high-performance microprocessors and related integrated circuits. The conference is held once a year in August in the center of the world's capital of electronics activity, Silicon Valley.

Program At-A-Glance

Sunday, 8/18/2019: Tutorials

- Morning Tutorials: Acceleration in the Cloud
- The Nitro Project - Next Generation AWS Infrastructure
- Microsoft Azure
- TPU V3 in Google Cloud: Architecture and Infrastructure
- Afternoon Tutorial: RISC-V
- Reception

Monday, 8/19/2019: Conference Day 1

- Opening Remarks
- General Purpose Compute
- Memory
- Keynote 1: "Delivering the Future of High-Performance Computing with System, Software and Silicon Co-Optimization" by Dr. Lisa Su, CEO, AMD
- Methodology and ML Systems

- ML Training
- Reception

Tuesday, 8/20/2019: Conference Day 2

- Embedded and Auto
- ML Inference
- Keynote 2: "What Will the Next Node Offer Us?" by Dr. Philip Wong, VP Corporate Research, TSMC
- Interconnects
- Break
- Packaging and Security
- Graphics and AR
- Closing Remarks

Click here to register!

ESSCIRC/ESSDERC Registration is Now Open!

September 23-26, 2019
Krakow, Poland

The aim of ESSDERC and ESSCIRC is to provide an annual European forum for the presentation and discussion of recent advances in solid-state devices and circuits. The level of integration for system-on-chip design is rapidly increasing. This is made available by advances in semiconductor technology. Therefore, more than ever before, a deeper interaction among technologists, device experts, IC designers and system designers is necessary. While keeping separate Technical Program Committees, ESSDERC and ESSCIRC are governed by a common Steering Committee and share Plenary Keynote Presentations and Joint Sessions bridging both communities. Attendees registered for either conference are encouraged to attend any of the scheduled parallel sessions, regardless to which conference they belong.

CONFERENCE HIGHLIGHTS

- 4 joint keynote presentations
- 3 ESSDERC keynote presentations
- 3 ESSCIRC keynote presentations
- Invited papers with overall coverage of all spects of advanced devices and circuits
- Presentation of IEEE and ESSDERC/ESSCIRC Awards
- ESSDERC/ESSCIRC Gala Dinner on Wednesday, September 25, 2019
- Tutorials and workshops

The venue of the conference events, including workshops and tutorials, will be in the strict centre of Cracow in the Auditorium Maximum of Jagiellonian University. The working language of the conference is English.

CLICK HERE FOR REGISTRATION INFORMATION!

IEEE NEWS

2020 IEEE Technical Field Award and 2019 Herz Award Recipients Announced

The IEEE Board of Directors has approved the 2020 IEEE Technical Field Award (TFA) and 2019 IEEE Eric Herz Outstanding Staff Member Award recipients. The complete list of recipients and their citations is posted online at **www.ieee.org/awards**. Please feel free to send notes of congratulations and to publicize the recipients within your professional fields of interest other IEEE affiliations.

- The nomination deadline is 15 January annually to nominate someone for these awards. For information about or how to nominate someone for an IEEE TFA, go to: https://www.ieee.org/about/awards/technical-field-awards/index.html. For information about or how to nominate someone for the IEEE Herz Award, **click here**.
- Learn about award sponsorship opportunities by **clicking here**.
- Check out the **IEEE Awards Facebook page** and **IEEE Awards Twitter** for new postings and various photos and videos!

For Society news and happenings, check out the Summer 2019 issue of the Solid-State Circuits Magazine.