IEEE SOLID-STATE CIRCUITS SOCIETY™
IC Innovation

January 2020

UPCOMING SSCS WEBINAR

Hybrid PLL Architectures and Implementations

Presenter: Daniel Friedman, IBM T.J. Watson Research Center
Thursday, February 27th, 2020
11:00 AM ET (New York)

Abstract: Depending on the target application and on implementation constraints, both conventional charge pump PLLs and high performance digital PLLs may be excellent implementation choices. Each design type offers significant technical advantages while also raising its own set of design challenges. For example, charge pump PLLs naturally provide a feedback signal that is linearly related to phase error, but typically demand the use of a physically large loop filter capacitor if lower loop bandwidths are desired. High performance digital PLLs solve the loop capacitor problem, but may require a high performance time-to-digital converter as part of the feedback linearization solution. This presentation will focus on the exploration of a hybrid PLL architecture, an approach which features an analog proportional path in combination with a digital integral path, thus in some way offering the best of both PLL worlds. The approach will be introduced and explored through the presentation of multiple high-performance integrated hybrid PLL implementations in deep submicron CMOS technologies.

Speaker bio: Daniel Friedman is currently a Distinguished Research Staff Member and Senior Manager of the Communication Circuits and Systems department of the IBM Thomas J. Watson Research Center. He received his doctorate from Harvard University and subsequently completed post-doctoral work at Harvard and consulting work at MIT Lincoln labs, broadly in the area of image sensor design. After joining IBM, he initially developed field-powered RFID tags before turning to high data rate wireline and wireless communication. His current research interests include high-speed I/O design, PLL design, mmWave circuits and systems, and circuit/system approaches to enabling new computing paradigms. He was a co-recipient of the Beatrice Winner Award for Editorial Excellence at the 2009 ISSCC, the 2009 JSSC Best Paper Award, the 2017 ISSCC Lewis Winner Outstanding Paper Award; and the 2017 JSSC Best Paper Award; he holds more than 50 patents and has authored or co-authored more than 75 publications. He was a member of the BCTM technical program committee from 2003-2008 and of the ISSCC international technical program committee from ISSCC 2009 through ISSCC 2016; he served as the Wireline sub-committee chair from ISSCC 2012 through ISSCC 2016. He has

served as the ISSCC Short Course Chair from 2017 to the present, and is a member of the SSCS Adcom since 2018.

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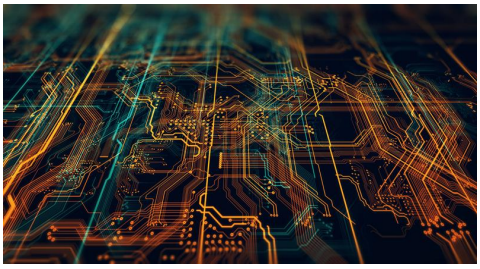
NEWS

Rising Stars Workshop at ISSCC 2020



Sunday, February 16th, 2020
6:30 PM
San Francisco Marriott Marquis

The ISSCC 2020 event includes two parallel academia and industry career panels titled "Navigating the Assistant Professorship" and "Rising to the Top in Industry" that will be open to all ISSCC 2020 attendees and to the general public at no additional cost. Well-recognized senior, mid-level, and young professionals will be available to answer your questions on navigating careers in either industry or academia.

Academia Career Panel: "Navigating the Assistant Professorship"

Abstract: The panel will provide perspectives from professors and rising stars in the academic field on the faculty application process, the necessary steps to increase your chances of being hired, and the requirements at the tenure review. The panel will provide participants with practical information and candid advice on seeking and interviewing for faculty jobs, networking, teaching, speaking, mentoring, funding research, setting up labs, getting tenure, and managing day-to-day life in academia.

Panel Moderators:
Prof. Dina Reda El-Damak, University of Southern California
Prof. Q. Jane Gu, University of California, Davis

Distinguished Panel Speaker:
"Words of Wisdom", Prof Azita Emami, California Institute of Technology

Panelists:
Prof. Vivienne Sze, Associate Professor, MIT
Prof. Esther Rodriguez Villegas, Professor, Imperial College, London
Prof. Jerald Yoo, Associate Professor, National University of Singapore
Prof. Zhengya Zhang, Associate Professor, University of Michigan

Prof. Milin Zhang, Assistant Professor, Tsinghua University

Industry Career Panel: "Rising to the Top in Industry"

Abstract: The industry career panel will tackle the question of how to become a rising star in the corporate world. Our diverse panelists bring their own experiences and perspectives from small startup organizations to large corporations, including corporate research labs. The panel will touch upon topics such as mentoring, setting career goals, deciding between management and technical tracks, publishing and filing patents, collaborating across diverse teams, and working effectively in a team. The goal is to provide the audience with the know-how to successfully navigate challenges in the corporate world, and rise to the top.

Panel Moderators:
Dr. Alicia Klinefelter, NVIDIA
Dr. Zeynep Deniz, IBM

Distinguished Panel Speaker:
"Words of Wisdom", Dr. Alice Wang, VP Hardware, Everactive

Panelists:
Wendy Belluomini, Director - AI and Cognitive Software, IBM Research
Dr. Mike Mulligan, Design Manager, Silicon Labs
Dr. Kazuko Nishimura, Manager, Technology Innovation Division, Panasonic
Dr. Walker Turner, Senior Research Scientist, NVIDIA
Dr. Laura Fick, Head of Mixed-Signal Circuits Research, Mythic AI

SSCS Young Professionals & Students Micromentoring & Career Coaching Session at ISSCC 2020

Tuesday, February 18th, 2020
6:00 PM
SoMa Room
San Francisco Marriott Marquis

Free SSCS hoodie available to all event attendees!

- Open to all students, faculty & engineers within 15 years of their first degree
- All student participants get 1 year complimentary SSCS membership
- Complimentary food and beverages for all participants
- Career coaching, entrepreneurship and publications publications advice and answers to all your questions
- Advice from leading experts from industry and academia, SSCS executives, and distinguished lecturers
- Learn about SSCS member benefits for young engineers and graduate students such as complimentary ISSCC tutorials and short courses, SSCS webinars, distinguished lecturers sponsored by SSCS to present at your region, conference travel grants for SSCS

volunteer leaders, and more..

Women in Circuits Networking Luncheon

Sponsored by the IEEE Solid-State Circuits Society & Western Digital

Thursday, February 20th, 2020
11:30 AM - 2:00 PM
Western Digital
951 Sandisk Drive
Milpitas, CA 95035

Join the Women in Circuits Networking Luncheon at Western Digital. Build and sustain a community among women in circuits. Meet and network with female luminaries in engineering.

Agenda:
11:30 AM - Doors Open
12:00 PM - 12:10 PM - Opening Talk by Kathy Wilcox, Fellow Design Engineer at AMD
12:10 PM - 12:40 PM - Distinguished Speaker Ingrid Verbauwhede, Professor at KU Leuven
12:40 PM - 1:20 PM - Special Talks by Engineering Leaders in Industry:

- **Cynthia Hsu, Director of Memory Design, Western Digital**
- **Venky Ramachandra, Director of Memory High Speed IO Design, Western Digital**

1:20 PM - 2:00 PM - Networking

Pricing:
FREE Students
$5 IEEE SSCS Members
$10 Non-Members

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SSCS YouTube Channel

SSCS now has a YouTube Channel where all CONFedu videos are posted including VLSIx 2016, CICCx 2017, ISSCCedu 2018, ESSCIRCedu 2018, CICCedu 2019, and VLSIedu 2019.

Coming Soon: ISSCCedu 2020

Call for Papers for NEW IEEE Open Journal of Solid-State Circuits

IEEE SSCS is now accepting paper submissions for its new gold fully open access IEEE Open Access Journal of Solid-State Circuits, spanning the full scope of the SSCS' fields of interest. The new journal will have an independent editorial board, established peer-review process, and will be fully

compliant with funder mandates, including Plan S. SSCS members receive a discount on Article Processing Charges. For more information or to submit a paper, **click here.**

PUBLICATIONS

The latest in SSCS Flagship Publications...

IEEE Journal of Solid-State Circuits

Vol. 55, Issue 2, February 2020

A 6.5-8.1-GHz Communication/Ranging VWB Transceiver for Secure Wireless Connectivity With Enhanced Bandwidth Efficiency and ΔΣ Energy Detection Haixin Song ; Dang Liu ; Yining Zhang ; Woogeun Rhee ; Zhihua Wang
A CMOS 76-81-GHz 2-TX 3-RX FMCW Radar Transceiver Based on Mixed-Mode PLL Chirp Generator Taikun Ma ; Wei Deng ; Zipeng Chen ; Jianxi Wu ; Wei Zheng ; Shufu Wang ; Nan Qi ; Yibo Liu ; Baoyong Chi
A Batteryless Padless Crystalless 116 μ m × 116 μ m "Dielet" Near-Field Radio With On-Chip Coil Antenna Bo Zhao ; Nai-Chung Kuo ; Benyuanyi Liu ; Yi-An Li ; Lorenzo Iotti ; Ali M. Niknejad
A Reconfigurable Spectrum-Compressing Receiver for Non-Contiguous Carrier Aggregation in CMOS SOI Hussam AlShammary ; Ahmed Hamza ; Cameron Hill ; James F. Buckwalter
High Linearity Transmit Power Mixers Using Baseband Current Feedback M. V. Praveen ; Nagendra Krishnapura
A CMOS Two-Element 170-GHz Fundamental-Frequency Transmitter With Direct RF-8PSK Modulation Peyman Nazari ; Saman Jafarlou ; Payam Heydari
An Event-Driven Quasi-Level-Crossing Delta Modulator Based on Residue Quantization Hongying Wang ; Filippo Schembari ; Robert Bogdan Staszewski
A 12.5-MHz Bandwidth 77-dB SNDR SAR-Assisted Noise Shaping Pipeline ADC Yan Song ; Chi-Hang Chan ; Yan Zhu ; Rui P. Martins
A Temperature-Stabilized Single-Channel 1-GS/s 60-dB SNDR SAR-Assisted Pipelined ADC With Dynamic Gm-R-Based Amplifier Wenning Jiang ; Yan Zhu ; Minglei Zhang ; Chi-Hang Chan ; Rui Paulo Martins
A Discrete-Time Audio Î"Î£ Modulator Using Dynamic Amplifier With Speed Enhancement and Flicker Noise Reduction Techniques Song Ma ; Liyuan Liu ; Tong Fang ; Jian Liu ; Nanjian Wu

A 76.6-dB-SNDR 50-MHz-BW 29.2-mW Multi-Bit CT Sturdy MASH With DAC Non-Linearity Tolerance
Liang Qi ; Ankesh Jain ; Dongyang Jiang ; Sai-Weng Sin ; Rui P. Martins ; Maurits Ortmanns

A Second-Order Purely VCO-Based CT ΔΣ ADC Using a Modified DPLL Structure in 40-nm CMOS
Yi Zhong ; Shaolan Li ; Xiyuan Tang ; Linxiao Shen ; Wenda Zhao ; Siliang Wu ; Nan Sun

A BJT-Based Temperature-to-Digital Converter With a ±0.25 °C 3 σ -Inaccuracy From −40 °C to +180 °C Using Heater-Assisted Voltage Calibration
Bahman Yousefzadeh ; Kofi A. A. Makinwa

A 0.3 lx-1.4 Mlx Monolithic Silicon Nanowire Light-to-Digital Converter With Temperature-Independent Offset Cancellation
Cyuyeol Rhee ; Junyoung Park ; Suhwan Kim

Combined In-Pixel Linear and Single-Photon Avalanche Diode Operation With Integrated Biasing for Wide-Dynamic-Range Optical Sensing
Hyunkyu Ouh ; Boyu Shen ; Matthew L. Johnston

A 10-mA LDO With 16-nA IQ and Operating From 800-mV Supply
Nicola Adorni ; Stefano Stanzione ; Andrea Boni

A 13.9-nA ECG Amplifier Achieving 0.86/0.99 NEF/PEF Using AC-Coupled OTA-Stacking
Somok Mondal ; Drew A. Hall

A 951-fsrms Period Jitter 3.2% Modulation Range in-Band Modulation Spread-Spectrum Clock Generator
Hyuk Sun ; Kazuki Sobue ; Koichi Hamashita ; Tejasvi Anand ; Un-Ku Moon

A 32-Gb/s Simultaneous Bidirectional Source-Synchronous Transceiver With Adaptive Echo Cancellation Techniques
Yang-Hang Fan ; Ankur Kumar ; Takayuki Iwai ; Ashkan Roshan-Zamir ; Shengchang Cai ; Bo Sun ; Samuel Palermo

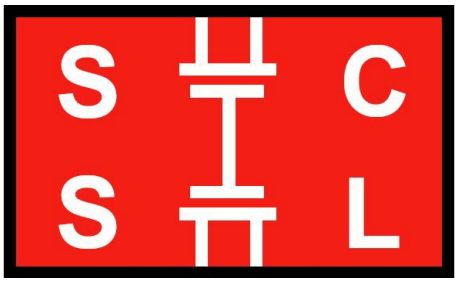
A 1.9-mW SVM Processor With On-Chip Active Learning for Epileptic Seizure Control
Shuo-An Huang ; Kai-Chieh Chang ; Horng-Huei Liou ; Chia-Hsiang Yang

STICKER: An Energy-Efficient Multi-Sparsity Compatible Accelerator for Convolutional Neural Networks in 65-nm CMOS
Zhe Yuan ; Yongpan Liu ; Jinshan Yue ; Yixiong Yang ; Jingyu Wang ; Xiaoyu Feng ; Jian Zhao ; Xueqing Li ; Huazhong Yang

Enhanced Power and Electromagnetic SCA Resistance of Encryption Engines via a Security-Aware Integrated All-Digital LDO
Arvind Singh ; Monodeep Kar ; Venkata Chaitanya Krishna Chekuri ; Sanu K. Mathew ; Anand Rajan ; Vivek De ; Saibal Mukhopadhyay

Computationally Enabled Minimum Total Energy Tracking for a Performance Regulated Sub-Threshold Microprocessor in 65-nm CMOS
Fahim ur Rahman ; Rajesh Pamula ; Visvesh S. Sathe

A 2.92-Gb/s/W and 0.43-Gb/s/MG Flexible and Scalable CGRA-Based Baseband Processor for Massive MIMO Detection
Guiqiang Peng ; Leibo Liu ; Sheng Zhou ; Shouyi Yin ; Shaojun Wei



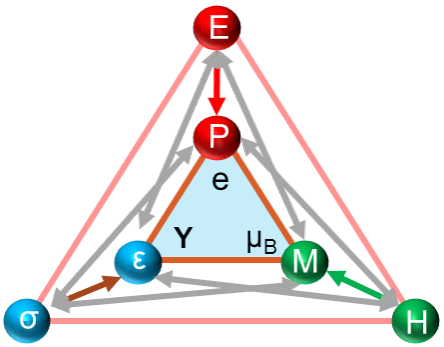
IEEE Solid-State Circuits Letters

2020

A 0.58-to-0.9-V Input 0.53-V Output 2.4- μ W Current-Feedback Low-Dropout Regulator With 99.8% Current Efficiency Ziyu Wang ; Shahriar Mirabbasi
A Cryogenic CMOS Parametric Amplifier Mohammadreza Mehrpoo ; Fabio Sebastiano ; Edoardo Charbon ; Masoud Babaie
A 117-dB In-Band CMRR 98.5-dB SNR Capacitance-to-Digital Converter for Sub-nm Displacement Sensing With an Electrically Floating Target Hui Jiang ; Samira Amani ; Johan G. Vogel ; Saleh Heidary Shalmany ; Stoyan Nihtianov
A 2.6 TOPS/W 16-Bit Fixed-Point Convolutional Neural Network Learning Processor in 65-nm CMOS Shihui Yin ; Jae-Sun Seo
A 1-V 8.1- μ W PPG-Recording Front-End With > 92-dB DR Using Light-to-Digital Conversion With Signal-Aware DC Subtraction and Ambient Light Removal Fatemeh Marefat ; Reza Erfani ; Pedram Mohseni
Novel Pulse-Based Analog Divider With Digital Output Kuan-Hung Chen ; Tse-An Chen ; Chia-Ling Wei
Secondary Side-Channel Wireline Communication Using Transmitter Clock Frequency Modulation Yi Fan Zhang ; Joshua Liang ; Shayan Shahramian ; Behzad Dehlaghi ; Ryan Bespalko ; Michael O'Farrel ; Dustin Dunwell ; Davide Tonietto ; Anthony Chan Carusone
A Coarse-Fine VCO-ADC for MEMS Microphones With Sampling Synchronization by Data Scrambling Andres Quintero ; Cesare Buffa ; Carlos Perez ; Fernando Cardes ; Dietmar Straeussnigg ; Andreas Wiesbauer ; Luis Hernandez

IEEE Journal on Exploratory Solid-State Computational Devices and Circuits

Issue 2, Part 1 - December 2019



Nonvolatile Spintronic Memory Cells for Neural Networks Andrew W. Stephan ; Qiuwen Lou ; Michael T. Niemier ; Xiaobo Sharon Hu ; Steven J. Koester
Benchmarking Delay and Energy of Neural Inference Circuits Dmitri E. Nikonov ; Ian A. Young
Energy-Efficient Convolutional Neural Network Based on Cellular Neural Network Using Beyond-CMOS Technologies Chenyun Pan ; Qiuwen Lou ; Michael Niemier ; Sharon Hu ; Azad Naeemi

JxCDC papers listed in order of popularity can be found online HERE.

For paper submission details, click HERE.

EDUCATION

Upcoming 2020 Distinguished Lectures

SSCS Delhi	Adaptive and Resilient Circuits for Processors - Presented by Keith Bowman	March 2, 2020	IIT Delhi **For more information, click here**
SSCS Saintgits College of Engineering	Adaptive and Resilient Circuits for Processors - Presented by Keith Bowman	March 6, 2020	Saintgits College of Engineering **For more information, click here**

CALL FOR PAPERS

Call for Papers: 2020 Symposia on VLSI

Technology and Circuits
June 14-19, 2020
Honolulu, Hawaii
https://vlsisymposium.org

Celebrating its 40th edition in 2020, the VLSI Symposia is the premier international conference on semiconductor technology and circuits. It offers a superb opportunity to interact and synergize on topics spanning the range from new neuromorphic devices, to beyond-the-state-of-the-art process technology to systems-on-chip and AI accelerators.

The circuits symposium is placing special emphasis on several innovation system focus areas, and encourages paper submissions on:

- Machine and deep learning
- FPGA-based accelerators
- Internet of Things
- Industrial electronics
- Big Data management
- Biomedical applications
- Robotics and autonomous transportation

In addition, submissions are welcomed in all of the following circuits areas:

- Processors, SoCs, and Machine Learning
- Digital circuits, signal integrity, and IOs
- Hardware security
- Memory circuits, architectures, and interfaces
- Biomedical circuits
- Sensors, imagers, and display circuits
- Power conversion circuits
- Analog, amplifier and filter circuits
- Wireless receivers and transmitters
- Data converters
- Frequency generation and clock circuits
- Wireline and optical transceivers

The technology symposium calls for papers in the following areas:

- Technologies for "Internet of Things"
- Technologies for Artificial Intelligence and Machine Learning Applications
- Stand-Alone and Embedded Static, Dynamic, non-Volatile and Emerging Memory
- Technologies
- CMOS Technology for Microprocessors and SoCs
- RF / Analog / Digital and Sensors Technologies

- New Process Technologies and Electronic Materials
- Advanced Packaging, System-in-Package (SiP) and 3D Technologies
- Photonics and Imaging Technologies
- Beyond CMOS Devices and Technologies for Heterogeneous Integration

Papers will be selected based on technical innovation, advances relative to previously published work, credibility of claims, and quality of writing and illustrations

Submission Information
Paper Submission Deadline: Monday, February 10, 2020, 23:59 PST

For more information, click here.

CONFERENCES

Upcoming 2020 SSCS-Sponsored Conferences

2020 IEEE International Solid-State Circuits Conference (ISSCC) San Francisco, California	**Feb 16 - 20, 2020**
2020 Design, Automation & Test in Europe Conference & Exhibition (DATE) Grenoble Cedex 2, France	**Mar 9 - 13, 2020**
2020 IEEE Custom Integrated Circuits Conference (CICC) Boston, MA	**Mar 22 - 25, 2020**
2020 International Symposium on VLSI Technology, Systems, and Applications (VLSI-TSA) Hsinchu, Taiwan	**Apr 20 - 23, 2020**
2020 International Symposium on VLSI Design, Automation, and Test (VLSI-DAT) Hsinchu, Taiwan	**Apr 20 - 23, 2020**
2020 IEEE Symposia on VLSI Technology and Circuits Honolulu, Hawaii	**Jun 16 - 19, 2020**
2020 IEEE Radio Frequency Integrated Circuits Symposium (RFIC) Los Angeles, California	**Jun 21 - 23, 2020**
2020 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS) Monterey, California	**Nov 8 - 11, 2020**
2020 IEEE Asian Solid-State Circuits Conference (A-SSCC) Hiroshima, Japan	**Nov. 9 - 11, 2020**

SSCS-Sponsored Conferences: Proceedings

Click the links below to access the latest SSCS-Sponsored conference proceedings.

2018

2018 IEEE International Solid-State Circuits Conference (ISSCC)
2018 IEEE Custom Integrated Circuits Conference (CICC)
2018 IEEE Symposium on VLSI Circuits (VLSI)
2018 IEEE 44th European Solid-State Circuits Conference (ESSCIRC)
2018 IEEE Asian Solid-State Circuits Conference (A-SSCC)

2019

2019 IEEE International Solid-State Circuits Conference (ISSCC)
2019 IEEE Custom Integrated Circuits Conference (CICC)
2019 Symposium on VLSI Circuits
2019 IEEE 45th European Solid-State Circuits Conference (ESSCIRC)

For Society news and happenings, check out the Fall 2019 issue of the Solid-State Circuits Magazine.
