IEEE SOLID-STATE CIRCUITS SOCIETY

Where ICs are in IEEE

January 2019

NEWS

UPCOMING WEBINAR

"Energy Efficient Computing in Nanoscale CMOS"

Presented by Vivek De
February 28, 2019
1:00 PM ET

CLICK HERE TO REGISTER

Abstract: Future computing systems spanning exascale supercomputers to wearable devices demand orders of magnitude improvements in energy efficiency while providing desired performance. The system-on-chip (SoC) designs need to span a wide range of performance and power across diverse platforms and workloads. The designs must achieve robust near-threshold-voltage (NTV) operation in nanoscale CMOS process while supporting a wide voltage-frequency operating range with minimal impact on die cost. We will discuss circuit and design technologies to overcome the challenges posed by device parameter variations, supply noises, temperature excursions, aging-induced degradations, workload and activity changes, and reliability considerations. The major pillars of energy-efficient SoC designs are: (1)

circuit/design optimizations for fine-grain multi-voltage & wide dynamic range, (2) fine-grain on-die power delivery & management, (3) dynamic adaptation & reconfiguration, (4) dynamic on-die error detection & correction, and (5) efficient interconnects.

Bio: Vivek De is an Intel Fellow and Director of Circuit Technology Research in Intel Labs. He is responsible for providing strategic technical directions for long term research in future circuit technologies and leading energy efficiency research across the hardware stack. He has 249 publications in refereed international conferences and journals and 209 patents issued, with 26 more patents filed (pending). He received an Intel Achievement Award for his contributions to an integrated voltage regulator technology. He received a Best Paper Award at the 1996 IEEE International ASIC Conference, and nominations for Best Paper Awards at the 2007 IEEE/ACM Design Automation Conference (DAC) and 2008 IEEE/ACM International Conference on Computer-Aided Design (ICCAD). One of his publications was recognized in the 2013 IEEE/ACM Design Automation Conference (DAC) as one of the "Top 10 Cited Papers in 50 Years of DAC". He received a PhD in Electrical Engineering from Rensselaer Polytechnic Institute, Troy, New York. He is a Fellow of the IEEE.

Starting January 1, 2019, SSCS will be charging for CEU's and PDH's. Attendees of webinars will have to pay a fee to obtain CEU's and PDH's. However, webinar attendees can obtain a complimentary certificate of attendance.

PUBLICATIONS

The latest in SSCS Flagship Publications...

IEEE Journal of Solid-State Circuits

Vol. 54, Issue 2, February 2019

High-Linearity Bottom-Plate Mixing Technique With Switch Sharing for N -path Filters/Mixers **Yuan-Ching Lien ; Eric A. M. Klumperink ; Bernard Tenbroek ; Jon Strange ; Bram Nauta**
A 3.7-mW 2.4-GHz Phase-Tracking GFSK Receiver With BBPLL-Based Demodulation **Yining Zhang ; Meng Ni ; Xiaohua Huang ; Woogeun Rhee ; Zhihua Wang**
A Low-Power Compact IEEE 802.15.6 Compatible Human Body Communication Transceiver With Digital Sigma-Delta IIR Mask Shaping

Bo Zhao ; Yong Lian ; Ali M. Niknejad ; Chun Huat Heng

An 82-107.6-GHz Integer- N ADPLL Employing a DCO With Split Transformer and Dual-Path Switched-Capacitor Ladder and a Clock-Skew-Sampling Delta-Sigma TDC
Zhiqiang Huang ; Howard C. Luong

85-110-GHz CMOS Magnetic-Free Nonreciprocal Components for Full-Duplex Transceivers
Chang Yang ; Ping Gui

A 0.53-THz Subharmonic Injection-Locked Phased Array With 63- Î¼ W Radiated Power in 40-nm CMOS
Kaizhe Guo ; Yang Zhang ; Patrick Reynaert

A Low-Power, Differential Relaxation Oscillator With the Self-Threshold-Tracking and Swing-Boosting Techniques in 0.18- um CMOS
Shao-Yung Lu ; Yu-Te Liao

A Single-Channel, 600-MS/s, 12-b, Ringamp-Based Pipelined ADC in 28-nm CMOS
Jorge Lagos ; Benjamin Hershberg ; Ewout Martens ; Piet Wambacq ; Jan Craninckx

A 10-b 20-MS/s SAR ADC With DAC-Compensated Discrete-Time Reference Driver
Maoqiang Liu ; Arthur H. M. van Roermund ; Pieter Harpe

A 0.029-mm2 17-fJ/Conversion-Step Third-Order CT Delt Sigma ADC With a Single OTA and Second-Order Noise-Shaping SAR Quantizer
Jiaxin Liu ; Shaolan Li ; Wenjuan Guo ; Guangjun Wen ; Nan Sun

A 78.5-dB SNDR Radiation- and Metastability-Tolerant Two-Step Split SAR ADC Operating Up to 75 MS/s With 24.9-mW Power Consumption in 65-nm CMOS
Hongda Xu ; Hai Huang ; Yongda Cai ; Ling Du ; Yuan Zhou ; Benwei Xu ; Datao Gong ; Jingbo Ye ; Yun Chiu

A 64-Gb/s 4-PAM Transceiver Utilizing an Adaptive Threshold ADC in 16-nm FinFET
Luke Wang ; Yingying Fu ; Marc-Andre LaCroix ; Euhan Chong ; Anthony Chan Carusone

12-Gb/s Over Four Balanced Lines Utilizing NRZ Braid Clock Signaling With No Data Overhead and Spread Transition Scheme for 8K UHD Intra-Panel Interfaces
Yeonho Lee ; Yoonjae Choi ; Junyoung Song ; Sewook Hwang ; Sang-Geun Bae ; Jaehun Jun ; Chulwoo

A Versatile CMOS Transistor Array IC for the Statistical Characterization of Time-Zero Variability, RTN, BTI, and HCI
Javier Diaz-Fortuny ; Javier Martin-Martinez ; Rosana Rodriguez ; Rafael Castro-Lopez ; Elisenda Roca ; Xavier Aragones ; Enrique Barajas ; Diego Mateo ; Francisco V. Fernandez ; Montserrat Nafria

Compensation Pixel Circuit to Improve Image Quality for Mobile AMOLED Displays
Chih-Lung Lin ; Po-Chun Lai ; Li-Wei Shih ; Chia-Che Hung ; Po-Cheng Lai ; Tsu-Yuan Lin ; Kuang-Hsiang Liu ; Tsang-Hong Wang

An 80X25 Pixel CMOS Single-Photon Sensor With Flexible On-Chip Time Gating of 40 Subarrays for Solid-State 3-D Range Imaging
Henna Ruokamo ; Lauri W. Hallman ; Juha Kostamovaara

A 141- uW High-Voltage MEMS Gyroscope Drive Interface Circuit Based on Flying Capacitors
Maximilian Marx ; Stefan Rombach ; Sebastian Nessler ; Daniel De Dorigo ; Yiannos Manoli

A 42 nJ/Conversion On-Demand State-of-Charge Indicator for Miniature IoT Li-Ion Batteries
Junwon Jeong ; Seokhyeon Jeong ; Dennis Sylvester ; David Blaauw ; Chulwoo Kim

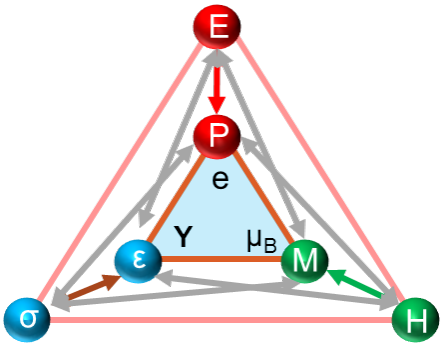
A Four-Camera VGA-Resolution Capsule Endoscope System With 80-Mb/s Body Channel Communication Transceiver and Sub-Centimeter Range Capsule Localization
Jaeeun Jang ; Jihee Lee ; Kyoung-Rog Lee ; Jiwon Lee ; Minseo Kim ; Yongsu Lee ; Joonsung Bae ; Hoi-Jun Yoo

Ultra-Low Power 18-Transistor Fully Static Contention-Free Single-Phase Clocked Flip-Flop in 65-nm CMOS

Yunpeng Cai ; Anand Savanth ; Pranay Prabhat ; James Myers ; Alex S. Weddell ; Tom J. Kazmiersk
An 88-fJ/40-MHz [0.4 V]-0.61-pJ/1-GHz [0.9 V] Dual-Mode Logic 8x8 bit Multiplier Accumulator With a Self-Adjustment Mechanism in 28-nm FD-SOI Ramiro Taco ; Itamar Levi ; Marco Lanuzza ; Alexander Fish
Improved Power/EM Side-Channel Attack Resistance of 128-Bit AES Engines With Random Fast Voltage Dithering Arvind Singh ; Monodeep Kar ; Sanu K. Mathew ; Anand Rajan ; Vivek De ; Saibal Mukhopadhyay
A ReRAM Macro Using Dynamic Trip-Point-Mismatch Sampling Current-Mode Sense Amplifier and Low-DC Voltage-Mode Write-Termination Scheme Against Resistance and Write-Delay Variation Chieh-Pu Lo ; Wen-Zhang Lin ; Wei-Yu Lin ; Huan-Ting Lin ; Tzu-Hsien Yang ; Yen-Ning Chiang ; Ya-Chin King ; Chrong-Jung Lin ; Yu-Der Chih ; Tsung-Yung Jonathon Chang ; Meng-Fan Chang
A 7T-SRAM With Data-Write Technique by Capacitive Coupling Daisaburo Takashima ; Masato Endo ; Kazuhiro Shimazaki ; Manabu Sai ; Masaaki Tanino

IEEE Journal on Exploratory Solid-State Computational Devices and Circuits

Volume 4, 2018



Circuit Models for Spintronic Devices Subject to Electric and Magnetic Fields Meshal Alawein ; Hossein Fariborzi
Complementary Logic Implementation for Antiferromagnet Field-Effect Transistors Chenyun Pan ; Azad Naeemi
Evaluation of Operating Margin and Switching Probability of Voltage- Controlled Magnetic Anisotropy Magnetic Tunnel Junctions Jeehwan Song ; Ibrahim Ahmed ; Zhengyang Zhao ; Delin Zhang ; Sachin S. Sapatnekar ; Jian-Ping Wang ; Chris H. Kim
Towards a Strong Spin-Orbit Coupling Magnetoelectric Transistor Peter A. Dowben ; Christian Binek ; Kai Zhang ; Lu Wang ; Wai-Ning Mei ; Jonathan P. Bird ; Uttam Singisetti ; Xia Hong ; Kang L. Wang ; Dmitri Nikonov
Using Programmable Graphene Channels as Weights in Spin-Diffusive Neuromorphic Computing Jiaxi Hu ; Gordon Stecklein ; Yoska Anugrah ; Paul A. Crowell ; Steven J. Koester
BCB Evaluation of High-Performance and Low-Leakage Three-Independent-Gate Field Effect Transistors Jorge Romero-Gonzalez ; Pierre-Emmanuel Gaillardon
Tunnel FET Analog Benchmarking and Circuit Design Hao Lu ; Paolo Paletti ; Wenjun Li ; Patrick Fay ; Trond Ytterdal ; Alan Seabaugh
Improving Energy Efficiency of Low Voltage Logic by Technology-Driven Design Kaushik Vaidyanathan ; Daniel H. Morris ; Uygar E. Avci ; Huichu Liu ; Tanay Karnik ; Hong Wang ; Ian A. Young

Inversion Charge Boost and Transient Steep-Slope Induced by Free-Charge-Polarization Mismatch in a Ferroelectric-Metal-Oxide-Semiconductor Capacitor

Sou-Chi Chang ; Uygar E. Avci ; Dmitri E. Nikonov ; Ian A. Young

Performance Characterization and Majority Gate Design for MESO-Based Circuits

Zhaoxin Liang ; Meghna G. Mankalale ; Jiaxi Hu ; Zhengyang Zhao ; Jian-Ping Wang ; Sachin S. Sapatnekar

JxCDC papers listed in order of popularity can be found online HERE.

For paper submission details, click HERE.

IEEE Solid-State Circuits Letters

Volume 1, Issue 7, July 2018

A 180 mV 81.2%-Efficient Switched-Capacitor Voltage Doubler for IoT Using Self-Biasing Deep N-Well in 16-nm CMOS FinFET

Yu-Tso Lin ; Naser Pourmousavian ; Chao-Chieh Li ; Min-Shueh Yuan ; Chih-Hsien Chang ; Robert Bog

EDUCATION

February 2019 Distinguished Lectures

SSCS/AP/CAS/ED/MTT San Diego	RF Harmonic Oscillators Integrated in Silicon Technologies - Presented by Pietro Andreani	February 15, 2019	Qualcomm, San Diego **For more information, please click here**
SSCS/AP/CAS/ED/MTT San Diego	Challenges in the Design of Integrated Circuits for Wireless Power Delivery and Information Transfer in Implantable Medical Applications - Presented by Zhihua Wang	February 22, 2019	Qualcomm, San Diego **For more information, please click here**
SSCS/CAS Central Texas	Design of synthesizable digital PLL - Presented by Jae-Yoon Sim	February 25, 2019	University of Texas at Austin **For more information, please click here**

CONFERENCES

Upcoming SSCS-Sponsored Conferences

2019 IEEE International Solid-State Circuits Conference (ISSCC) San Francisco, California	**February 17 - 19, 2019**
2019 Design, Automation & Test in Europe Conference and Exhibition Florence, Italy	**March 25 - 29, 2019**
2019 IEEE Custom Integrated Circuits Conference (CICC) Austin, Texas	**April 14 - 17, 2019**
2019 International Symposium on VLSI Design, Automation and Test (VLSI-DAT) Hsinchu, Taiwan	**April 22 - 25, 2019**
2019 International Symposium on VLSI Technology, Systems, and Application (VLSI-TSA) Hsinchu, Taiwan	**April 22 - 25, 2019**
2019 IEEE Radio Frequency Integrated Circuits Symposium (RFIC) Boston, Massachusetts	**June 2 - 4, 2019**
2019 Symposium on VLSI Circuits Kyoto, Japan	**June 9 - 14, 2019**
2019 IEEE Hot Chips 31 Symposium (HCS) Cupertino, California	**August 18 - 29, 2019**
ESSCIRC 2019 - IEEE 45th European Solid-State Circuits Conference (ESSCIRC) Cracow, Poland	**September 23 - 26, 2019**
2019 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS) Nashville, Tennessee	**November 3 - 6, 2019**

SSCS-Sponsored Conferences: Proceedings

Click the links below to access 2018 SSCS-Sponsored conference proceedings.

2018 IEEE International Solid-State Circuits Conference (ISSCC)
2018 IEEE Custom Integrated Circuits Conference (CICC)
2018 IEEE Symposium on VLSI Circuits (VLSI)
2018 IEEE 44th European Solid-State Circuits Conference (ESSCIRC)
2018 IEEE Asian Solid-State Circuits Conference

DATE 2019 in Florence: Advance Program now Available

View the advance program here: https://www.date-conference.com/programme

The DATE conference will take place from 25 to 29 March 2019 at the Firenze Fiera in Florence, Italy. It combines the world's favorite electronic systems design and test conference with an international exhibition for electronic design, automation and test, from system-level hardware and software implementation right down to integrated circuit design.

On the first day of the DATE week, six in-depth technical tutorials on the main topics of DATE as well as two industry hands-on tutorials will be given by leading experts in their respective fields. The topics cover Machine Learning for Manufacturing and Test, OpenCL Design Flows for FPGAs, Approximate Computing, Hardware-based Security, Co-simulation, and Safety and Security in Automotive, while the hands-on tutorials are on Quantum Computing with IBM Q and on Python Productivity for Xilinx Zynq.

During the Opening Ceremony on Tuesday, plenary keynote lectures will be given by Kenneth P. Caviasca, Vice President of Internet of Things Group and General Manager of Architecture, Silicon and Platform Engineering at Intel, and Jürgen Bortolazzi, Director Driver Assistance Systems at Porsche. On the same day, the Executive Track offers a series of business panels with executive speakers from companies leading the design and automation industry, discussing hot topics. Furthermore, a talk by Claudio Giorgione, Curator of the Leonardo Department at the National Museum of Science and Technology Milano, will give insight into live and work of Leonardo da Vinci in line with the 500th anniversary of his death, which is celebrated in Florence in 2019.

The main conference programme from Tuesday to Thursday includes 58 technical sessions organized in parallel tracks from the four areas:

D - Design Methods & Tools
A - Application Design
T - Test, Reliability, and Robustness
E - Embedded and Cyber-physical Systems

and from several special sessions on Hot Topics, such as Emerging Design Technologies, Design and Test of Secure Systems, IoT Security, Embedded Systems for Deep Learning, Augmented Living and Personalized Healthcare, Robotics and Industry 4.0., as well as results and lessons learned from European projects. Additionally, there are numerous Interactive Presentations which are organized into five IP sessions.

Two Special Days in the programme will focus on areas bringing new challenges to the system design community: Embedded Meets Hyperscale and HPC and Model-Based Design of Intelligent Systems. Each of the Special Days will have a full programme of keynotes, panels, tutorials and technical presentations.

Heterogeneous computing with multiple, specialized processors and application-specific accelerators is vital for embedded systems to meet performance, latency, and efficiency targets. The same goals of fast, efficient, and cost-effective processing are also gating factors for the evolution of hyperscale data center (DC) and high-performance computing (HPC) and Moore's law no longer provides the necessary efficiency gains. The theme of the special day Embedded Meets Hyperscale and HPC is to highlight this confluence of methods and technologies to better understand, how heterogeneous computing is shaping the future of hyperscale DCs and HPC.

The special day on Model-Based Design of Intelligent Systems will explore all that is needed to lift model-based design into the era of intelligent systems. Topics addressed are, among others, model-based design frameworks for IoT systems, model-based machine learning, and application of model-based design in safety-critical and autonomous systems. The special day will also highlight the upcoming challenges in this domain and invite the DATE community to help overcome them.

To inform attendees on commercial and design-related topics, there will be a full programme in the Exhibition Theatre which will combine presentations by exhibiting companies, best-practice reports by industry leaders on their latest design projects and selected conference special sessions. Two of the highlights here will be a career session called Inspiring Futures!,where interested companies may introduce their work and job portfolios, and the newly created Publisher's Session.
The conference is complemented by an exhibition, running for three days (Tuesday - Thursday),

including exhibition booths from companies, and collaborative research initiatives including EU project presentations.The exhibition provides a unique networking opportunity and states the perfect venue for industries to meet University Professors to foster University Programme and especially for PhD Students to meet future employers.

On Friday, 10 full-day workshops cover several hot topics from areas like (a) Open Source and Machine Learning in EDA, (b) Emerging Techniques for Memories, Interconnections, and Quantum Computing, (c) Hardware Design, Synthesis, and Approximate Computing, as well as EDA in application domains such as (d) Autonomous Systems and IoT.

For further information please visit: **www.date-conference.com**

IEEE Radio Frequency Integrated Circuits Symposium

2-4 June 2019

Boston, Massachusetts

The **2019 IEEE Radio Frequency Integrated Circuits Symposium (RFIC 2019)** will be held in Boston, MA on 2-4 June 2019. The RFIC Symposium is an annual IEEE conference that is combined with the International Microwave Symposium (IMS), ARFTG, and the Industry Exhibition to form the "Microwave Week", the largest worldwide RF/microwave technical meeting of the year. In 2019, the conference will also extend its focus to emerging circuit technologies related to RFIC, such as MEMS sensors and actuators, heterogeneous and 3D ICs, silicon photonics, biomedical applications, quantum computing and more. We cordially invite you to participate in this international symposium.

To encourage student attendance, the IMS'19 is offering deep registration discounts and numerous benefits for student volunteers who are IEEE members and willing to help with conference activities. For more details, visit **https://ims-ieee.org/students-main/student-volunteers.**

For 2019, RFIC is promoting a new educational experience for the attendees: a "Technical Lecture" comprising a 1 ½ hour interactive short course delivered by a distinguished speaker during lunchtime on Sunday, between the AM and PM workshops. For 2019, Prof. Ali Niknejad from University of California, Berkeley, will teach "Fundamentals of mmWave IC Design in CMOS".

The 2019 RFIC Symposium will begin on Sunday, June 2nd 2019, with 12 RFIC focused workshops and one technical lecture. In addition, there will be several joint RFIC/IMS workshops on Sunday and Monday. These workshops cover a wide range of advanced topics in RFIC technology and IC design, including power amplifiers, 5G systems, silicon photonics, quantum computing, hardware security, and beyond. The 2019 RFIC Plenary Session on Sunday will conclude the day with two visionary plenary talks: Dr. Greg Henderson, Senior Vice President, Automotive, Communications and Aerospace/Defense at Analog Devices, will outline "The Digital Future of RFICs", and Dr. Ir. Michael Peeters, Program Director Connectivity and Humanized Technology at IMEC, will address the question "Do the networks of the future care about the materials of the past?". Immediately after the plenary session, the RFIC reception will follow, with highlight from our industry showcase and student paper finalists in an engaging social and technical evening event supported by the RFIC Symposium corporate sponsors. You will not want to miss the RFIC reception!

On Monday and Tuesday, the RFIC Symposium will have multiple tracks of oral technical paper sessions. The 5G Summit technical sessions on Tuesday afternoon will provide high-level 5G overview presentations that will complement the 5G-focused RFIC technical sessions on Tuesday morning. Two enlightening panels will be featured during lunchtime on both days: "The Internet of Things (IoT) - back to the future, or no future?" on Monday and "Will Artificial Intelligence (AI) and Machine Learning (ML) take away my job as an RF/Analog Designer?" on Tuesday.

On behalf of the RFIC Steering and Executive Committees, we welcome you to join us at the 2019 RFIC Symposium in Boston, Massachusetts! Please visit the RFIC 2019 website **(http://rfic-ieee.org/)** for more details and updates.

Call for Participation:
VLSI Technology, Systems, and Applications
VLSI Design, Automation and Test
22-25 April 2019
Hsinchu, Taiwan

REGISTER NOW!

VLSI-TSA https://expo.itri.org.tw/2019vlsitsa	VLSI-DAT https://expo.itri.org.tw/2019vlsidat
• 40 Selected Top Papers • 4 Special Sessions on - Silicon Photonics, Low Dimensional Devices and Materials, 3D/Heterogeneous Integration and Unconventional Manufacturing, Machine Learning for the Semiconductor Industry • **2 Profound Short Courses** • Best Student Paper Award	• 36 Selected Top Papers • 3 Special Sessions on - Advanced AI Chips and Applications, Silicon Photonics for Next Generation Chips, Heterogeneous Integration/Flexible Hybrid Electronics • 2 Industrial Sessions • **3 Profound Tutorials** • Best Paper Award

Joint Program Highlights

- Six Plenary Talks by Ghavam Shahidi, IBM Research ; Li Fung Chang, Industrial Technology Research Institute ; Winfried Kaiser, Carl Zeiss SMT GmbH ; Peter Hsieh, ARM ; Thomas Ernst, CEA-LETI ; Mike Davies, Intel
- Two Luncheon Keynotes by H-S. Philip Wong, Vice President of Corporate Research, TSMC ;Owain Vaughan, Chief Editor of Nature Electronics
- Two Joint Special Sessions on (5G: From Systems to Device) and (Future of Memory: From Storage to Computing)

CALL FOR PAPERS

ESSCIRC/ESSDERC 2019: Call for Papers
European Solid-State Device Research Conference
European Solid-State Circuits Conference
September 23-26, 2019
Cracow, Poland

The aim of ESSDERC and ESSCIRC is to provide an annual European forum for the presentation and discussion of recent advances in solid-state devices and circuits. The level of integration for system-on-chip design is rapidly increasing. This is made available by advances in semiconductor technology. Therefore, more than ever before, a deeper interaction among technologists, device experts, IC designers and system designers is necessary. While keeping separate Technical Program Committees, ESSDERC and ESSCIRC are governed by a common Steering Committee and share Plenary Keynote Presentations and Joint Sessions bridging both communities. Attendees registered for either conference are encouraged to attend any of the scheduled parallel sessions, regardless to which conference they belong.

Although not limited, papers are solicited for the following main topics:

ESSCIRC

Analog
OP-Amps and instrumentation amplifiers; CT and DT filters; SC circuits, Comparators; Voltage and current references; High voltage circuits; Nonlinear analog circuits; Digitally assisted analog circuits.

Data Converters
Nyquist-rate and oversampling A/D and D/A converters; Sample-hold circuits; Time-to-digital converters; ADC and DAC calibration/error correction circuits.

RF and mm-Wave
RF/IF building blocks like LNAs, mixers, power amplifiers, IF amplifiers; Power detectors; Subsystems for RF, mm-wave and THz design.

Frequency Generation
Modulators/demodulators; VCOs; PLLs; DLLs; Frequency synthesizers; Frequency dividers; Integrated passive components.

Wireless and Wireline Systems
Receivers/transmitters/transceivers for wireless/wireline systems Gigabit serial links; Clock and data recovery; Equalization; Advanced modulation systems; Base station and handset applications; TV/radio/satellite receivers and transmitters; Radars.

Sensors, Imager and Biomedical
Sensor subsystems and interfaces; Accelerometers; Temperature sensing; Imaging and smart imaging chips; AMOLED; MEMs subsystems; RF MEMs; Implantable electronic ICs; Biomedical imagers; Bio-MEMs integrated systems; Lab-on-chip; Organic LED and liquid-crystal-display interface circuits; Flat panel and projection display.

Digital, Security and Memory
Techniques for energy efficient and high performance digital circuits; I/O and inter-chip communication; Reconfigurable digital circuits; Security and encryption circuits; Clocking; Arithmetic building blocks; Memories; Microprocessors; DSPs; Memory interfacing; Bus interfacing; Many core and multirate ICs; 3D integration.

Power Management
Energy transducers; Power regulators; DC-DC converters; Energy scavenging circuits; LDOs Boost-buck-converters; LED and gate drivers; Sequencers and supervisors; Green circuits.

ESSDERC

CMOS Devices and Technology
CMOS scaling; Novel MOS device architectures; Circuit/device interaction and co-optimization; High-mobility channel devices; CMOS front-end or back-end processes; Interconnects; Integration of RF or photonic devices; 3D integration; Front-end and back-end manufacturing processes; 3D integration and wafer-level packaging; Reliability and characterization of materials, processes and devices; Advanced interconnects; ESD, latch-up, soft errors, noise and mismatch behavior, hot carrier effects, bias temperature instabilities, and EMI; Defect monitoring and control; Metrology; Test structures and methodologies; Manufacturing yield modeling, analysis and testing.

Opto-, Power and Microwave Devices
New device or process architectures; New phenomena and performance improvement of optoelectronic, high voltage, smart power, IGBT, microwave devices; Passive devices, antennas and filters (including Si, Ge, SiC, GaN); Optoelectronic devices including sensors, LEDs, semiconductor lasers; Photovoltaic devices; Studies of high temperature operation; IC cooling and packaging aspects; Reliability and characterization of materials, processes and devices.

Physical Modeling of Materials and Devices
Numerical, analytical and statistical modeling and simulation of electronic, optical or hybrid devices, the interconnect, isolation and 2D or 3D integration; Aspects of materials, fabrication processes and devices, e.g. advanced physical phenomena (quantum mechanical and non-stationary transport phenomena, ballistic transport, and other related aspects); Mechanical or electro-thermal modeling and simulation; DfM. Reliability of materials and devices.

Compact Modeling of Devices and Circuits

Compact/SPICE modeling of electronic, optical, organic, and hybrid devices and their IC implementation and interconnection. Topics include compact/SPICE models and their Verilog-A standardization of the semiconductor devices (including Bio/Med sensors, MEMS, Microwave, RF, High voltage and Power), parameter extraction, compact models for emerging technologies and novel devices, performance evaluation, reliability, variability, and open source benchmarking/implementation methodologies. Modeling of interactions between process, device, and circuit design as well as Foundry/Fabless Interface Strategies.

Memory Devices and Technology
Embedded and stand-alone memories; DRAM, FeRAM, MRAM, ReRAM, PCRAM, Flash, Nanocrystal and single/few-electron memories, Organic memories, NEMS-based devices, Selectors; Novel memory cell concepts and architectures, covering device physics, reliability, process integration and manufacturability issues and including 3D NAND Flash, crosspoint arrays, and 3D systems integration; Devices and concepts for neuromorphic computing, memory-enabled logic and security applications.

Emerging non-CMOS Devices and Technologies
Novel non-CMOS materials, processes and devices, (carbon nanotubes, nanowires and nanoparticles, 2D materials, graphene, metal oxides, etc.) for electronic, optoelectronic, sensor & actuator applications; Reliability and characterization of materials, processes and devices; Molecular and quantum devices; Nanophotonics, plasmonics, spintronics, selfassembling methods; Energy harvesters; High frequency digital and analog devices including THz; New high-mobility channels (strained Si, Ge, SiGe).

Sensor Devices and Technology
Design, fabrication, modeling, reliability, packaging and smart systems integration of actuators (discrete SoC, SiP, or heterogenous 3D integration); MEMS, NEMS, optical, chemical or biological sensors; Display technologies; High-speed imagers; TFTs; Organic and flexible substrate electronics.

POST-CONFERENCE PUBLICATIONS

All accepted ESSDERC and ESSCIRC papers will be included in the conference proceedings and posted on IEEE Xplore after the conference.

Co-publication of qualified papers in SSC-L
Upon acceptance, outstanding ESSCIRC papers will be invited to submit to a Special Issue of IEEE Solid-State Circuit Letters (SSC-L, 4 pages format) on the ESSCIRC, subject to additional editorial and quality reviews. Publication on IEEE Xplore of the SSC-L Special Issue is timed to be September 1, 2019

Special JSSC issue
Authors of outstanding papers will be invited to submit their work to a Special Issue of IEEE Journal of Solid-State Circuits (JSSC, up to 10-12 pages format) on the ESSCIRC to appear in July 2020, with an opportunity to provide additional material, such as mathematical analysis, in-depth circuit description, more experimental results and benchmarking data.

Special J-EDS issue
Authors of selected outstanding ESSDERC papers will be invited to submit their work to the special issue of IEEE Journal of the Electron Devices Society. The authors will be asked to revise the conference version of the paper by adding at least 30% new material. All manuscripts will undergo additional editorial and quality review process.

IMPORTANT INFORMATION
Manuscript guidelines as well as instructions on how to submit electronically will be available on the **conference website**. Papers must not exceed four A4 pages with all illustrations and references included.

Key Dates:

Paper submission Deadline: April 8th, 2019
Paper Selection Meeting: May 20th, 2019
Notification of Acceptance: May 31st, 2019
Early Registration Start: June 3rd, 2019

UPCOMING EVENTS

Students and Young Professionals Micro-Mentoring and Career Coaching Session at ISSCC 2019

Sponsored by the IEEE Solid-State Circuits Society Young Professionals

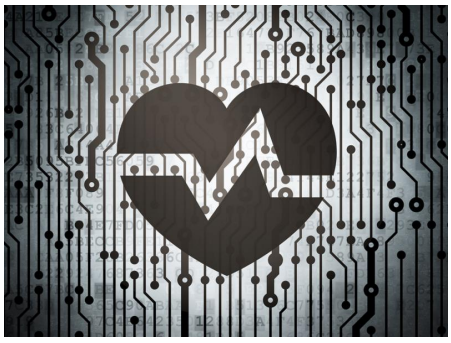
Tuesday, February 19, 2019
6:00 PM - 7:00 PM
Sierra A/B Room
San Francisco Marriott Marquis

Complimentary event for all students, faculty, and engineers within 15 years of their first degree.

- **Leading experts from industry and academia, IEEE SSCS Executives, and Distinguished Leaders will share their experiences**
- **1 on 1 answers to all your questions on publications, entrepreneurship, industry vs. academia and career coaching.**
- **Complimentary giveaways for attendees**
- **Free SSCS student membership offer for event attendees**

Learn about SSCS member benefits for young engineers & students, such as complimentary tutorials and short courses, webinars, distinguished lecturers to present at your region, networking with 10,000 + SSCS members around the globe, latest technical content, Student fellowships programs and more.

Click here to RSVP (walk-in's welcome!)



ISSCC Evening Event - How to Save Lives with Circuits

Sunday, February 17, 2019 at 6:00 PM
San Francisco, California Marriott Marquis

The workshop highlights circuits and their impact on healthcare-related industries. The goal of the panel is to provide perspectives from system architects, security experts and circuit designers on where we should be heading with the large amount of data that is being generated from more-advanced tests and increased monitoring of our current health status.

Distinguished Speakers

6:00 - 6:30 PM
Catalyzing Growth and Innovation
Sue Siegel
GE Chief Innovation Officer and CEO, GE Business Innovations

6:30 - 7:00 PM
Better Circuits for a Better World
Dr. Jennifer Lloyd
VP, Healthcare and Consumer, Analog Devices

Invited Talks

7:00 - 7:20 PM
Unravelling the Brain with High-Density CMOS Neural Probes
Dr. Carolina Mora Lopez
Team Leader Circuits for Neural Interfaces at imec

7:20 - 7:40 PM
Neurotechnology: where engineering meets neuroscience
Dr. Hyunjoo J. Lee
Assistant Professor Electrical Engineering, KAIST

Panel: What Can Circuit Designers Do to Bolster Security in AI-driven Healthcare

7:45 - 9:00 PM
Moderator: Ingrid Verbauwhede, KU Leuven, Leuven, Belgium

Distinguished Speaker

7:45 -8:15 PM
Perspectives on Machine Learning and Cryptography By Turning Award Winner Shafi Goldwasser
Shafi Goldwasser
Professor Electrical Engineering and Computer Sciences, University of California at Berkeley, Berkeley, CA

Panelists

Alison Burdett, Sensium Healthcare, Abingdom, United Kingdom
Shafi Goldwasser, University of California at Berkeley, Berkeley, CA
Rikky Muller, University of California at Berkeley, Berkeley, CA
Sugako Otani, Renesas Electronics Corporation, Tokyo, Japan
Vivienne Sze, Massachusetts Institute of Technology, Cambridge, MA
Wenyuan Xu, Zhejiang University, Hangzhou, China

IEEE NEWS

2019 IEEE Medals & Recognitions to Be Presented at 2019 IEEE VIC Summit & Honors Ceremony

The **IEEE Vision, Innovation, and Challenges (VIC) Summit** brings together leading innovators, visionaries, and disruptors in technology to discuss, explore, and uncover what is imminent, what is possible, and what these emerging technologies mean for our future. This is a unique opportunity to connect with, learn from, and build partnerships with some of the

technology "Giants" in the world. Topics at the 2019 VIC Summit will include AI/Machine Learning, IoT/Smart Networks, Cybersecurity ... and more!

The VIC Summit culminates with the **Honors Ceremony Gala**, an evening's festivities that will include the celebration of the contributions of some of the greatest minds of our time who have made a lasting impact on society for the benefit of humanity.

Visit **http://ieee-vics.org/** for information.

For more information about the IEEE Awards Program, visit **www.ieee.org/awards** or e-mail **awards@ieee.org**.

Seeking News

Please send any chapter news or happenings (Distinguished Lecturer visits, events hosted by your SSCS chapter, awards received by members, etc) to Abira Altvater, SSCS Magazine News Editor, for inclusion in an upcoming issue of the magazine. Please email - **Abira.Altvater@ieee.org**. We look forward to receiving your news articles!

For more chapter news, check out the Fall 2018 issue of the Solid-State Circuits Magazine.