IEEE SOLID-STATE CIRCUITS SOCIETY

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February 2019

NEWS

UPCOMING WEBINAR

"Agile Hardware Design with a Generator-Based Methodology"

Presented by Prof. Elad Alon
Wednesday, March 20th, 2019
12:30 PM ET

CLICK HERE TO REGISTER

ABSTRACT: Despite the many applications that could substantially benefit from the energy-performance achievable with an SoC implemented in an advanced process technology, the high costs of designing and verifying such an SoC using current methodologies limits their adoption to end markets greater than ~$1B in size. Not only has this prevented substantial hardware innovation in emerging markets, but even in markets large enough to bear the high initial design cost, designers are being put under constant pressure to improve their productivity given increasingly tight time-to-market constraints and product cycles. In this talk, I will describe a collaborative effort to develop an "agile" approach that aims to substantially reduce

the design and verification costs of such advanced SoCs. Building on principles originally developed for agile software design, the key missing piece for hardware is that rather than focusing on developing instances, designers should focus on developing generators that facilitate re-use and enable agile validation as well as verification. As I will describe in this talk, to support this shift in approach, our team is developing technologies that enable generation of digital and analog hardware as well as the means to verify the hardware that is produced. After briefly describing each of these technologies and highlighting some of their key features, I will then briefly describe the SoC generator we have developed and used to tape-out multiple SoC demonstrators on TSMC's 16nm FFC process.

BIOGRAPHY: Elad Alon is a Professor of Electrical Engineering and Computer Sciences at the University of California at Berkeley, as well as a co-director of the Berkeley Wireless Research Center (BWRC). He is also a Co-Founder and Chief Scientist at Blue Cheetah Analog Design, which is commercializing the generator technologies described in this talk in order to enable analog/mixed-signal solutions at lower barrier to entry. He has also held advisory, consulting, or visiting positions at Ayar Labs, Locix, Lion Semiconductor, Cadence, Xilinx, Wilocity (now Qualcomm), Oracle, Intel, AMD, Rambus, Hewlett Packard, and IBM Research, where he worked on digital, analog, and mixed-signal integrated circuits for computing, test and measurement, power management, and high-speed communications. His research focuses on energy-efficient integrated systems, including the circuit, device, communications, and optimization techniques used to design them. Prof. Alon received the B.S., M.S., and Ph.D. degrees in Electrical Engineering from Stanford University in 2001, 2002, and 2006, respectively. He received the IBM Faculty Award in 2008, the 2009 Hellman Family Faculty Fund Award, as well as the 2010 and 2017 UC Berkeley Electrical Engineering Outstanding Teaching Awards, and has co-authored papers that received the 2010 ISSCC Jack Raper Award for Outstanding Technology Directions Paper, the 2011 Symposium on VLSI Circuits Best Student Paper Award, the 2012 as well as the 2013 Custom Integrated Circuits Conference Best Student Paper Awards, and 2010-2016 Symposium on VLSI Circuits Most Frequently Cited Paper Award.

Starting January 1, 2019, SSCS will be charging for CEU's and PDH's. Attendees of webinars will have to pay a fee to obtain CEU's and PDH's. However, webinar attendees can obtain a complimentary certificate of attendance.

PUBLICATIONS

The latest in SSCS Flagship Publications...

IEEE Journal of Solid-State Circuits

Vol. 54, Issue 3, March 2019

Special Section on the 2018 Custom Integrated Circuits Conference

Introduction to the Special Section on the 2018 Custom Integrated Circuits Conference Samuel Palermo ; Nan Sun
An 11-nW CMOS Temperature-to-Digital Converter Utilizing Sub-Threshold Current at Sub-Thermal Drain Voltage Teruki Someya ; A. K. M. Mahfuzul Islam ; Takayasu Sakurai ; Makoto Takamiya
A Noise-Shaped VCO-Based Nonuniform Sampling ADC With Phase-Domain Level Crossing Tzu-Fan Wu ; Mike Shuo-Wei Chen
A Compact 10-b SAR ADC With Unit-Length Capacitors and a Passive FIR Filt er Pieter Harpe
A 1-GS/s, 12-b, Single-Channel Pipelined ADC With Dead-Zone-Degenerated Ring Amplifiers Jorge Lagos ; Benjamin Poris Hershberg ; Ewout Martens ; Piet Wambacq ; Jan Craninckx
A 52-Gb/s ADC-Based PAM-4 Receiver With Comparator-Assisted 2-bit/Stage SAR ADC and Partially Unrolled DFE in 65-nm CMOS Shiva Kiran ; Shengchang Cai ; Ying Luo ; Sebastian Hoyos ; Samuel Palermo
A 56-Gb/s PAM4 Receiver With Low-Overhead Techniques for Threshold and Edge-Based DFE FIR- and IIR-Tap Adaptation in 65-nm CMOS Ashkan Roshan-Zamir ; Takayuki Iwai ; Yang-Hang Fan ; Ankur Kumar ; Hae-Woong Yang ; Lee Sledjeski ; John Hamilton ; Soumya Chandramouli ; Arlo Aude ; Samuel Palermo
A 15-Gb/s Sub-Baud-Rate Digital CDR Dongwook Kim ; Woo-Seok Choi ; Ahmed Elkholy ; Jack Kenney ; Pavan Kumar Hanumolu
A Noise Circulating Oscillator Fei Wang ; Hua Wang
A Compact Transformer-Combined Polar/Quadrature Reconfigurable Digital Power Amplifier in 28-nm Logic LP CMOS Yun Yin ; Yiting Zhu ; Liang Xiong ; Wei Luo ; Bowen Chen ; Tong Li ; Na Yan ; Hongtao Xu
A Fully Integrated Li-Ion-Compatible Hybrid Four-Level DC-DC Converter in 28-nm FDSOI Sally Safwat Amin ; Patrick P. Mercier
AC-Coupled Stacked Dual-Active-Bridge DC-DC Converter for Integrated Lithium-Ion Battery Power Delivery Yongjun Li ; Mervin John ; Yogesh Ramadass ; Seth R. Sanders
Adaptive Artificial Neural Network-Coupled LDPC ECC as Universal Solution for 3-D and 2-D, Charge-Trap and Floating-Gate NAND Flash Memories Toshiki Nakamura ; Yoshiaki Deguchi ; Ken Takeuchi
A Low-Noise Fractional- N Digital Frequency Synthesizer With Implicit Frequency Tripling for mm-Wave Applications Zhirui Zong ; Peng Chen ; Robert Bogdan Staszewski
Integrated Synthetic Fourth-Order Q -Enhanced Bandpass Filter With High

Dynamic Range, Tunable Frequency, and Fractional Bandwidth Control
Farooq Amin ; Sanjay Raman ; Kwang-Jin Koh

Design and Analysis of a DCO-Based Phase-Tracking RF Receiver for IoT Applications
Yao-Hong Liu ; Vijaya Kumar Purushothaman ; Christian Bachmann ; Robert Bogdan Staszewski

A Harmonic-Selective Multi-Band Wireless Receiver With Digital Harmonic Rejection Calibration
Hao Wu ; David Murphy ; Hooman Darabi

A Wake-Up Receiver With a Multi-Stage Self-Mixer and With Enhanced Sensitivity When Using an Interferer as Local Oscillator
Vivek Mangal ; Peter R. Kinget

A 56-GS/s 8-bit Time-Interleaved ADC With ENOB and BW Enhancement Techniques in 28-nm CMOS
Kexu Sun ; Guanhua Wang ; Qing Zhang ; Salam Elahmadi ; Ping Gui

34-GBd Linear Transimpedance Amplifier for 200-Gb/s DP-16-QAM Optical Coherent Receivers
Mostafa G. Ahmed ; Tam N. Huynh ; Christopher Williams ; Yong Wang ; Pavan Kumar Hanumolu ; Alexander Rylyakov

A 53-Gbit/s Optical Receiver Frontend With 0.65 pJ/bit in 28-nm Bulk-CMOS
Laszlo Szilagyi ; Jan Pliva ; Ronny Henker ; David Schoeniger ; Jarosław P. Turkiewicz ; Frank Ellinger

An Energy-Efficient 3.7-nV Hz Bridge Readout IC With a Stable Bridge Offset Compensation Scheme
Hui Jiang ; Stoyan Nihtianov ; Kofi A. A. Makinwa

A Time-Domain-Controlled Current-Mode Buck Converter With Wide Output Voltage Range
Jin-Gyu Kang ; Jeongpyo Park ; Min-Gyu Jeong ; Changsik Yoo

An Inductive Voltage-/Current-Mode Integrated Power Management With Seamless Mode Transition and Energy Recycling
Hesam Sadeghi Gougheri ; Mehdi Kiani

A 130-nm Ferroelectric Nonvolatile System-on-Chip With Direct Peripheral Restore Architecture for Transient Computing System
Yongpan Liu ; Fang Su ; Yixiong Yang ; Zhibo Wang ; Yiqun Wang ; Zewei Li ; Xueqing Li ; Ryuji Yoshimura ; Takashi Naiki ; Takashi Tsuwa ; Takahiko Saito ; Zhongjun Wang ; Koji Taniuchi ; Huazhong Yang

Bitline Charge-Recycling SRAM Write Assist Circuitry for VMIN Improvement and Energy Saving
Hanwool Jeong ; Se Hyeok Oh ; Tae Woo Oh ; Hoonki Kim ; Chang Nam Park ; Woojin Rim ; Taejoong Song ; Seong-Ook Jung

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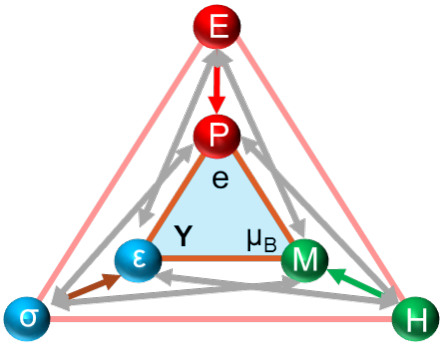
IEEE Journal on Exploratory Solid-State Computational Devices and Circuits

Volume 4, 2018



Circuit Models for Spintronic Devices Subject to Electric and Magnetic Fields
Meshal Alawein ; Hossein Fariborzi

Complementary Logic Implementation for Antiferromagnet Field-Effect Transistors
Chenyun Pan ; Azad Naeemi

Evaluation of Operating Margin and Switching Probability of Voltage- Controlled Magnetic Anisotropy Magnetic Tunnel Junctions
Jeehwan Song ; Ibrahim Ahmed ; Zhengyang Zhao ; Delin Zhang ; Sachin S. Sapatnekar ; Jian-Ping Wang ; Chris H. Kim

Towards a Strong Spin-Orbit Coupling Magnetoelectric Transistor
Peter A. Dowben ; Christian Binek ; Kai Zhang ; Lu Wang ; Wai-Ning Mei ; Jonathan P. Bird ; Uttam Singisetti ; Xia Hong ; Kang L. Wang ; Dmitri Nikonov

Using Programmable Graphene Channels as Weights in Spin-Diffusive Neuromorphic Computing
Jiaxi Hu ; Gordon Stecklein ; Yoska Anugrah ; Paul A. Crowell ; Steven J. Koester

BCB Evaluation of High-Performance and Low-Leakage Three-Independent-Gate Field Effect Transistors
Jorge Romero-Gonzalez ; Pierre-Emmanuel Gaillardon

Tunnel FET Analog Benchmarking and Circuit Design
Hao Lu ; Paolo Paletti ; Wenjun Li ; Patrick Fay ; Trond Ytterdal ; Alan Seabaugh

Improving Energy Efficiency of Low Voltage Logic by Technology-Driven Design
Kaushik Vaidyanathan ; Daniel H. Morris ; Uygar E. Avci ; Huichu Liu ; Tanay Karnik ; Hong Wang ; Ian A. Young

Inversion Charge Boost and Transient Steep-Slope Induced by Free-Charge-Polarization Mismatch in a Ferroelectric-Metal-Oxide-Semiconductor Capacitor
Sou-Chi Chang ; Uygar E. Avci ; Dmitri E. Nikonov ; Ian A. Young

Performance Characterization and Majority Gate Design for MESO-Based Circuits
Zhaoxin Liang ; Meghna G. Mankalale ; Jiaxi Hu ; Zhengyang Zhao ; Jian-Ping Wang ; Sachin S. Sapatnekar

JxCDC papers listed in order of popularity can be found online HERE.

For paper submission details, click HERE.

IEEE Solid-State Circuits Letters

Volume 1, Issue 7, July 2018

A 180 mV 81.2%-Efficient Switched-Capacitor Voltage Doubler for IoT Using Self-Biasing Deep N-Well in 16-nm CMOS FinFET
Yu-Tso Lin ; Naser Pourmousavian ; Chao-Chieh Li ; Min-Shueh Yuan ; Chih-Hsien Chang ; Robert Bogdan Staszewski

A 0.01-mm2 Mostly Digital Capacitor-Less AFE for Distributed Autonomous Neural Sensor Nodes
Jiannan Huang ; Farah Laiwalla ; Jihun Lee ; Lingxiao Cui ; Vincent Leung ; Arto Nurmikko ; Patrick P. Mercier

A Fully Packaged 130-GHz QPSK Transmitter With an Integrated PRBS Generator
Mahmoud Sawaby ; Nemat Dolatsha ; Baptiste Grave ; Cheng Chen ; Amin Arbabian

±0.5 V 15 u W Recycling Folded Cascode Amplifier With 34767 MHz·pF/mA FOM
Jose M. Algueta-Miguel ; Antonio Lopez-Martin ; M. Pilar Garde ; Carlos A. De La Cruz ; Jaime Ramirez-Angulo

A 1.1-pJ/cycle, 20-MHz, 0.42-V Temperature Compensated ARM Cortex-M0+ SoC With Adaptive Self Body-Biasing in FD-SOI

Guénolé Lallement ; Fady Abouzeid ; Jean-Marc Daveau ; Philippe Roche ; Jean-Luc Autran

EDUCATION

March 2019 Distinguished Lectures

SSCS Macau	Ultra-Low-Power DTC-Based Fractional-N-Digital PLL Techniques - Presented by Kenichi Okada	March 5, 2019	University of Macau **For more information, please click here**

CONFERENCES

Upcoming SSCS-Sponsored Conferences

2019 Design, Automation & Test in Europe Conference and Exhibition Florence, Italy	**March 25 - 29, 2019**
2019 IEEE Custom Integrated Circuits Conference (CICC) Austin, Texas	**April 14 - 17, 2019**
2019 International Symposium on VLSI Design, Automation and Test (VLSI-DAT) Hsinchu, Taiwan	**April 22 - 25, 2019**
2019 International Symposium on VLSI Technology, Systems, and Application (VLSI-TSA) Hsinchu, Taiwan	**April 22 - 25, 2019**
2019 IEEE Radio Frequency Integrated Circuits Symposium (RFIC) Boston, Massachusetts	**June 2 - 4, 2019**
2019 Symposium on VLSI Circuits Kyoto, Japan	**June 9 - 14, 2019**
2019 IEEE Hot Chips 31 Symposium (HCS) Cupertino, California	**August 18 - 29, 2019**
ESSCIRC 2019 - IEEE 45th European Solid-State Circuits Conference (ESSCIRC) Cracow, Poland	**September 23 - 26, 2019**
2019 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS) Nashville, Tennessee	**November 3 - 6, 2019**

SSCS-Sponsored Conferences: Proceedings

Click the links below to access 2018 SSCS-Sponsored conference

proceedings.

2018 IEEE International Solid-State Circuits Conference (ISSCC)
2018 IEEE Custom Integrated Circuits Conference (CICC)
2018 IEEE Symposium on VLSI Circuits (VLSI)
2018 IEEE 44th European Solid-State Circuits Conference (ESSCIRC)
2018 IEEE Asian Solid-State Circuits Conference

DATE 2019 in Florence: Advance Program now Available

View the advance program here: https://www.date-conference.com/programme

The DATE conference will take place from 25 to 29 March 2019 at the Firenze Fiera in Florence, Italy. It combines the world's favorite electronic systems design and test conference with an international exhibition for electronic design, automation and test, from system-level hardware and software implementation right down to integrated circuit design.

On the first day of the DATE week, six in-depth technical tutorials on the main topics of DATE as well as two industry hands-on tutorials will be given by leading experts in their respective fields. The topics cover Machine Learning for Manufacturing and Test, OpenCL Design Flows for FPGAs, Approximate Computing, Hardware-based Security, Co-simulation, and Safety and Security in Automotive, while the hands-on tutorials are on Quantum Computing with IBM Q and on Python Productivity for Xilinx Zynq.

During the Opening Ceremony on Tuesday, plenary keynote lectures will be given by Kenneth P. Caviasca, Vice President of Internet of Things Group and General Manager of Architecture, Silicon and Platform Engineering at Intel, and Jürgen Bortolazzi, Director Driver Assistance Systems at Porsche. On the same day, the Executive Track offers a series of business panels with executive speakers from companies leading the design and automation industry, discussing hot topics. Furthermore, a talk by Claudio Giorgione, Curator of the Leonardo Department at the National Museum of Science and Technology Milano, will give insight into live and work of Leonardo da Vinci in line with the 500th anniversary of his death, which is celebrated in Florence in 2019.

The main conference programme from Tuesday to Thursday includes 58 technical sessions organized in parallel tracks from the four areas:

D - Design Methods & Tools
A - Application Design
T - Test, Reliability, and Robustness
E - Embedded and Cyber-physical Systems

and from several special sessions on Hot Topics, such as Emerging Design Technologies, Design and Test of Secure Systems, IoT Security, Embedded Systems for Deep Learning, Augmented Living and Personalized Healthcare, Robotics and Industry 4.0., as well as results and lessons learned from European projects. Additionally, there are numerous Interactive Presentations which are organized into five IP sessions.

Two Special Days in the programme will focus on areas bringing new challenges to the system design community: Embedded Meets Hyperscale and HPC and Model-Based Design of Intelligent Systems. Each of the Special Days will have a full programme of keynotes, panels, tutorials and technical presentations.

Heterogeneous computing with multiple, specialized processors and application-specific accelerators is vital for embedded systems to meet performance, latency, and efficiency targets. The same goals of fast, efficient, and cost-effective processing are also gating factors for the evolution of hyperscale data center (DC) and high-performance computing (HPC) and Moore's

law no longer provides the necessary efficiency gains. The theme of the special day Embedded Meets Hyperscale and HPC is to highlight this confluence of methods and technologies to better understand, how heterogeneous computing is shaping the future of hyperscale DCs and HPC.

The special day on Model-Based Design of Intelligent Systems will explore all that is needed to lift model-based design into the era of intelligent systems. Topics addressed are, among others, model-based design frameworks for IoT systems, model-based machine learning, and application of model-based design in safety-critical and autonomous systems. The special day will also highlight the upcoming challenges in this domain and invite the DATE community to help overcome them.

To inform attendees on commercial and design-related topics, there will be a full programme in the Exhibition Theatre which will combine presentations by exhibiting companies, best-practice reports by industry leaders on their latest design projects and selected conference special sessions. Two of the highlights here will be a career session called Inspiring Futures!,where interested companies may introduce their work and job portfolios, and the newly created Publisher's Session.
The conference is complemented by an exhibition, running for three days (Tuesday - Thursday), including exhibition booths from companies, and collaborative research initiatives including EU project presentations.The exhibition provides a unique networking opportunity and states the perfect venue for industries to meet University Professors to foster University Programme and especially for PhD Students to meet future employers.

On Friday, 10 full-day workshops cover several hot topics from areas like (a) Open Source and Machine Learning in EDA, (b) Emerging Techniques for Memories, Interconnections, and Quantum Computing, (c) Hardware Design, Synthesis, and Approximate Computing, as well as EDA in application domains such as (d) Autonomous Systems and IoT.

For further information please visit: **www.date-conference.com**

IEEE Radio Frequency Integrated Circuits Symposium

2-4 June 2019

Boston, Massachusetts

The **2019 IEEE Radio Frequency Integrated Circuits Symposium (RFIC 2019)** will be held in Boston, MA on 2-4 June 2019. The RFIC Symposium is an annual IEEE conference that is combined with the International Microwave Symposium (IMS), ARFTG, and the Industry Exhibition to form the "Microwave Week", the largest worldwide RF/microwave technical meeting of the year. In 2019, the conference will also extend its focus to emerging circuit technologies related to RFIC, such as MEMS sensors and actuators, heterogeneous and 3D ICs, silicon photonics, biomedical applications, quantum computing and more. We cordially invite you to participate in this international symposium.

To encourage student attendance, the IMS'19 is offering deep registration discounts and numerous benefits for student volunteers who are IEEE members and willing to help with conference activities. For more details, visit **https://ims-ieee.org/students-main/student-volunteers.**

For 2019, RFIC is promoting a new educational experience for the attendees: a "Technical Lecture" comprising a 1 ½ hour interactive short course delivered by a distinguished speaker during lunchtime on Sunday, between the AM and PM workshops. For 2019, Prof. Ali Niknejad from University of California, Berkeley, will teach "Fundamentals of mmWave IC Design in CMOS".

The 2019 RFIC Symposium will begin on Sunday, June 2nd 2019, with 12 RFIC focused workshops and one technical lecture. In addition, there will be several joint RFIC/IMS workshops on Sunday and Monday. These workshops cover a wide range of advanced topics in RFIC technology and IC design, including power amplifiers, 5G systems, silicon photonics, quantum computing, hardware security, and beyond. The 2019 RFIC Plenary Session on Sunday will conclude the day with two visionary plenary talks: Dr. Greg Henderson, Senior Vice President,

Automotive, Communications and Aerospace/Defense at Analog Devices, will outline "The Digital Future of RFICs", and Dr. Ir. Michael Peeters, Program Director Connectivity and Humanized Technology at IMEC, will address the question "Do the networks of the future care about the materials of the past?". Immediately after the plenary session, the RFIC reception will follow, with highlight from our industry showcase and student paper finalists in an engaging social and technical evening event supported by the RFIC Symposium corporate sponsors. You will not want to miss the RFIC reception!

On Monday and Tuesday, the RFIC Symposium will have multiple tracks of oral technical paper sessions. The 5G Summit technical sessions on Tuesday afternoon will provide high-level 5G overview presentations that will complement the 5G-focused RFIC technical sessions on Tuesday morning. Two enlightening panels will be featured during lunchtime on both days: "The Internet of Things (IoT) - back to the future, or no future?" on Monday and "Will Artificial Intelligence (AI) and Machine Learning (ML) take away my job as an RF/Analog Designer?" on Tuesday.

On behalf of the RFIC Steering and Executive Committees, we welcome you to join us at the 2019 RFIC Symposium in Boston, Massachusetts! Please visit the RFIC 2019 website **(http://rfic-ieee.org/)** for more details and updates.

Call for Participation:

VLSI Technology, Systems, and Applications
VLSI Design, Automation and Test
22-25 April 2019
Hsinchu, Taiwan

REGISTER NOW!

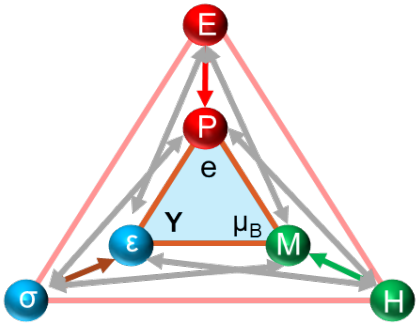
VLSI-TSA https://expo.itri.org.tw/2019vlsitsa	VLSI-DAT https://expo.itri.org.tw/2019vlsidat
• 40 Selected Top Papers • 4 Special Sessions on - Silicon Photonics, Low Dimensional Devices and Materials, 3D/Heterogeneous Integration and Unconventional Manufacturing, Machine Learning for the Semiconductor Industry • **2 Profound Short Courses** • Best Student Paper Award	• 36 Selected Top Papers • 3 Special Sessions on - Advanced AI Chips and Applications, Silicon Photonics for Next Generation Chips, Heterogeneous Integration/Flexible Hybrid Electronics • 2 Industrial Sessions • **3 Profound Tutorials** • Best Paper Award

Joint Program Highlights

- Six Plenary Talks by Ghavam Shahidi, IBM Research ; Li Fung Chang, Industrial Technology Research Institute ; Winfried Kaiser, Carl Zeiss SMT GmbH ; Peter Hsieh, ARM ; Thomas Ernst, CEA-LETI ; Mike Davies, Intel
- Two Luncheon Keynotes by H-S. Philip Wong, Vice President of Corporate Research, TSMC ;Owain Vaughan, Chief Editor of Nature Electronics
- Two Joint Special Sessions on (5G: From Systems to Device) and (Future of Memory: From Storage to Computing)

CALL FOR PAPERS

CALL FOR PAPERS



IEEE Journal on Exploratory Solid-State Computational Devices and Circuits

Special Issue on "Ferroelectric Transistors for Advanced Logic, Analog, and Memory Applications"

Guest Editor
Azad Naeemi, Georgia Institute of Technology, azad@ece.gatech.edu

Editor-in-Chief
Ian Young, Intel, ian.young@intel.com

Aims and Scope
With recent advancements in the growth and processing of ferroelectric materials and the emergence of CMOS compatible ferroelectrics, major research and development efforts are underway on ferroelectric transistors for logic, analog, and memory applications. With CMOS scaling facing challenges in improving energy efficiency and power density, research in this area is needed to augment the CMOS technology by lowering the required supply voltage or adding new features and functionalities, such as non-volatility or reconfigurability. Ferroelectric transistors also show great promise for non-traditional circuits, such as convolutional and spiking neural networks and in-memory computing. Research in this area spans many levels of abstraction: from fundamental physical properties and material processing and characterization, to various device concepts, and to circuit and system design and benchmarking.

This special issue of the IEEE JXCDC will present the most recent developments in the area of ferroelectric transistors based on experiments and theoretical models. It aims to feature original papers on various aspects of this emerging technology, its challenges and opportunities, its intrinsic versus practical limits, and the circuits and systems it may enable.

Topics of Interest include but are not limited to:

1. Advanced logic devices, such as negative capacitance transistors (NCFETs).
2. Memory devices, such as single- and multi-state ferroelectric transistors and ferroelectric tunnel junctions.
3. Analog devices, such as binary, multistate, or continuous synapses and oscillatory devices.
4. Ferroelectric switching coupled to other computing variables, such as ferromagnetic, anti-ferromagnetic, and strain.
5. Circuit- and system-level design and performance evaluation with ferroelectric devices.
6. Emerging circuit and system concepts, such as convolutional and spiking neural networks, coupled oscillators, in-memory computing, and instant-on circuits.

Important Dates:
Open for Submission: Feb 15th, 2019
Submission Deadline: April 30th, 2019
First Notification: May 15th, 2019
Revision Submission: June 15th, 2019
Final Decision: July 15th, 2019
Publication Online: August 1st, 2019

Submission Guidelines:
The IEEE Journal on Exploratory Solid-State Computational Devices and Circuits (J XCDC) IS AN OPEN ACCESS PUBLICATION: The Open Access Fee is: $1,350 USD per article.Article submissions must be done through the ScholarOne Manuscripts website: **https://mc.manuscriptcentral.com/jxcdc**.

Inquiries for the JxCDC Journal should be sent to: JXCDC@IEEE.ORG.

ESSCIRC/ESSDERC 2019: Call for Papers

European Solid-State Device Research Conference
European Solid-State Circuits Conference
September 23-26, 2019
Cracow, Poland

The aim of ESSDERC and ESSCIRC is to provide an annual European forum for the presentation and discussion of recent advances in solid-state devices and circuits. The level of integration for system-on-chip design is rapidly increasing. This is made available by advances in semiconductor technology. Therefore, more than ever before, a deeper interaction among technologists, device experts, IC designers and system designers is necessary. While keeping separate Technical Program Committees, ESSDERC and ESSCIRC are governed by a common Steering Committee and share Plenary Keynote Presentations and Joint Sessions bridging both communities. Attendees registered for either conference are encouraged to attend any of the scheduled parallel sessions, regardless to which conference they belong.

Although not limited, papers are solicited for the following main topics:

ESSCIRC

Analog
OP-Amps and instrumentation amplifiers; CT and DT filters; SC circuits, Comparators; Voltage and current references; High voltage circuits; Nonlinear analog circuits; Digitally assisted analog circuits.

Data Converters
Nyquist-rate and oversampling A/D and D/A converters; Sample-hold circuits; Time-to-digital converters; ADC and DAC calibration/error correction circuits.

RF and mm-Wave
RF/IF building blocks like LNAs, mixers, power amplifiers, IF amplifiers; Power detectors; Subsystems for RF, mm-wave and THz design.

Frequency Generation
Modulators/demodulators; VCOs; PLLs; DLLs; Frequency synthesizers; Frequency dividers; Integrated passive components.

Wireless and Wireline Systems
Receivers/transmitters/transceivers for wireless/wireline systems Gigabit serial links; Clock and data recovery; Equalization; Advanced modulation systems; Base station and handset applications; TV/radio/satellite receivers and transmitters; Radars.

Sensors, Imager and Biomedical
Sensor subsystems and interfaces; Accelerometers; Temperature sensing; Imaging and smart imaging chips; AMOLED; MEMs subsystems; RF MEMs; Implantable electronic ICs; Biomedical imagers; Bio-MEMs integrated systems; Lab-on-chip; Organic LED and liquid-crystal-display interface circuits; Flat panel and projection display.

Digital, Security and Memory
Techniques for energy efficient and high performance digital circuits; I/O and inter-chip communication; Reconfigurable digital circuits; Security and encryption circuits; Clocking; Arithmetic building blocks; Memories; Microprocessors; DSPs; Memory interfacing; Bus interfacing; Many core and multirate ICs; 3D integration.

Power Management
Energy transducers; Power regulators; DC-DC converters; Energy scavenging circuits; LDOs Boost-buck-converters; LED and gate drivers; Sequencers and supervisors; Green circuits.

ESSDERC

CMOS Devices and Technology
CMOS scaling; Novel MOS device architectures; Circuit/device interaction and co-optimization; High-mobility channel devices; CMOS front-end or back-end processes; Interconnects; Integration of RF or photonic devices; 3D integration; Front-end and back-end manufacturing processes; 3D integration and wafer-level packaging; Reliability and characterization of materials, processes and devices; Advanced interconnects; ESD, latch-up, soft errors, noise and mismatch behavior, hot carrier effects, bias temperature instabilities, and EMI; Defect monitoring and control; Metrology; Test structures and methodologies; Manufacturing yield modeling, analysis and testing.

Opto-, Power and Microwave Devices
New device or process architectures; New phenomena and performance improvement of optoelectronic, high voltage, smart power, IGBT, microwave devices; Passive devices, antennas and filters (including Si, Ge, SiC, GaN); Optoelectronic devices including sensors, LEDs, semiconductor lasers; Photovoltaic devices; Studies of high temperature operation; IC cooling and packaging aspects; Reliability and characterization of materials, processes and devices.

Physical Modeling of Materials and Devices
Numerical, analytical and statistical modeling and simulation of electronic, optical or hybrid devices, the interconnect, isolation and 2D or 3D integration; Aspects of materials, fabrication processes and devices, e.g. advanced physical phenomena (quantum mechanical and non-stationary transport phenomena, ballistic transport, and other related aspects); Mechanical or electro-thermal modeling and simulation; DfM. Reliability of materials and devices.

Compact Modeling of Devices and Circuits
Compact/SPICE modeling of electronic, optical, organic, and hybrid devices and their IC implementation and interconnection. Topics include compact/SPICE models and their Verilog-A standardization of the semiconductor devices (including Bio/Med sensors, MEMS, Microwave, RF, High voltage and Power), parameter extraction, compact models for emerging technologies and novel devices, performance evaluation, reliability, variability, and open source benchmarking/implementation methodologies. Modeling of interactions between process, device, and circuit design as well as Foundry/Fabless Interface Strategies.

Memory Devices and Technology
Embedded and stand-alone memories; DRAM, FeRAM, MRAM, ReRAM, PCRAM, Flash, Nanocrystal and single/few-electron memories, Organic memories, NEMS-based devices, Selectors; Novel memory cell concepts and architectures, covering device physics, reliability, process integration and manufacturability issues and including 3D NAND Flash, crosspoint arrays, and 3D systems integration; Devices and concepts for neuromorphic computing, memory-enabled logic and security applications.

Emerging non-CMOS Devices and Technologies
Novel non-CMOS materials, processes and devices, (carbon nanotubes, nanowires and nanoparticles, 2D materials, graphene, metal oxides, etc.) for electronic, optoelectronic, sensor & actuator applications; Reliability and characterization of materials, processes and devices; Molecular and quantum devices; Nanophotonics, plasmonics, spintronics, selfassembling methods; Energy harvesters; High frequency digital and analog devices including THz; New high-mobility channels (strained Si, Ge, SiGe).

Sensor Devices and Technology
Design, fabrication, modeling, reliability, packaging and smart systems integration of actuators (discrete SoC, SiP, or heterogenous 3D integration); MEMS, NEMS, optical, chemical or biological sensors; Display technologies; High-speed imagers; TFTs; Organic and flexible substrate electronics.

POST-CONFERENCE PUBLICATIONS

All accepted ESSDERC and ESSCIRC papers will be included in the conference proceedings and posted on IEEE Xplore after the conference.

Co-publication of qualified papers in SSC-L
Upon acceptance, outstanding ESSCIRC papers will be invited to submit to a Special Issue of IEEE Solid-State Circuit Letters (SSC-L, 4 pages format) on the ESSCIRC, subject to additional editorial and quality reviews. Publication on IEEE Xplore of the SSC-L Special Issue is timed to be September 1, 2019

Special JSSC issue
Authors of outstanding papers will be invited to submit their work to a Special Issue of IEEE Journal of Solid-State Circuits (JSSC, up to 10-12 pages format) on the ESSCIRC to appear in July 2020, with an opportunity to provide additional material, such as mathematical analysis, in-depth circuit description, more experimental results and benchmarking data.

Special J-EDS issue
Authors of selected outstanding ESSDERC papers will be invited to submit their work to the special issue of IEEE Journal of the Electron Devices Society. The authors will be asked to revise the conference version of the paper by adding at least 30% new material. All manuscripts will undergo additional editorial and quality review process.

IMPORTANT INFORMATION
Manuscript guidelines as well as instructions on how to submit electronically will be available on the **conference website**. Papers must not exceed four A4 pages with all illustrations and references included.

Key Dates:

Paper submission Deadline: April 8th, 2019
Paper Selection Meeting: May 20th, 2019
Notification of Acceptance: May 31st, 2019
Early Registration Start: June 3rd, 2019

BioCAS 2019 : Call for Papers

Biomedical Circuits and Systems Conference

October 17 - 19, 2019

Nara, Japan

BioCAS 2019 is a premier international forum for presenting the interdisciplinary research and development activities at the crossroads of medicine, life sciences, physical sciences and engineering that shape tomorrow's medical devices and healthcare systems.

This conference brings together members of our communities to broaden their knowledge in emerging areas of research at the interface of the life sciences and the circuits and systems engineering. The three-day single-track program for BioCAS 2019 is multidisciplinary in topics including but not limited to:

Biomedical Technologies:
* Assistive, Rehabilitation, and Quality of Life Technologies
* Biofeedback, Neuromodulation, and Closed-Loop Systems
* Bio-Inspired and Neuromorphic Circuits and Systems
* Biosensor Devices and Interface Circuits
* Biotelemetry and Energy Harvesting/Scavenging Circuits and Systems
* Body Area/Sensor Network and Wireless/Wearable Health Monitoring
* Electronics for Neuroscience
* Implantable Medical Electronics
* Lab-on-Chip and BioMEMS
* Point-of-Care Technologies for Healthcare

Biomedical Applications:
* Biomedical Imaging and Image Processing
* Biosignal Recording, Processing, and Machine Learning
* Human-Machine Interfaces
* Medical Information Systems and Bioinformatics

Submission Guidelines:
The complete 4-page paper (in standard IEEE double-column format), including the title, authors' names, affiliations and e-mail addresses, as well as a short abstract and an optional demonstration video link (3 minute max) are requested. Papers must be submitted electronically in PDF format through **www.biocas2019.org.**

Important Dates:
Monday, April 22, 2019 - Special Session Proposal Deadline
Monday, June 10, 2019 - Regular Paper Submission Deadline
Monday, July 15, 2019 - Live Demo Submission Deadline
Monday, August 12, 2019 - Author Notification Date
Sunday, September 15, 2019 - Final Paper Submission Deadline

UPCOMING EVENTS

The following courses may be of interest to IEEE SSCS Members:

Novel Power Converters for DC Fast Charging - Monday, March 4, 2PM-3:30PM EDT - **CLICK HERE TO REGISTER**

Integrated PV/Smart-grid Based Charging Applications, Monday, March 11, 2PM-3:30PM EDT - **CLICK HERE TO REGISTER**

IEEE NEWS

2019 IEEE Medals & Recognitions to Be Presented at 2019 IEEE VIC Summit & Honors Ceremony

The **IEEE Vision, Innovation, and Challenges (VIC) Summit** brings together leading innovators, visionaries, and disruptors in technology to discuss, explore, and uncover what is imminent, what is possible, and what these emerging technologies mean for our future. This is a unique opportunity to connect with, learn from, and build partnerships with some of the technology "Giants" in the world. Topics at the 2019 VIC Summit will include AI/Machine Learning, IoT/Smart Networks, Cybersecurity ... and more!

The VIC Summit culminates with the **Honors Ceremony Gala**, an evening's festivities that will include the celebration of the contributions of some of the greatest minds of our time who have made a lasting impact on society for the benefit of humanity.

Visit **http://ieee-vics.org/** for information.

For more information about the IEEE Awards Program, visit **www.ieee.org/awards** or e-mail **awards@ieee.org**.

Seeking News

Please send any chapter news or happenings (Distinguished Lecturer visits, events hosted by your SSCS chapter, awards received by members, etc) to Abira Altvater, SSCS Magazine News Editor, for inclusion in an upcoming issue of the magazine. Please email - **Abira.Altvater@ieee.org**. We look forward to receiving your news articles!

For more chapter news, check out the Winter 2019 issue of the Solid-State Circuits Magazine.