IEEE SOLID-STATE CIRCUITS SOCIETY

Where ICs are in IEEE

December 2019

UPCOMING SSCS WEBINAR

Electronic-Photonic Co-Design: From Communication to Optical Phase Control

Presenter: Prof. Firooz Aflatouni, University of Pennsylvania
Thursday, January 16th, 2020
12:00 PM ET (New York)

Abstract: Integrated electronic-photonic co-design can profoundly impact both fields resulting in advances in several areas such as energy-efficient communication, signal processing, imaging, and sensing. Examples of integrated electronic-photonic co-design may be categorized into two groups: (a) electronic assisted photonics, where integrated analog, RF, mm-wave, and THz circuits are employed to improve the performance of photonic systems, and (b) photonic assisted electronics, where photonic systems and devices are used to improve the performance of integrated RF, mm-wave, and THz systems. In this talk, examples of electronic-photonic co-design such as optical synthesis and low power laser stabilization will be presented.

Bio: Firooz Aflatouni received the Ph.D. degree in Electrical Engineering from the University of Southern California, Los Angeles, in 2011. He was a post-doctoral scholar in the Department of Electrical Engineering at the California Institute of Technology before joining the University of Pennsylvania in 2014 where he is Skirkanich Assistant Professor in the Department of Electrical and Systems Engineering. His research interests include electronic-photonic co-design and low power RF and mm-wave integrated circuits. In 1999, he co-founded Pardis Bargh Company where he served as the CTO for five years working on design and manufacturing of inclined-orbit satellite tracking systems. From 2004 to 2006, he was a Design Engineer with MediaWorks Integrated Circuits Inc., Irvine, CA. Firooz received the Young Investigator Program (YIP) Award from the Office of Naval Research in 2019, the NASA Early Stage Innovation Award in 2019, the 2015 IEEE Benjamin Franklin Key Award, 2011 USC Department of Electrical Engineering best Ph.D. thesis award, and 2010 NASA Tech Award for his work on development of a

Ka-Band SiGe receiver MMIC for space transponder applications.

CLICK HERE TO REGISTER

NEWS

SSCS Members Elevated to Fellow in 2020

Congratulations to the SSCS Members who were elevated to Fellow in 2020.

For more information on the elevated SSCS members, **click here**. To view the full class of IEEE Fellows elevated in 2020, **click here**.

William Bidermann
For leadership in commercially successful image sensors and microprocessors

Ramon Carvajal
For contributions to low-voltage and low-power CMOS analog circuit design

Barbara De Salvo
For contributions to device physics of nonvolatile embedded and stand-along memories

Jose De La Rosa
For contributions to delta-sigma modulators

Pavan Kumar Hanumolu
For contributions to the design of mixed-signal integrated circuits

Eric A M Klumperink
For contributions to thermal noise canceling and software-defined radio architecture

Yiannos Manoli
For contributions to the design of integrated analog-to-digital interface circuits and energy harvesting systems

Bich-yen Nguyen
For contributions to silicon on insulator technology

Michael Perrott
For contributions to phase-locked loop integrated circuits

Ulrich Pfeiffer
For development of silicon-based millimeter-wave and terahertz circuits and systems

Jae-sung Rieh
For contributions to silicon-germanium integrated circuits for wireless communications

Ravi Todi
For contributions to innovative design and commercialization of high performance eDRAM

Huazhong Yang
For low-power circuit techniques for sensor applications and design automation

Masoud Zargari
For contributions to the development of CMOS radio-frequency integrated circuits

2019-2020 Circuit Analysis & Design Contest

Calling all students!

2019-2020 CIRCUIT ANALYSIS & DESIGN CONTEST
This contest involves solving a thought-provoking circuit analysis and design problem. Submissions are solicited by undergraduate and graduate students who are currently enrolled in a college or university. Win up to $2K towards entering an SSCS-sponsored conference. **Click here for more information** on contest eligibility, how to enter, and more. **Submission Deadline: January 15, 2020 - EXTENDED DEADLINE!**

SSCS YouTube Channel

SSCS now has a YouTube Channel where all CONFedu videos are posted including VLSIx 2016, CICCx 2017, ISSCCedu 2018, and ESSCIRCedu 2018.

Now Available: CICCedu 2019 and VLSIedu 2019.

Call for Papers for NEW IEEE Open Journal of Solid-State Circuits

IEEE SSCS is now accepting paper submissions for its new gold fully open access **IEEE Open Access Journal of Solid-State Circuits**, spanning the full scope of the SSCS' fields of interest. The new journal will have an independent editorial board, established peer-review process, and will be fully compliant with funder mandates, including Plan S. SSCS members receive a discount on Article Processing Charges. For more information or to submit a paper, **click here.**

PUBLICATIONS

The latest in SSCS Flagship Publications...

IEEE Journal of Solid-State

Circuits

Vol. 55, Issue 1, January 2020

Special Issue on the 2019 IEEE International Solid-State Circuits Conference (ISSCC)

A 28-nm Automotive Flash Microcontroller With Virtualization-Assisted Processor Supporting ISO26262 ASIL D
Hiroyuki Kondo ; Sugako Otani ; Norimasa Otsuki ; Yasufumi Suzuki ; Naoto Okumura ; Shohei Maeda ; Tomonori Yanagita ; Takao Koike ; Kosuke Yayama ; Yasuhisa Shimazaki ; Masao Ito ; Minoru Uemura ; Toshihiro Hattori ; Noriaki Sakamoto

A 2 × 30k-Spin Multi-Chip Scalable CMOS Annealing Processor Based on a Processing-in-Memory Approach for Solving Large-Scale Combinatorial Optimization Problems
Takashi Takemoto ; Masato Hayashi ; Chihiro Yoshimura ; Masanao Yamaoka

A 7.5 Gb/s/pin 8-Gb LPDDR5 SDRAM With Various High-Speed and Low-Power Techniques
Kyung-Soo Ha ; Chang-Kyo Lee ; Dongkeon Lee ; Daesik Moon ; Hyong-Ryol Hwang ; Dukha Park ; Young-Hwa Kim ; Young Hoon Son ; Byongwook Na ; Seungseob Lee ; Youn-Sik Park ; Hyuck-Joon Kwon ; Tae-Young Oh ; Young-Soo Sohn ; Seung-Jun Bae ; Kwang-Il Park ; Jung-Bae Lee

A 1.1-V 10-nm Class 6.4-Gb/s/Pin 16-Gb DDR5 SDRAM With a Phase Rotator-ILO DLL, High-Speed SerDes, and DFE/FFE Equalization Scheme for Rx/Tx
Dongkyun Kim ; Minsu Park ; Sungchun Jang ; Jun-Yong Song ; Hankyu Chi ; Geunho Choi ; Sunmyung Choi ; Changhyun Kim ; Minsik Han ; Kibong Koo ; Yongmi Kim ; Dong Uk Lee ; Jaein Lee ; Kihun Kwon ; Byeongchan Choi ; Hongjung Kim ; Sanghyun Ku ; Jongsam Kim ; Seungwook Oh ; Dain Im ; Yongsung Lee ; Mingyu Park ; Jonghyuck Choi ; Junhyun Chun ; Kyowon Jin

A 1.33-Tb 4-Bit/Cell 3-D Flash Memory on a 96-Word-Line-Layer Technology
Noboru Shibata ; Kazushige Kanda ; Takahiro Shimizu ; Jun Nakai ; Osamu Nagao ; Naoki Kobayashi ; Makoto Miakashi ; Yasushi Nagadomi ; Tomoaki Nakano ; Takahisa Kawabe ; Taira Shibuya ; Mario Sako ; Kosuke Yanagidaira ; Toshifumi Hashimoto ; Hiroki Date ; Manabu Sato ; Tomoki Nakagawa ; Junji Musha ; Takatoshi Minamoto ; Mizuki Uda ; Dai Nakamura ; Katsuaki Sakurai ; Takahiro Yamashita ; Jieyun Zhou ; Ryoichi Tachibana ; Teruo Takagiwa ; Takahiro Sugimoto ; Masatsugu Ogawa ; Yusuke Ochi ; Kazuaki Kawaguchi ; Masatsugu Kojima ; Takeshi Ogawa ; Tomoharu Hashiguchi ; Ryo Fukuda ; Masami Masuda ; Koichi Kawakami ; Tadashi Someya ; Yasuyuki Kajitani ; Yuuki Matsumoto ; Jumpei Sato ; Namasivayam Raghunathan ; Yee Lih Koh ; Shuo Chen ; Juan Lee ; Hiroaki Nasu ; Hiroshi Sugawara ; Koji Hosono ; Toshiki Hisada ; Hiroshi Nakamura

A Twin-8T SRAM Computation-in-Memory Unit-Macro for Multibit CNN-Based AI Edge Processors
Xin Si ; Jia-Jing Chen ; Yung-Ning Tu ; Wei-Hsing Huang ; Jing-Hong Wang ; Yen-Cheng Chiu ; Wei-Chen Wei ; Ssu-Yen Wu ; Xiaoyu Sun ; Rui Liu ; Shimeng Yu ; Ren-Shuo Liu ; Chih-Cheng Hsieh ; Kea-Tiong Tang ; Qiang Li ; Meng-Fan Chang

Embedded 1-Mb ReRAM-Based Computing-in- Memory Macro With Multibit Input and Weight for CNN-Based AI Edge Processors
Cheng-Xin Xue ; Wei-Hao Chen ; Je-Syu Liu ; Jia-Fang Li ; Wei-Yu Lin ; Wei-En Lin ; Jing-Hong Wang ; Wei-Chen Wei ; Tsung-Yuan Huang ; Ting-Wei Chang ; Tung-Cheng Chang ; Hui-Yao Kao ; Yen-Cheng Chiu ; Chun-Ying Lee ; Ya-Chin King ; Chrong-Jung Lin ; Ren-Shuo Liu ; Chih-Cheng Hsieh ; Kea-Tiong Tang ; Meng-Fan Chang

IEEE Solid-State Circuits Letters

Issue 12, December 2019

Special Issue on the 2019 IEEE Symposium on VLSI Circuits

Introduction to the Special Issue on the 2019 IEEE Symposium on VLSI Circuits

Jon Proesel ; Xin Zhang ; Minkyu Je

A 24-MB Embedded Flash System Based on 28-nm SG-MONOS Featuring 240-MHz Read Operations and Robust Over-the-Air Software Update for Automotive Applications
Akihiko Kanda ; Takashi Kurafuji ; Koichi Takeda ; Tomoya Ogawa ; Yasuhiko Taito ; Kazuo Yoshihara ; Masaya Nakano ; Takashi Ito ; Hiroyuki Kondo ; Takashi Kono

A 76-GHz to 81-GHz, 0.6° RMS Phase Error Multichannel Transmitter With a Novel Phase Detector and Compensation Technique
Takeji Fujibayashi ; Yohsuke Takeda

A Low-Power Relaxation Oscillator With Switched-Capacitor Frequency-Locked Loop for Wireless Sensor Node Applications
Xiaodong Meng ; Xing Li ; Lin Cheng ; Chi-Ying Tsui ; Wing-Hung Ki

A 56-Gb/s Long-Reach Fully Adaptive Wireline PAM-4 Transceiver in 7-nm FinFET
Dirk Pfaff ; Xin-Jie Wang ; Chai Palusa ; Robert Abbott ; Shahaboddin Moazzeni ; Leisheng Gao ; Mei-Chen Chuang ; Rolando Ramirez ; Maher Amer ; Tae Young Goh

Evaluating Celerity: A 16-nm 695 Giga-RISC-V Instructions/s Manycore Processor With Synthesizable PLL
Austin Rovinski ; Chun Zhao ; Khalid Al-Hawaj ; Paul Gao ; Shaolin Xie ; Christopher Torng ; Scott Davidson ; Aporva Amarnath ; Luis Vega ; Bandhav Veluri ; Anuj Rao ; Tutu Ajayi ; Julian Puscar ; Steve Dai ; Ritchie Zhao ; Dustin Richmond ; Zhiru Zhang ; Ian Galton ; Christopher Batten ; Michael B. Taylor ; Ronald G. Dreslinski

An Energy-Efficient Normally Off Microcontroller With 880-nW Standby Power, 1 Clock System Backup, and 4.69- μ s Wakeup Featuring 60-nm CAAC-IGZO FETs
Takahiko Ishizu ; Kazuma Furutani ; Yuto Yakubo ; Atsuo Isobe ; Masashi Fujita ; Tomoaki Atsumi ; Yoshinori Ando ; Tsutomu Murakawa ; Kiyoshi Kato ; Masahiro Fujita ; Shunpei Yamazaki

A 7-nm All-Digital Leakage-Current-Supply Circuit for Analog LDO Dropout Voltage Reduction
Keith A. Bowman ; Samantak Gangopadhyay ; Francois I. Atallah ; Hoan H. Nguyen ; Jihoon Jeong ; Daniel J. Yingling ; Anthony Polomik ; Mahesh Harinath ; Nathaniel Reeves ; Amer Cassier ; Brad R. Appel ; Arijit Raychowdhury

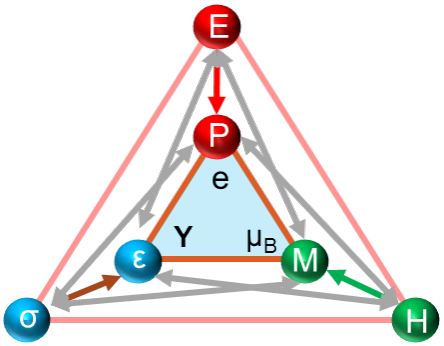
A Piezoelectric Energy-Harvesting System With Parallel-SSHI Rectifier and Integrated Maximum-Power-Point Tracking
Shuo Li ; Abhishek Roy ; Benton H. Calhoun

A Fast-Transient and High-Accuracy, Adaptive-Sampling Digital LDO Using a Single-VCO-Based Edge-Racing Time Quantizer
Jeonghyun Lee ; Jooeun Bang ; Younghyun Lim ; Seyeon Yoo ; Yongsun Lee ; Taeho Seong ; A

A Highly Reconfigurable Bit-Level Duty-Cycled TRF Receiver Achieving âˆ'106-dBm Sensitivity and 33-nW Average Power Consumption
Jesse Moody ; Anjana Dissanayake ; Henry Bishop ; Ruochen Lu ; Ningxi Liu ; Divya Duvvuri ; Anming Gao ; Daniel Truesdell ; N. Scott Barker ; Songbin Gong ; Benton H. Calhoun ; Steven M. Bowers

---

IEEE Journal on Exploratory Solid-State Computational Devices and Circuits



Issue 2, Part 1 - December 2019

Nonvolatile Spintronic Memory Cells for Neural Networks
Andrew W. Stephan ; Qiuwen Lou ; Michael T. Niemier ; Xiaobo Sharon Hu ; Steven J. Koester

JxCDC papers listed in order of popularity can be found online HERE.

For paper submission details, click HERE.

EDUCATION

Upcoming 2020 Distinguished Lectures

SSCS Delhi	Adaptive and Resilient Circuits for Processors - Presented by Keith Bowman	March 2, 2020	IIT Delhi **For more information, click here**
SSCS Saintgits College of Engineering	Adaptive and Resilient Circuits for Processors - Presented by Keith Bowman	March 6, 2020	Saintgits College of Engineering **For more information, click here**

CALL FOR PAPERS

Call for Papers: RFIC 2020

2020 IEEE Radio Frequency Integrated Circuits Symposium

June 21-23, 2020

Los Angeles, CA

https://www.rfic-ieee.org/

NEW for RFIC 2020: The RFIC symposium is expanding its scope to include System Applications and Interactive Demonstrations. This includes systems and applications in 5G, radar, imaging, terahertz, biomedical, and optoelectronic areas. In addition to the Emerging Circuit Technology area introduced in RFIC 2019, this year the symposium has introduced a completely new System Applications area and sub-committee that targets advanced system presentations in a range of topics related to communication, radar, imaging, sensing, and biomedical. To further highlight the systems aspects and enrich our attendees' experience, selected papers from this area will also be presented in a new Interactive Demonstration session.

The symposium starts on Sunday, 21 June 2020 with workshops and short courses, followed by two exciting plenary talks. Immediately following the plenary session, we will be holding an RFIC 'interactive' Sunday reception that will highlight our industry show-case and student papers finalists for an engaging social and technical evening event. Monday, 22 June and Tuesday, 23 June will be comprised of oral paper presentations, an interactive demonstration, and entertaining panel sessions.

We invite authors to submit their technical papers via the RFIC 2020 website; author's guidelines and **Call for Papers can be found here** . Complete information on how and when to submit a paper will be posted on the RFIC 2020 website. The conference will solicit papers describing original work in RFIC circuits, systems engineering, design methodology, RF modeling and CAD simulation, RFIC technologies, device technologies, fabrication, testing, reliability, packaging, and modules to support RF applications in areas such as Wireless Cellular and Connectivity, Low Power Transceivers, Receiver Sub-Systems and Circuits, Mixed-Signal RF and Data Converters, Reconfigurable and Tunable Front-Ends, Transmitter Sub-Systems and Power Amplifiers, Oscillators, Frequency Synthesis, Millimeter- and Sub-Millimeter Wave Systems, and High-Speed Data Transceivers.

Same as last year, a double-blind review process will be adopted to ensure anonymity for both authors and reviewers. Detailed instructions on how to submit a paper compliant with double-blind rules will be posted on the RFIC 2020 website.

Electronic Submission Deadlines:
Technical Paper Summaries in PDF format: 10 January 2020
Final Manuscripts for the Digest and Attendee Download: 23 March 2020

All submissions must be made at rfic-ieee.org in pdf form. Hard Copies are not accepted.

DOWNLOAD the RFIC 2020 Call for Papers

Call for Papers: IEEE Journal on Exploratory Solid-State Computational Devices and Circuits

Special Topic on "Exploratory Devices and Circuits for Compute-in-Memory"

Aims and Scope:

Deep learning and non-convex optimization problems are well known to be data-intensive applications. While graphic processing units (GPU) have become the mainstream platform to accelerate the algorithms in the cloud, there is a growing interest to develop application-specific integrated-circuit (ASIC) chips for further improving the energy-efficiency for these data-intensive workloads. Digital multiply-and-accumulate (MAC) arrays are generally employed as ASIC solutions, and data flow is often optimized to increase the data reuse on-chip. Nevertheless, most of the inputs and outputs are moved across MAC arrays and from global buffers . Therefore, it is more attractive to embed the MAC computations into the memory array itself, namely compute-in-memory (CiM), to minimize the data transfer. In C iM, the vector-matrix multiplication is executed in parallel (with analog computation) where the input vectors activate multiple rows.The dot-product is obtained as the multiplication of input voltage and cell conductance, and the partial sum is added up by the column current. An analog-to-digital converter (ADC) at the edge of the array generally converts the partial sum to binary bits for further digital processing.

To implement CiM, mature SRAM technologies (possibly with modified bit cells) have been proposed. However, SRAM is inherently volatile, anIEd consumes significant standby leakage power. In this sense, emerging non-volatile memory (eNVM) technologies are better suited for the area/power constraint platforms, as they could be turned on and off instantly without losing the stored weights. eNVMs of industry's interest here include resistive random access memory (RRAM), phase change memory (PCM), spin-transfer-torque magnetic random access memory (STT-MRAM) and ferroelectric field effect transistor (FeFET). In recent years, the industry has heavily invested in the commercialization of eNVM technologies, e.g. TSMC's 40nm RRAM, Intel's 22nm RRAM, TSMC's 40nm PCM, Intel's 22nm STT-MRAM, and Samsung's 28 nm STT-MRAM, while doped HfO2 based FeFET technology is also emerging, e.g. Globalfoundries' FeFET at 22nm.

Capitalizing on these developments, eNVM based CiM designs have also become viable. This special issue of the IEEE Journal on Exploratory Computational Devices and Circuits (JXCDC) aims to call for the recent research advances in the area of the compute-in-memory spanning devices, circuits, and systems. Papers on the interaction and co-optimization of the materials and devices as well as circuits and architecture are solicited.

Topics of Interest include but are not limited to:

Prospective authors are invited to submit original works and/or extended works based on conference presentations on various aspects of compute-in-memory. Memory technologies of interest include (but not limited to) SRAM, DRAM, NOR/NAND Flash, and emerging NVM devices such as PCM, RRAM/CBRAM, STT-MRAM/SOT-MRAM (or other spintronic memories), FeFET (or other ferroelectric memories), etc. The following topics are specifically solicited:

- Materials and devices that can enable compute-in-memory
- Integration of emerging technologies with silicon for compute-in-memory
- Crossbar array design for compute-in-memory
- Array-level demonstration for compute-in-memory
- Peripheral circuit design for compute-in-memory
- Architectural-level design for compute-in-memory
- Algorithms and hardware co-design for compute-in-memory

- Benchmarking simulators for compute-in-memory
- New applications for compute-in-memory beyond deep learning

Submission Guidelines:

The IEEE Journal on Exploratory Solid-State Computational Devices and Circuits (J XCDC) IS AN OPEN ACCESS PUBLICATION: The Open Access Fee is: $1,350 USD per article. Article submissions must be done through the ScholarOne Manuscripts website: **https://mc.manuscriptcentral.com/jxcdc.**

View our guidelines for papers and supplementary materials, as well as paper templates.

Important Dates:

Open for Submission: December 1st, 2019
Submission Deadline: February 1st, 2020
First Notification: March 1st, 2020
Revision Submission: April 1st, 2020
Final Decision: May 1st, 2020
Publication Online: June 1st, 2020

Guest Editor:

Shimeng Yu, Georgia Institute of Technology, **shimeng.yu@ece.gatech.edu**

Deputy Editor:

Azad Naeemi, Georgia Institute of Technology, **azad@gatech.edu**

Inquiries for the JxCDC Journal should be sent to: JXCDC@IEEE.ORG

JxCDC is sponsored by:

- Solid-State Circuits Society
- Magnetics Society
- Circuits & Systems Society
- Council on Electronic Design Automation
- Electron Devices Society
- Council on Superconductivity

Call for Papers: 2020 Symposia on VLSI

Technology and Circuits
June 14-19, 2020
Honolulu, Hawaii
https://vlsisymposium.org

Celebrating its 40th edition in 2020, the VLSI Symposia is the premier international conference on semiconductor technology and circuits. It offers a superb opportunity to interact and synergize on topics spanning the range from new neuromorphic devices, to beyond-the-state-of-the-art process technology to systems-on-chip and AI accelerators.

The circuits symposium is placing special emphasis on several innovation system focus areas, and encourages paper submissions on:

- Machine and deep learning
- FPGA-based accelerators
- Internet of Things
- Industrial electronics
- Big Data management
- Biomedical applications
- Robotics and autonomous transportation

In addition, submissions are welcomed in all of the following circuits areas:

- Processors, SoCs, and Machine Learning
- Digital circuits, signal integrity, and IOs
- Hardware security
- Memory circuits, architectures, and interfaces
- Biomedical circuits
- Sensors, imagers, and display circuits
- Power conversion circuits
- Analog, amplifier and filter circuits
- Wireless receivers and transmitters
- Data converters
- Frequency generation and clock circuits
- Wireline and optical transceivers

The technology symposium calls for papers in the following areas:

- Technologies for "Internet of Things"
- Technologies for Artificial Intelligence and Machine Learning Applications
- Stand-Alone and Embedded Static, Dynamic, non-Volatile and Emerging Memory
- Technologies
- CMOS Technology for Microprocessors and SoCs
- RF / Analog / Digital and Sensors Technologies
- New Process Technologies and Electronic Materials
- Advanced Packaging, System-in-Package (SiP) and 3D Technologies
- Photonics and Imaging Technologies
- Beyond CMOS Devices and Technologies for Heterogeneous Integration

Papers will be selected based on technical innovation, advances relative to previously published work, credibility of claims, and quality of writing and illustrations

Submission Information
Paper Submission Deadline: Monday, February 10, 2020, 23:59 PST

For more information, click here.

CONFERENCES

Upcoming 2020 SSCS-Sponsored Conferences

2020 IEEE International Solid-State Circuits Conference (ISSCC) San Francisco, California	**Feb 16 - 20, 2020**
2020 Design, Automation & Test in Europe Conference & Exhibition (DATE) Grenoble Cedex 2, France	**Mar 9 - 13, 2020**
2020 IEEE Custom Integrated Circuits Conference (CICC) Boston, MA	**Mar 22 - 25, 2020**
2020 International Symposium on VLSI Technology, Systems, and Applications (VLSI-TSA) Hsinchu, Taiwan	**Apr 20 - 23, 2020**
2020 International Symposium on VLSI Design, Automation, and Test (VLSI-DAT) Hsinchu, Taiwan	**Apr 20 - 23, 2020**
2020 IEEE Symposia on VLSI Technology and Circuits Honolulu, Hawaii	**Jun 16 - 19, 2020**
2020 IEEE Radio Frequency Integrated Circuits	**Jun 21 - 23, 2020**

Symposium (RFIC) Los Angeles, California	
2020 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS) Monterey, California	**Nov 8 - 11, 2020**
2020 IEEE Asian Solid-State Circuits Conference (A-SSCC) Hiroshima, Japan	**Nov. 9 - 11, 2020**

SSCS-Sponsored Conferences: Proceedings

Click the links below to access the latest SSCS-Sponsored conference proceedings.

2018

2018 IEEE International Solid-State Circuits Conference (ISSCC)
2018 IEEE Custom Integrated Circuits Conference (CICC)
2018 IEEE Symposium on VLSI Circuits (VLSI)
2018 IEEE 44th European Solid-State Circuits Conference (ESSCIRC)
2018 IEEE Asian Solid-State Circuits Conference (A-SSCC)

2019

2019 IEEE International Solid-State Circuits Conference (ISSCC)
2019 IEEE Custom Integrated Circuits Conference (CICC)
2019 Symposium on VLSI Circuits
2019 IEEE 45th European Solid-State Circuits Conference (ESSCIRC)

For Society news and happenings, check out the Fall 2019 issue of the Solid-State Circuits Magazine.