IEEE SOLID-STATE CIRCUITS SOCIETY

Where ICs are in IEEE

August 2019

UPCOMING SSCS WEBINAR

Challenges in the Design of Integrated Circuits for Wireless Power Delivery and Information Transfer in Implantable Medical Applications

Presenter: Prof. Zhihua Wang, Tsinghua University, Beijing, China
Wednesday, September 18th, 10:00 AM

Abstract: The demand for medical electronic devices, both smaller and smarter, is a key driving force behind integrated circuits and systems development. Implantable medical devices (IMDs), fully or partially implanted into the human body through surgery, have a set of strict technical requirements for information transfer between the external host devices (EHDs) and IMDs. They include the choice of frequency and bandwidth, power consumption, data rate, signal modulation scheme, disturbance, and interference. The miniaturization of IMDs makes the power supply design especially challenging. In order to power miniaturized IMDs, wireless power delivery (WPD) or wireless power transfer (WPT) is desirable. In a WPT system, improving the energy efficiency is a very important objective. The energy transfer efficiency should be as high as possible despite large variations in coupling and loading conditions.

This lecture comprises three parts. First, a recent radio transceiver design technique to reduce power consumption and area is proposed. A set of miniature IMDs has been implemented using this ultra-low power transceiver which can be integrated in different application-specific system-on-chip. Second, critical techniques for improving energy efficiency are addressed. Approaches include tracking the maximum efficiency point with a low-cost method, optimizing the efficiency of rectifiers and inverters, implementing a

power control loop between transmitter and receiver, and increasing the quality factor of loop antenna coils and coupling coefficient between coils. Finally, system-level implementations of popular biomedical applications, such as involve Gastric Electric Stimulator, Hearing Aid System, and digestive Tract Endoscopy System, are presented.

Bio: Zhihua Wang (M'99-SM'04-F'17) received the B.S., M.S., and Ph.D. degrees in Electronic Engineering in 1983, 1985 and 1990, respectively, from Tsinghua University, Beijing, China, where he has served as full professor and Deputy Director of the Institute of Microelectronics since 1997 and 2000. He was a visiting scholar at CMU (1992-1993) and KU Leuven (1993-1994), and was a visiting professor at HKUST (2014.9-2015.3). His current research mainly focuses on CMOS RFIC and biomedical applications, involving RFID, PLL, low-power wireless transceivers, and smart clinic equipment combined with leading edge RFIC and digital image processing techniques. He has co-authored 12 books/chapters, over 197 (514) papers in international journals (conferences), over 246 (29) papers in Chinese journals (conferences) and holds 118 Chinese and 9 US patents.

Prof. Wang has served as the chairman of IEEE SSCS Beijing Chapter (1999-2009), an AdCom Member of the IEEE SSCS (2016-2019), a technology program committee member of the IEEE ISSCC (2005-2011), a steering committee member of the IEEE A-SSCC (2005-), the technical program chair for A-SSCC 2013, a guest editor for IEEE JSSC Special Issues (2006.12, 2009.12 and 2014.11), an associate editor of IEEE Trans on CAS-I, II and IEEE Trans on BioCAS, and other administrative/expert committee positions in China's national science and technology projects.

CLICK HERE TO REGISTER

NEWS

Apply Now: ISSCC Rising Stars 2020

The **IEEE SSCS Women in Circuits** together with **ISSCC** will be sponsoring the first "Rising Stars 2020" for young professionals and students.

The Rising Stars 2020 is an educational workshop for graduate and undergraduate students, and young professionals who have graduated within the last two years, and are interested in learning how to excel at academic and industry careers in computer science, computer and electrical engineering.

20 rising stars in academia and industry will be selected to attend a special dinner, keynote from a high-profile already "Risen Star", and mentoring session. There will be a pre-dinner event introduction and welcome, networking, and poster event for the selected

20 rising stars where leading figures in the solid-state circuits community will be available for an intimate question and answer session.

Application Information: Applicants must be undergraduate, graduate, and young professionals who have graduated within the last two years at the time of the workshop or they must have obtained their last degree no earlier than 2018 and currently do not hold a faculty position.

All applications must be submitted by October 24, 2019 . Notification of acceptance will be sent out by November 12, 2019.

Click here for application instructions and more information.

SSCS Election Begins September 12th

The SSCS election for Members-at-Large for 2020-2022 will begin on September 12th. We hope you will take the time to exercise your vote and help choose the future direction of the Society.

If you are eligible to vote, then you will receive an email with a link to vote in the next few days.

The voting period will be from September 12 - October 24.

Machine Learning and AI Track at ISSCC

The ISSCC (International Solid State Circuits Conference) is the venue where the world's prime silicon implementations are published. This conference takes place yearly in February, located in the heart of Silicon Valley, San Francisco.

ISSCC now added an additional track to its conference focusing entirely on Machine Learning and AI. ISSCC ambitions to attract cutting edge AI chips, to innovate across the complete technology-circuit-architecture design space. To this end, a new dedicated conference subcommittee groups experts from all areas of machine learning, across different design levels.

With this email, we invite you to submit a paper on your next AI chip to ISSCC. Papers can be submitted here before September 9th, 2019. For more information, please consult the **ISSCC website** and **call for papers**.

NEW - SSCS Open Access Journal

The IEEE Solid-State Circuits Society (SSCS) is launching a new gold fully open access journal, IEEE Open Journal of Solid-State Circuits, spanning the full scope of the SSCS' fields of interest. The new journal, which will be fully compliant with funder mandates, including Plan S, will begin accepting submissions in fall 2019 and publish its first articles in early 2020.

An Independent editorial board will drive SSCS' commitment to publish high-quality articles including cutting-edge studies and breakthroughs in integrated circuits. The new journal will follow IEEE's established high standard of peer review, drawing on experts in the field to continue to publish the most highly cited content in field of interests.

The journal will be led by Jan Craninckx, imec, Leuven, Belgium.

For more information, please visit **open.ieee.org** or complete the **form** to receive an email when the journal will begin accepting submissions.

NEW! Get your SSCS Membership Certificate

Steps to download and print your certificate

1). **Log into Collabratec**
2). Click your name in the top right of the screen and select "Member Certificates" from the drop-down menu
3). From the "Member Certificates" page, click on the "Download PDF" link to the right of "IEEE Solid-State Circuits Society Membership"
4). Open the PDF and print it

SSCS Contests for Students

Calling all students! SSCS is pleased to announce the launch of two contests open to undergraduate and graduate students. Prizes are valued up to $2K.

CIRCUITS VIDEO CONTEST
Create a fun short (5-10 minute) video that explains circuits for high school students. Tell a story about a circuits concept. Videos should motivate a real-world application of circuits. Undergraduate and graduate students who are currently enrolled in a college or university may enter. Win up to $2K towards entering an SSCS-sponsored conference. **Click here for more information** on contest eligibility, how to enter, and more. **Submission Deadline: December 15, 2019**

2019 STUDENT CIRCUITS CONTEST
This contest involves solving a thought-provoking circuit analysis and design problem. Submissions are solicited by undergraduate and graduate students who are currently enrolled in a college or university. Win up tp $2K towards entering an SSCS-sponsored conference. **Click here for more information** on contest eligibility, how to enter, and more. **Submission Deadline: September 15, 2019**

2019-2020 SSCS STUDENT HOODIE DESIGN CONTEST
Design a hoodie that illustrates how integrated circuits power the artificial intelligence era. How do solid-state circuits play a role in the era of artificial intelligence? The winning design will be made into a hoodie (a hooded sweatshirt) and be distributed to all SSCS Student and Graduate Student members at ISSCC 2020. The contest is open only to IEEE SSCS Student and Graduate Student members. One grand prize winner will be selected and awarded $500 in cash prize and reimbursement to a 2020 SSCS sponsored conference of their choice. Two finalists will receive reimbursement to a 2020 SSCS sponsored conference. **Click here for more information**. **Submission Deadline: November 14, 2019.**

UPCOMING SSCS-SPONSORED EVENTS

Save the date for these upcoming Society-sponsored events.

The IEEE Solid-State Circuits Society will be sponsoring two exciting events at ESSCIRC/ESSDERC 2019. ESSCIRC/ESSDERC is an annual European forum for the presentation and discussion of recent advances in solid-state devices and circuits.
The conference will be held in Krakow, Poland, September 23-26, 2019 at the Conference Center of the Jagiellonian University.

For more information about the conference, **please click here**.

SSCS Diversity Luncheon: Cultivating Engineering Confidence
Tuesday, September 24, 2019
12:40 - 2:00 PM
Bistro Room, Level 0

Pick up your lunch from the cafeteria and bring it to the room. Drinks, coffee, and dessert will be provided.

The luncheon will feature talks by industry and academic professionals sharing their experiences in their careers where a challenge, project, or a mentor helped them become a better engineer and problem solver. There will be a group discussion about mentoring.

Tickets for this event will be distributed on a first come, first serve basis. Pick up your ticket at the ESSCIRC/ESSDERC registration desk. This event is open to everyone of all ages and genders.

Young Professionals and Students Micro-Mentoring and Career Coaching Session
Monday, September 23, 2019
6:30 PM - 8:30 PM
Exhibition Room

Complimentary event with light refreshments for all students, faculty, and engineers within 15 years of their first degree. Leading experts from industry and academia, IEEE SSCS executives, and Distinguished Lecturers will share their experiences. One-on-one answers to all your questions on publications, entrepreneurship, industry vs. academia and career coaching.

Click here to register for the event.
On-site registration is also available.

PUBLICATIONS

The latest in SSCS Flagship Publications...

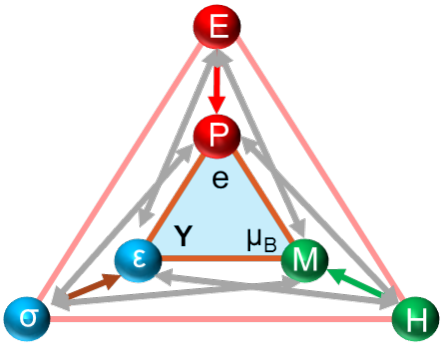
IEEE Journal of Solid-State Circuits

Vol. 54, Issue 9, September 2019

Introduction to the Special Section on the 2018 IEEE BCICTS Conference Shahriar Shahramian
Analysis and Design of Wideband I/Q CMOS 100-200 Gb/s Modulators Hasan Al-Rubaye ; Gabriel M. Rebeiz
Design of a 55-nm SiGe BiCMOS 5-bit Time-Interleaved Flash ADC for 64-Gbd 16-QAM Fiberoptics Applications Alireza Zandieh ; Peter Schvan ; Sorin P. Voinigescu
Broadband 240-GHz Radar for Non-Destructive Testing of Composite Materials Thomas Merkle ; Dominik Meier ; Sandrine Wagner ; Axel Tessmann ; Michael Kuri ; Hermann Massler ; Arnulf Leuther
A Three-Stage 18.5-24-GHz GaN-on-SiC 4 W 40% Efficient MMIC PA Maxwell Robert Duffy ; Gregor Lasser ; Guillermo Nevett ; Michael Roberg ; Zoya Popović
20-nm In0.8 Ga0.2 As MOSHEMT MMIC Technology on Silicon Axel Tessmann ; Arnulf Leuther ; Felix Heinz ; Frank Bernhardt ; Laurenz John ; Hermann Massler
A Fully Integrated 384-Element, 16-Tile, W -Band Phased Array With Self-Alignment and Self-Test Shahriar Shahramian ; Michael J. Holyoak ; Amit Singh ; Yves Baeyens
A 115-135-GHz 8PSK Receiver Using Multi-Phase RF-Correlation-Based Direct-Demodulation Method Hossein Mohammadnezhad ; Huan Wang ; Andreia Cathelin ; Payam Heydari
A 0.34-THz Wideband Wide-Angle 2-D Steering Phased Array in 0.13- Î¼m SiGe BiCMOS Hossein Jalili ; Omeed Momeni
A 4-GHz Low-Power, Multi-User Approximate Zero-IF FM-UWB Transceiver for IoT Vladimir Kopta ; Christian C. Enz
RF Filter Synthesis Based on Passively Coupled N-Path Resonators Pingyue Song ; Hossein Hashemi
A 1-2 GHz Computational-Locking ADPLL With Sub-20-Cycle Locktime Across PVT Variation Fahim ur Rahman ; Greg Taylor ; Visvesh Sathe
A 320-fs RMS Jitter and - 75-dBc Reference-Spur Ring-DCO-Based Digital PLL Using an Optimal-Threshold TDC Taeho Seong ; Yongsun Lee ; Seyeon Yoo ; Jaehyouk Choi
Analysis and Correction of Noise Injection Due to Parallel-Output-Misalignment (POM) Effects in Ring-Type Time-to-Digital Converters (TDCs) Tuoxin Wang ; John W. M. Rogers ; Krste Mitric
A 1-V 175-u W 94.6-dB SNDR 25-kHz Bandwidth Delta-Sigma Modulator Using Segmented Integration Techniques Sheng-Hui Liao ; Jieh-Tsorng Wu
A 9.1-ENOB 6-mW 10-Bit 500-MS/s Pipelined-SAR ADC With Current-Mode Residue Processing in 28-nm CMOS Kyoung-Jun Moon ; Dong-Shin Jo ; Wan Kim ; Michael Choi ; Hyung-Jong Ko ; Seung-Tak Ryu
Study and Design of a Fast Start-Up Crystal Oscillator Using Precise Dithered Injection and Active Inductance Alireza Karimi-Bidhendi ; Haoran Pu ; Payam Heydari
Single-Chip 3072-Element-Channel Transceiver/128-Subarray-Channel 2-D Array IC With Analog RX and All-Digital TX Beamformer for Echocardiography Yutaka Igarashi ; Shinya Kajiyama ; Yusaku Katsube ; Takuma Nishimoto ; Tatsuo Nakagawa ; Yasuyuki Okuma ; Yohei Nakamura ; Takahide Terada ; Taizo Yamawaki ; Toru Yazaki ; Yoshihiro Hayashi ; Kazuhiro Amino ; Takuya Kaneko ; Hiroki Tanaka
A 1.17-Megapixel CMOS Image Sensor With 1.5 A/D Conversions per Digital CDS Pixel Readout and Four In-Pixel Gain Steps

Øyvind Janbu ; Robert Johansson ; Tore Martinussen ; Johannes Solhusvik
A Reconfigurable Cross-Connected Wireless-Power Transceiver for Bidirectional Device-to-Device Wireless Charging Fangyu Mao ; Yan Lu ; Rui P. Martins
Analysis and Design of a Multi-Step Bias-Flip Rectifier for Piezoelectric Energy Harvesting Sundeep Javvaji ; Vipul Singhal ; Vinod Menezes ; Rajat Chauhan ; Shanthi Pavan
Design of Sub-Gigahertz Reconfigurable RF Energy Harvester From âˆ'22 to 4 dBm With 99.8% Peak MPPT Power Efficiency Zizhen Zeng ; Shanpu Shen ; Xiaopeng Zhong ; Xing Li ; Chi-Ying Tsui ; Amine Bermak ; Ross Murch ; Edgar Sánchez-Sinencio
Self-Convergent Trimming SRAM True Random Number Generation With In-Cell Storage Po-Shao Yeh ; Chih-An Yang ; Yi-Hong Chang ; Yue-Der Chih ; Chrong-Jung Lin ; Ya-Chin King
Reconfigurable Clock Networks for Wide Voltage Scaling Longyang Lin ; Saurabh Jain ; Massimo Alioto

IEEE Journal on Exploratory Solid-State Computational Devices and Circuits



Issue 1, Part 2 - June 2019

Boosted Spin Channel Networks for Energy-efficient Inference Ameya D. Patil ; Sasikanth Manipatruni ; Dmitri E. Nikonov ; Ian A. Young ; Naresh R. Shanbhag
Using Floating Gate Memory to Train Ideal Accuracy Neural Networks Sapan Agarwal ; Diana Garland ; John Niroula ; Robin B. Jacobs-Gedrim ; Alex Hsia ; Michael S. Van Heukel
Unsupervised learning to overcome catastrophic forgetting in neural networks Irene Muñoz-Martín ; Stefano Bianchi ; Giacomo Pedretti ; Octavian Melnic ; Stefano Ambrogio ; Daniele Ielmini
Performance Estimate of Inverse Rashba-Edelstein Magnetoelectric Devices for Neuromorphic Computing Andrew W. Stephan ; Jiaxi Hu ; Steven J. Koester
Graded-Anisotropy-Induced Magnetic Domain Wall Drift for an Artificial Spintronic Leaky Integrate-and-Fire Neuron Wesley H. Brigner ; Xuan Hu ; Naimul Hassan ; Christopher H. Bennett ; Jean Anne C. Incorvia ; Felipe Garcia-Sanchez ; Joseph S. Friedman
Subthreshold Spintronic Stochastic Spiking Neural Networks with Probabilistic Hebbian Plasticity and Homeostasis Steven D. Pyle ; Ramtin Zand ; Shadi Sheikhfaal ; Ronald F. DeMara

JxCDC papers listed in order of popularity can be found online HERE.

For paper submission details, click HERE.

IEEE Solid-State Circuits Letters

Issue 7, July 2019

Crossover Logic: A Low-Power Topology for Unipolar Dual-Gate Thin-Film Technologies
Florian De Roose ; Jan Genoe ; Wim Dehaene ; Kris Myny

EDUCATION

October 2019 Distinguished Lectures

There are currently no scheduled Distinguished Lectures in September

SSCS Lehigh Valley	Continuous-Time Sigma-Delta ADCs for Receiver Application - Presented by Maurits Ortmanns	October 7, 2019	Lehigh University **For more information, click here.**
SSCS Princeton/Central NJ	Talk Title: TBD - Presented by Maurits Ortmanns	October 8, 2019	Princeton University **For more information, click here.**
SSCS/EDS New York	Talk Title TBD - Presented by Maurits Ortmanns	October 9, 2019	Columbia University **For more information, click here.**

CALL FOR PAPERS

ISSCC 2020: Call for Papers

IEEE International Solid-State Circuits Conference
February 16 - 20, 2020
San Francisco, California
www.isscc.org

ISSCC 2020 Conference Theme: Integrated Circuits Powering the AI Era"

The steady advancement of solid-state circuits has led to technological betterment in our daily living, demonstrated by exploding applications ranging from medical, wearable and mobile electronics to IoT, virtual reality, autonomous driving and robotics. While the widespread excitement resides in the applications where end-users touch and feel, the systems are enabled by integrated circuits engines that are woven into this technological fabric of our lives. Galvanized by this reality, the solid-state circuits community is driven to enhance the platform that continues to evolve. With much enthusiasm and anticipation, and even uncertainty, we look onward to this emerging AI era. Consequently, ISSCC 2020 seeks contributions that will continue to enhance and reshape the future.

Innovative and original papers are solicited in subject areas including (but not limited to) the following:

ANALOG: Amplifiers, comparators, oscillators, filters, references; nonlinear analog circuits; digitally-assisted analog circuits; MEMS/sensor interface circuits.
DATA CONVERTERS: Nyquist-rate and oversampling A/D and D/A converters; embedded and application-specific A/D and D/A converters; analog to information conversion; time-to-digital converters.
DIGITAL CIRCUITS and ARCHITECTURES & SYSTEMS: Digital circuits, building blocks, and complete systems for microprocessors, micro-controllers, application processors, graphics processors; digital systems for communications, video and multimedia, cryptography, smart cards, security and trusted computing, accelerators,reconfigurable systems, near- and sub-threshold systems, emerging applications. Digital circuits for intra-chip communication, clock distribution, soft-error and variation-tolerant design, power management (i.e. voltage regulators, adaptive digital circuits, digital sensors), PLLs for digital clocking applications, and security circuits (i.e. PUFs, TRNG, side-channel attack countermeasures, and attack-detection sensors).
IMAGERS, MEMS, MEDICAL, & DISPLAY: Image sensors and SoCs; automotive, LIDAR, and ultrasonic sensors; MEMS sensor systems; wearable, implantable, ingestible electronics, biomedical SoCs, neural interfaces and closed-loop systems; biosensors, microarrays, and lab-on-a-chip; display electronics, displays with sensing functionality; sensing for AR/VR.
MACHINE LEARNING and AI: Chips demonstrating system, architecture and circuit innovations for machine learning and artificial intelligence: processor architectures, accelerators and digital circuits; mixed-signal, analog, near-sensor and in-sensor processing schemes; architectures leveraging near-memory and in-memory computation, using volatile or non-volatile memories.
MEMORY: Static, dynamic, and non-volatile memories for stand-alone and embedded applications; memory/SSD controllers; high-bandwidth I/O interfaces; memories based on phase-change, magnetic, spin-transfer-torque, ferroelectric, and resistive materials; array architectures and circuits to improve low-voltage operation, power reduction, reliability, and fault tolerance; application-specific circuit enhancements within the memory subsystem, including in-memory logic functions and compute.
POWER MANAGEMENT: Power management and control circuits, regulators; switched-mode power converter ICs using inductive, capacitive, and hybrid techniques; energy harvesting circuits and systems; wide-bandgap topologies and gate-drivers; power and signal isolators; robust power management circuits for automotive and other harsh environments; circuits for lighting, wireless power and envelope modulators.
RF CIRCUITS and WIRELESS SYSTEMS: Building blocks and complete solutions at RF, mm-Wave and THz frequencies for receivers, transmitters, frequency synthesizers, transceivers, SoCs, and SiPs. Innovative circuit-level and system-architecture solutions for established wireless standards and future systems or applications such as radar, sensing, and imaging.
TECHNOLOGY DIRECTIONS: Emerging IC and system solutions for: biomedical, sensor interfaces, analog signal processing, power management, computation (including non-CMOS machine learning), data storage, and communication; non-silicon-, carbon-, organic-, metal-oxide-, compound-semiconductor- and new-device-based circuits; nano, flexible, large-area, stretchable, printable, spintronics, quantum, optical, integrated photonics, and 3D-integrated electronics.
WIRELINE: Receivers/transmitters/transceivers for wireline systems, including backplane transceivers, optical links, chip-to-chip communications, 2.5/3D interconnect, copper-cable links, and equalizing on-chip links; exploratory I/O circuits for advancing data rates, power efficiency, equalization, robustness, adaptation capability, and design methodology; building blocks for wireline transceivers (such as AGCs, analog and ADC/DAC-based front ends, equalizers, clock generation and distribution circuits including PLLs, line drivers, and hybrids).

Deadline for Paper Submission: Monday, September 9, 2019, 3:00 PM Eastern Daylight Time

The ISSCC 2020 Paper Submission Site Opens July 1st!

Click here for more information

2020 VLSI-DAT: Call for Papers

2020 International Symposium on VLSI Design, Automation, and Test

April 20-23, 2020

Hsinchu, Taiwan

www.expo.itri.org.tw/2020vlsidat

The International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA symposium) held once every two years, gathers experts from all over the world. Scientists and engineers discuss and present the state-of-the-art technology R&D and macro development of the industry's future. It is considered the most important event in Taiwan's semiconductor industry and highly anticipated by local companies. Taking advantage of the information learned during the conference, the symposium hopes to create new opportunities for Taiwan's semiconductor industry. The VLSI-TSA symposium is becoming more significant since Taiwan not only occupies a prominent position in the global semiconductor industry, but also is increasingly competitive globally in IC design technology and communications information products.

The VLSI-DAT symposium is proud to create a platform for technical exchanges and communications shared by experts from all over the world. The purpose is to bring together scientists and engineers actively engaged in research, development, and manufacturing on VLSI Design, Automation and Test to discuss current progress in this field.

Original, unpublished papers on all aspects of VLSI Design, Automation, and Test are solicited, including but not limited to:

ANALOG DESIGN	DIGITAL DESIGN	EDA	TEST
RF, Analog and Mixed Signal Circuits	Digital Circuits and ASICs	Logic and Behavioral Synthesis	Test Generation and Compression
Sensors and Interface Circuits	CPU, DSP and Multicore Architectures	Physical Design and Verification	Design-for-Testability and BIST
Memory Circuits and Systems	Multimedia Processing Designs	Design for Manufacturability	RF, Analog and Mixed-Signal Test
Biomedical Circuits	Communication Designs	Power/Thermal Estimation and Optimization	Memory Test
Energy-Harvesting and Power Circuits	Hardware Security and Trust	Design Verification	SOC and System Level Test
Ultra Low-Power Circuits and Systems	Designs for Edge Computing	Modeling and Simulation	Silicon Debug and Diagnosis
Memristive and Neuromorphic Circuits	Designs for Machine Learning	Electronic System Level Design	3D IC and Interposer-Based IC Test
Security Circuits for IoT and AI	SOC and NOC Architectures	Hardware/Software Co-Design	Yield and Reliability Enhancement
	Embedded System and Software	Machine Learning for EDA	On-Chip Monitoring
	System-in-Package Designs	Analog EDA	Test Data Mining and Learning
		EDA for Microfluidic Biochips	Test Standards

Important Dates:
Paper Submission Deadline: Oct. 15, 2019
Notification of Paper Acceptance: Dec. 31, 2019
Final Paper Submission Deadline: Jan. 31, 2020
Author Registration Deadline: Feb. 29, 2020

Click here for more information

Call for Papers: CICC 2020

IEEE Custom Integrated Circuits Conference

March 22 - 25, 2019

Boston, MA

http://ieee-cicc.org/

The IEEE Custom Integrated Circuits Conference is a premier conference devoted to IC development. The conference program is a blend of oral presentations, exhibits, panels and forums. The conference sessions present original first published technical work and innovative circuit techniques that tackle practical problems. CICC is the conference to find out how to solve design problems, improve circuit design techniques, get exposure to new technology areas, and network with peers, authors and industry experts.

There are 3 days of Technical Sessions that include lecture presentations addressing state of the art developments in integrated circuit design. The Educational Sessions are a full day of tutorials instructed by recognized invited speakers. The Panels, and Forums are presented throughout the conference to enrich the learning experience of the attendees. The Panel Discussions and Forums are presented by leaders from the IC industry. CICC includes an Exhibits Hall that is open in the evenings where Semiconductor manufacturers, software tool suppliers, silicon IP providers, design-service houses, and technical book publishers offer displays and demonstrations of their products. CICC is sponsored by the IEEE Solid-State Circuits Society and technically co-sponsored by the IEEE Electron Devices Society.

Submission of original and unpublished work is being solicited in the following areas:

- **Analog Circuits and Techniques** for areas such as communications, biomedical, aerospace, automotive, energy, environment, analog computing and security applications, ranging from building blocks to silicon sensors, interfaces, and novel clock generation architectures.
- **Data Converters** including but not limited to A/D, D/A, time-to-digital, frequency-to-digital and analog to information converters of all types enabled by new techniques, architectures, or technologies.
- **Design Foundations** for novel digital, analog, mixed-signal, and memory circuit techniques for present and emerging applications (deep learning, autonomous vehicles, IoT, security, quantum computing). Modeling and simulation of advanced CMOS (FinFET, UTTB-SOI) and beyond-CMOS devices (MEMS, GaN, Non-Volatile Memories, STT) to improve design quality, efficiency, and reliability. Design for manufacturing, test, aging, security, and reliability (novel DFT circuits, system-level testing). High-level system modeling, digital/analog design infrastructure, and verification and emulation for complex SoCs.
- **Digital Circuits, SoCs, and Systems** solicit hardware-based papers in technologies that enhance integrated systems including processors, accelerators, memory systems, with applications in artificial intelligence, security, autonomous transportation, cloud computing, sensing, and communication.
- **Emerging Technologies, Systems, and Applications** solicit hardware focused papers in the technologies of tomorrow extending from new device to system integration and applications with focus on, but not limited to:
    - **Next-generation technology and sensors** including devices, integration, and packaging including nano-primitives, non-silicon based technology, and advanced assembly. Sensor interfaces for MEMS, mm-wave/THz, flexible, printed, large-area and organic electronics, electronic-photonic co-design, and silicon photonics.
    - **Biomedical circuits, systems, and applications** including neural interfaces, microarrays, lab-on-a-chip, bio-inspired circuits, implantable and/or wearable systems, closed-loop systems with sensing and actuation, medical imaging, and other biosensors including biomedical signal processing SoCs.
- **Power Management** circuits and design techniques including DCDC converters, control and management circuits, linear regulators, wireless power transfer, and other methods for improvements in overall system efficiency and performance.
- **Wireless Transceivers and RF/mm-Wave Circuits and Systems** for low-power, energy-efficient and high performance wireless links, biomedical and sensing networks, IoT applications, cellular connectivity including M2M applications (LTE-M, NB-IoT), emerging broadband and MIMO networks (5G, WLAN), vehicle-to-vehicle (V2V), millimeter-wave & THz systems (radar, sensing and imaging), frequency synthesis and LO generation.
- **Wireline and Optical Communications Circuits and Systems** for electrical and optical communications, including serial links for intra-chip and chip-to-chip interconnections, high-speed memory and graphics interfaces, backplanes, long-haul, and power line communications; novel I/O circuits for advancing data rates, improving power efficiency, and supporting extended voltage applications; clocking techniques including PLLs and CDRs; components such as equalizers, high-speed ADC-RX/DAC-TX, silicon photonic and optical interface circuitry.

Important Dates:

Paper Submission Deadline: November 1, 2019
Paper Acceptance Notification: January 31, 2020

Click here for more information

CONFERENCES

Upcoming 2019 SSCS-Sponsored Conferences

ESSCIRC/ESSDERC 2019 - IEEE 45th European Solid-State Circuits Conference (ESSCIRC)/49th European Solid-State Device Research Conference Cracow, Poland	**September 23 - 26, 2019**
2019 IEEE Biomedical Circuits and Systems Conference (BioCAS) Nara, Japan	**October 17 - 19, 2019**
2019 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS) Nashville, Tennessee	**November 3 - 6, 2019**
2019 IEEE Asian Solid-State Circuits Conference (A-SSCC) Macau, China	**November 4 - 6, 2019**

SSCS-Sponsored Conferences: Proceedings

Click the links below to access the latest SSCS-Sponsored conference proceedings.

2018

2018 IEEE International Solid-State Circuits Conference (ISSCC)
2018 IEEE Custom Integrated Circuits Conference (CICC)
2018 IEEE Symposium on VLSI Circuits (VLSI)
2018 IEEE 44th European Solid-State Circuits Conference (ESSCIRC)
2018 IEEE Asian Solid-State Circuits Conference (A-SSCC)

2019

2019 IEEE International Solid-State Circuits Conference (ISSCC)
2019 IEEE Custom Integrated Circuits Conference (CICC)

ESSCIRC/ESSDERC Registration is EXTENDED!

September 23-26, 2019
Krakow, Poland

The aim of ESSDERC and ESSCIRC is to provide an annual European forum for the presentation and discussion of recent advances in solid-state devices and circuits. The level of integration for system-on-chip design is rapidly increasing. This is made available by advances in semiconductor technology. Therefore, more than ever before, a deeper interaction among technologists, device experts, IC designers and system designers is

necessary. While keeping separate Technical Program Committees, ESSDERC and ESSCIRC are governed by a common Steering Committee and share Plenary Keynote Presentations and Joint Sessions bridging both communities. Attendees registered for either conference are encouraged to attend any of the scheduled parallel sessions, regardless to which conference they belong.

CONFERENCE HIGHLIGHTS

- 4 joint keynote presentations
- 3 ESSDERC keynote presentations
- 3 ESSCIRC keynote presentations
- Invited papers with overall coverage of all spects of advanced devices and circuits
- Presentation of IEEE and ESSDERC/ESSCIRC Awards
- ESSDERC/ESSCIRC Gala Dinner on Wednesday, September 25, 2019
- Tutorials and workshops

The venue of the conference events, including workshops and tutorials, will be in the strict centre of Cracow in the Auditorium Maximum of Jagiellonian University. The working language of the conference is English.

CLICK HERE FOR REGISTRATION INFORMATION!

For Society news and happenings, check out the Summer 2019 issue of the Solid-State Circuits Magazine.
