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April 2020

UPCOMING SSCS & MTT-S JOINT WEBINAR

Transceiver Architectures for Beyond-5G: Challenges and R&D Opportunities

Presenter: Prof. Payam Heydari, University of California, Irvine
Thursday, May 14th, 2020
12:00 PM ET

Abstract: The ongoing super-linear growth of world's population coupled with the worldwide access to internet and the general public's tendency to use more bandwidth-intensive applications fuel the urgency to enhance wireless infrastructures so as to meet these demands. Consequently, the wireless R&D is headed towards the inception of "Beyond-5G" (e.g., 6G) technology. This webinar provides a comprehensive overview of challenges and opportunities in designing beyond-5G transceiver architectures capable of achieving high data rates above and beyond 20 Gbps.

Biography: Payam Heydari received his Ph.D. degree from the University of Southern California in 2001. He is currently a Full Professor of Electrical Engineering at the University of California, Irvine. Dr. Heydari's research covers the design of terahertz/millimeter-wave/RF and analog integrated circuits. He is the (co)-author of two books, one book chapter, and more than 150 journal and conference papers. He has given several Keynote Speech and tutorials to international forums and conferences. He was a Distinguished Lecturer of the IEEE Solid-State Circuits Society (Jan. 2014 - Jan. 2016), and is now a Distinguished Microwave Lecturer of the IEEE Microwave Theory and Techniques Society (Jan. 2019 - Dec.

2022). His group was among the first who introduced the design of millimeter-wave integrated circuits in silicon technologies. They demonstrated the world's first fundamental frequency CMOS transceiver operating above 200 GHz, the world's highest radiated power and highest efficiency sub-terahertz circularly-polarized radiator in silicon employing a multi-port cavity-backed structure.

Dr. Heydari was selected as the inaugural Faculty Innovation Fellow by the University of California, Irvine (UCI) Beall Applied Innovation. He is the recipient of a number of awards including the 2017 UCI's School of Engineering Mid-Career Excellence in Research, the 2010 Faculty of the Year Award from UC-Irvine's Engineering Student Council (ECS), the 2009 School of Engineering Best Faculty Research Award, the 2007 IEEE Circuits and Systems Society Guillemin-Cauer Award, the 2005 IEEE Circuits and Systems Society Darlington Award, and the 2005 National Science Foundation (NSF) CAREER Award.

Dr. Heydari is an AdCom member of the IEEE Solid-State Circuits Society. Dr. Heydari currently serves an Associate Editor for the IEEE Journal of Solid-State Circuits and the IEEE Solid-State Circuits Letters. He was a member of the Technical Program Committee of the International Solid-State Circuits Conference (ISSCC). Dr. Heydari is an IEEE Fellow for contributions to silicon-based millimeter-wave integrated circuits and systems.

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EDUCATION

Upcoming 2020 Distinguished Lectures

Due to the COVID-19 Pandemic, there are currently no SSCS Distinguished Lectures scheduled.

CONFERENCES

Upcoming 2020 SSCS-Sponsored Conferences

2020 International Symposium on VLSI Technology, Systems, and Applications (VLSI-TSA) Hsinchu, Taiwan	**Rescheduled to August 10th -13th, 2020**
2020 International Symposium on VLSI Design, Automation, and Test (VLSI-DAT) Hsinchu, Taiwan	**Rescheduled to August 10th -13th, 2020**
2020 IEEE Symposia on VLSI Technology and Circuits Honolulu, Hawaii	**Jun 14 - 19, 2020** **To be held virtually**
2020 IEEE Radio Frequency Integrated Circuits Symposium (RFIC) Los Angeles, California	**Jun 21 - 23, 2020**
2020 European Solid-State Circuits Conference/2020 European Solid-State Device Research Conference Grenoble, France	**Rescheduled to September 2021.** **A new virtual educational event is currently being developed for September 14, 2020.**
2020 IEEE Biomedical Circuits and Systems	**Rescheduled for October 2021**

Conference (BioCAS) Berlin, Germany	
2020 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS) Monterey, California	**Nov 8 - 11, 2020**
2020 IEEE Asian Solid-State Circuits Conference (A-SSCC) Hiroshima, Japan	**Nov. 9 - 11, 2020**

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Due to the cancellation of ESSCIRC/ESSDERC 2020, the conferences steering committee recommends the following for authors:

For authors who were planning on submitting their paper to ESSCIRC/ESSDERC, you are encouraged to submit your publications to the following IEEE Journals:

For ESSCIRC, you can submit to Solid-State Circuits Letters (SSC-L).
Visit: **https://mc.manuscriptcentral.com/ssc-l** and select the Special Section on ESSCIRC 2020 when submitting your paper. The submission deadline is May 15th, 2020. Publication will be in October/November 2020. Authors having accepted papers through this path will be invited to present their work in a Special Oral Session at ESSCIRC 2021.

Authors are also welcome to submit their papers to IEEE Journal of Solid-State Circuits and the IEEE Open Journal of Solid-State Circuits.

For ESSDERC, please see **https://eds.ieee.org/publications** for more information

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2019

2019 IEEE International Solid-State Circuits Conference (ISSCC)
2019 IEEE Custom Integrated Circuits Conference (CICC)
2019 IEEE Symposium on VLSI Circuits
2019 IEEE 45th European Solid-State Circuits Conference (ESSCIRC)
2019 IEEE Asian Solid-State Circuits Conference (A-SSCC)

2020

2020 IEEE International Solid-State Circuits Conference (ISSCC)
2020 IEEE Custom Integrated Circuits Conference (CICC)

PUBLICATIONS

JxCDC Call for Papers: Special Topic on Tunneling FETs for Energy-Efficient Computing & Information

Processing

A call for papers is now open for Special Topic on Tunneling FETs for Energy-Efficient Computing & Information Processing

Guest Editor:
Uygar Avci, Intel Corporation, **uygar.e.avci@intel.com**
Editor-in-Chief:
Azad Naeemi, Georgia Institute of Technology, **azad@gatech.edu**

Aims and Scope:
The Tunneling Field-Effect Transistor (T-FET) is considered a future transistor option due to its steep-slope prospects and the resulting advantages in operating at low supply voltage (VDD).

Reducing supply voltage (VDD) while keeping a low leakage current and a reasonably high on-current is critical for minimizing energy consumption and improving the energy efficiency of computing and information processing. The thermal limit (Boltzmann's Tyranny) of the MOSFET transistor subthreshold swing (SS) restricts lowering its threshold voltage (Vt), causing significant performance degradation at low VDD. A Tunneling Field Effect Transistor's (T-FET) SS is not limited by this thermal tail and may perform better at low VDD. Since the first experimental proof of subthreshold swing (SS) < 60mV/dec, T-FET's prospects have attracted the interest of researchers. Silicon's large indirect bandgap and large carrier mass prevents Si T-FET from achieving high drive currents. But due to the availability of high-quality material together with years of know-how, Si and Si/Ge T-FETs have been studied initially, and showed the first of many devices with SS < 60mV/dec. III-V materials for T-FETs attracted attention next because of their low bandgap and carrier mass. While more challenging to fabricate, the broken bandgap hetero-junctions III-V T-FETs eventually showed the highest T-FET drive-current. Beyond III-V materials, Transition Metal Dichalcogenide and other 2D materials may provide a path in the future to high performance energy efficient transistors, thanks to thinner channels enabling better control of the tunneling field.

This call for papers on Tunneling FETs is for rapid publication of seminal results across the areas of T-FET materials, devices, and circuits for novel computation and information processing paradigms. Paper submissions with key insights into the advantages and challenges of specific T-FET device and material designs and circuit techniques are especially valued in order to guide the semiconductor industry and academia on a path toward more energy-efficient computing.

Topics of Interest:
Special Topic on Tunneling Field Effect Transistors (Tunneling FETs, T-FETs)

- N- and P- Tunneling FET experimental transistors demonstrating high performance at low supply voltage
- T-FET material and device design, including hetero-junction III-V materials, transition metal dichalcogenides, other two-dimensional materials and their hetero-junctions
- T-FET circuits for energy efficient computing and information processing
- Energy-Efficient computing and information processing with T-FET transistor circuits and architectures.

Important Dates:
Open for Submission: April 15th, 2020
Submission Deadline: June 30th, 2020
First Notification: August 1st, 2020
Revision Submission: August 21st, 2020
Final Decision: September 30th, 2020
Publication Online: December 1st, 2020

Submission Guidelines:
The IEEE Journal on Exploratory Solid-State Computational Devices and Circuits (JXCDC) IS AN OPEN ACCESS ONLY PUBLICATION:

Charge for Authors: $1,350 USD per paper.

Paper submissions must be done through the ScholarOne Manuscripts website: **https://mc.manuscriptcentral.com/jxcdc**

Guidelines for papers and supplementary materials, as well as a paper template, are provided at this **website**.

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IEEE Journal of Solid-State Circuits

Vol. 55, Issue 5, May 2020

Special Issue on the 2019 RFIC Symposium

Introduction to the Special Section on the 2019 RFIC Symposium
Hongtao Xu

Millimeter-Scale Node-to-Node Radio Using a Carrier Frequency-Interlocking IF Receiver for a Fully Integrated 4 × 4 × 4 mm3 Wireless Sensor Node
Li-Xuan Chuo ; Zhen Feng ; Yejoong Kim ; Nikolaos Chiotellis ; Makoto Yasuda ; Satoru Miyoshi ; Masaru Kawaminami ; Anthony Grbic ; David Wentzloff ; David Blaauw ; Hun-Seok Kim

A Fully Passive RF Front End With 13-dB Gain Exploiting Implicit Capacitive Stacking in a Bottom-Plate N-Path Filter/Mixer
Vijaya Kumar Purushothaman ; Eric A. M. Klumperink ; Berta Trullas Clavera ; Bram Nauta

An 802.11ba-Based Wake-Up Radio Receiver With Wi-Fi Transceiver Integration
Renzhi Liu ; Asma Beevi K. T. ; Richard Dorrance ; Deepak Dasalukunte ; Vinod Kristem ; Mario A. Santana Lopez ; Alexander W. Min ; Shahrnaz Azizi ; Minyoung Park ; Brent R. Carlton

Design and Analysis of Enhanced Mixer-First Receivers Achieving 40-dB/decade RF Selectivity
Sashank Krishnamurthy ; Ali M. Niknejad

A 24.5-43.5-GHz Ultra-Compact CMOS Receiver Front End With Calibration-Free Instantaneous Full-Band Image Rejection for Multiband 5G Massive MIMO
Min-Yu Huang ; Taiyun Chi ; Sensen Li ; Tzu-Yuan Huang ; Hua Wang

Multi-Mode 60-GHz Radar Transmitter SoC in 45-nm SOI CMOS
Wooram Lee ; Tolga Dinc ; Alberto Valdes-Garcia

A Code-Domain RF Signal Processing Front End With High Self-Interference Rejection and Power Handling for Simultaneous Transmit and Receive
Hussam Alshammary ; Cameron Hill ; Ahmed Hamza ; James F. Buckwalter

A Coupler-Based Differential mm-Wave Doherty Power Amplifier With Impedance Inverting and Scaling Baluns
Huy Thong Nguyen ; Hua Wang

A Wideband Low-Power Cryogenic CMOS Circulator for Quantum Applications
Andrea Ruffino ; Yatao Peng ; Fabio Sebastiano ; Masoud Babaie ; Edoardo Charbon

A 1.7-dB Minimum NF, 22-32-GHz Low-Noise Feedback Amplifier With Multistage Noise Matching in 22-nm FD-SOI CMOS
Bolun Cui ; John R. Long

A 39-GHz 64-Element Phased-Array Transceiver With Built-In Phase and Amplitude Calibrations for Large-Array 5G NR in 65-nm CMOS
Yun Wang ; Rui Wu ; Jian Pang ; Dongwon You ; Ashbir Aviat Fadila ; Rattanan Saengchan ; Xi Fu ; Daiki Matsumoto ; Takeshi Nakamura ; Ryo Kubozoe ; Masaru Kawabuchi ; Bangan Liu ; Haosheng Zhang ; Junjun Qiu ; Hanli Liu ; Naoki Oshima ; Keiichi Motoi ; Shinichi Hori ; Kazuaki Kunihiro ; Tomoya Kaneko ; Atsushi Shirane ; Kenichi Okada

Code-Domain Multiplexing for Shared IF/LO Interfaces in Millimeter-Wave MIMO Arrays
Manoj Johnson ; Armagan Dascurcu ; Kai Zhan ; Arman Galioglu ; Naresh Kumar Adepu ; Sanket Jain ; Harish Krishnaswamy ; Arun S. Natarajan

A 50-Gb/s PAM4 Si-Photonic Transmitter With Digital-Assisted Distributed Driver and Integrated CDR in 40-nm CMOS
Qiwen Liao ; Nan Qi ; Miaofeng Li ; Shang Hu ; Jian He ; Bozhi Yin ; Jingbo Shi ; Jian Liu ; Patrick Yin Chiang ; Xi Xiao ; Nanjian Wu

A 20-32-GHz Quadrature Digital Transmitter Using Synthesized Impedance Variation Compensation
Huizhen Jenny Qian ; Yiyang Shu ; Jie Zhou ; Xun Luo

Highly Integrated Guidewire Ultrasound Imaging System-on-a-Chip
Jaemyung Lim ; Coskun Tekes ; Evren F. Arkan ; Ahmad Rezvanitabar ; F. Levent Degertekin ; Maysam Ghovanloo

A High-Voltage Dual-Input Buck Converter Achieving 52.9% Maximum End-to-End Efficiency for Triboelectric Energy-Harvesting Applications
Inho Park ; Junyoung Maeng ; Minseob Shim ; Junwon Jeong ; Chulwoo Kim

An OTA-Less Second-Order VCO-Based CT ΔΣ Modulator Using an Inherent Passive Integrator and Capacitive Feedback
Shaolan Li ; David Z. Pan ; Nan Sun

A 102.2-dB, 181.1-dB FoM Extended Counting Analog-to-Digital Converter With Capacitor Scaling Saqib Mohamad ; Jie Yuan ; Amine Bermak
An 8.2- μ W 0.14-mm2 16-Channel CDMA-Like Capacitance-to-Digital Converter Yuxuan Luo ; Yida Li ; Aaron Voon-Yew Thean ; Chun-Huat Heng
A Time-Interleaved Resonant Voltage Mode Wireless Power Receiver With Delay-Based Tracking Loops for Implantable Medical Devices Se-Un Shin ; Minseong Choi ; Seungchul Jung ; Hyung-Min Lee ; Gyu-Hyeong Cho
A Wireless Power and Data Transfer Receiver Achieving 75.4% Effective Power Conversion Efficiency and Supporting 0.1% Modulation Depth for ASK Demodulation Dawei Ye ; Yu Wang ; Yingfei Xiang ; Liangjian Lyu ; Hao Min ; C.-J. Richard Shi
Mixer-First MIMO Receiver With Reconfigurable Multi-Port Decoupling and Matching Charley Wilson ; Jacob Dean ; Brian A. Floyd
A 30-GHz CMOS SOI Outphasing Power Amplifier With Current Mode Combining for High Backoff Efficiency and Constant Envelope Operation Kang Ning ; Yihao Fang ; Navid Hosseinzadeh ; James F. Buckwalter
TG-SPP: A One-Transmission-Gate Short-Path Padding for Wide-Voltage-Range Resilient Circuits in 28-nm CMOS Weiwei Shan ; Wentao Dai ; Chuan Zhang ; Hao Cai ; Peiye Liu ; Jun Yang ; Longxing Shi

IEEE Solid-State Circuits Letters

Volume 3 - 2020

A 0.58-to-0.9-V Input 0.53-V Output 2.4- μ W Current-Feedback Low-Dropout Regulator With 99.8% Current Efficiency Ziyu Wang ; Shahriar Mirabbasi
A Cryogenic CMOS Parametric Amplifier Mohammadreza Mehrpoo ; Fabio Sebastiano ; Edoardo Charbon ; Masoud Babaie
A 117-dB In-Band CMRR 98.5-dB SNR Capacitance-to-Digital Converter for Sub-nm Displacement Sensing With an Electrically Floating Target Hui Jiang ; Samira Amani ; Johan G. Vogel ; Saleh Heidary Shalmany ; Stoyan Nihtianov
A 2.6 TOPS/W 16-Bit Fixed-Point Convolutional Neural Network Learning Processor in 65-nm CMOS Shihui Yin ; Jae-Sun Seo
A 1-V 8.1- μ W PPG-Recording Front-End With > 92-dB DR Using Light-to-Digital Conversion With Signal-Aware DC Subtraction and Ambient Light Removal Fatemeh Marefat ; Reza Erfani ; Pedram Mohseni
Novel Pulse-Based Analog Divider With Digital Output Kuan-Hung Chen ; Tse-An Chen ; Chia-Ling Wei
Secondary Side-Channel Wireline Communication Using Transmitter Clock Frequency

Modulation
Yi Fan Zhang ; Joshua Liang ; Shayan Shahramian ; Behzad Dehlaghi ; Ryan Bespalko ; Michael O'Farrel ; Dustin Dunwell ; Davide Tonietto ; Anthony Chan Carusone

A Coarse-Fine VCO-ADC for MEMS Microphones With Sampling Synchronization by Data Scrambling
Andres Quintero ; Cesare Buffa ; Carlos Perez ; Fernando Cardes ; Dietmar Straeussnigg ; Andreas Wiesbauer ; Luis Hernandez

A Fully-Synthesizable Fractional-N Injection-Locked PLL for Digital Clocking with Triangle/Sawtooth Spread-Spectrum Modulation Capability in 5-nm CMOS
Bangan Liu ; Yuncheng Zhang ; Junjun Qiu ; Hongye Huang ; Zheng Sun ; Dingxin Xu ; Haosheng Zhang ; Yun Wang ; Jian Pang ; Zheng Li ; Xi Fu ; Atsushi Shirane ; Hitoshi Kurosu ; Yoshinori Nakane ; Shunichiro Masaki ; Kenichi Okada

A 3.2-GHz Quadrature Error Corrector for DRAM Transmitters, Using Replica Serializers and Pulse-Shrinking Delay Lines
Hyeongjun Ko ; Changho Hyun ; Joo-Hyung Chae ; Gi-Moon Hong ; Suhwan Kim

Design and Packaging of a Robust 120-GHz OOK Receiver Used in a Short-Range Dielectric Fiber Link
Simon Ooms ; Patrick Reynaert

610-GHz Fourth Harmonic Signal Reactively Generated in a CMOS Voltage Controlled Oscillator Using Differentially Pumped Varactors
Zhe Chen ; Zhiyu Chen ; Wooyeol Choi ; Kenneth K. O

An Implantable Body Channel Communication System With 3.7-pJ/b Reception and 34-pJ/b Transmission Efficiencies
Beomjin Yuk ; Byeongseol Kim ; Sanggeon Park ; Yeowool Huh ; Joonsung Bae

Design of a Boost DC-DC Converter With 82-mV Startup Voltage and Fully Built-in Startup Circuits for Harvesting Thermoelectric Energy
Jhe-Jia Jhang ; Hung-Hsien Wu ; Tien Hsu ; Chia-Ling Wei

A 2T-MONOS Embedded Flash Macro With 65-nm SOTB Technology Achieving 0.15-pJ/bit Read Energy With 80-MHz Access for IoT Applications
Ken Matsubara ; Tsutomu Nagasawa ; Yoshinobu Kaneda ; Hidenori Mitani ; Takashi Iwase ; Yasunobu Aoki ; Kohei Hashimoto ; Toshiaki Morioka ; Keiichi Maekawa ; Takashi Ito ; Hiroyuki Kondo ; Takashi Kono

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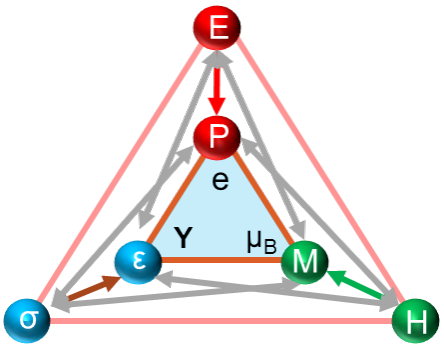

Volume 5: 2019 - December

Nonvolatile Spintronic Memory Cells for Neural Networks
Andrew W. Stephan ; Qiuwen Lou ; Michael T. Niemier ; Xiaobo Sharon Hu ; Steven J. Koester

Benchmarking Delay and Energy of Neural Inference Circuits
Dmitri E. Nikonov ; Ian A. Young

Energy-Efficient Convolutional Neural Network Based on Cellular Neural Network Using Beyond-CMOS Technologies
Chenyun Pan ; Qiuwen Lou ; Michael Niemier ; Sharon Hu ; Azad Naeemi

Ultracompact and Low-Power Logic Circuits via Workfunction Engineering
Talha F. Canan ; Savas Kaya ; Avinash Karanth ; Ahmed Louri

Early Access Articles

Accurate Inference with Inaccurate RRAM Devices: A Joint Algorithm-Design Solution Gouranga Charan ; Abinash Mohanty ; Xiaocong Du ; Gokul Krishnan ; Rajiv V. Joshi ; Yu Cao
A DNA Read Alignment Accelerator based on Computational RAM Zamshed I. Chowdhury ; Masoud Zabihi ; S. Karen Khatamifard ; Zhengyang Zhao ; Salonik Resch ; Meisam Razaviyayn ; Jian-Ping Wang ; Sachin S. Sapatnekar ; Ulya R. Karpuzcu
Analyzing the Effects of Interconnect Parasitics in the STT CRAM In-memory Computational Platform Masoud Zabihi ; Arvind K. Sharma ; Meghna G. Mankalale ; Zamshed I. Chowdhury ; Zhengyang Zhao ; Salonik Resch ; Ulya R. Karpuzcu ; Jian-Ping Wang ; Sachin S. Sapatnekar
Short-Term Long-Term Compute-In-Memory Architecture: A Hybrid Spin/CMOS Approach Supporting Intrinsic Consolidation Shadi Sheikhfaal ; Ronald F. DeMara
Energy-Efficient Moderate Precision Time-Domain Mixed-Signal Vector-by-Matrix Multiplier Exploiting 1T-1R Arrays Shubham Sahay ; Mohammad Bavandpour ; Mohammad Reza Mahmoodi ; Dmitri Strukov

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