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December 2018

NEWS

UPCOMING WEBINAR

"On-Chip Epilepsy Detection: Where Machine Learning Meets Personalized Wearable Healthcare"

Presented by Jerald Yoo
January 24, 2019, 10 AM ET

CLICK HERE TO REGISTER

Abstract: Epilepsy is a severe and chronic neurological disorder that affects over 65 million people worldwide. Yet current seizure/epilepsy detection and treatment largely relies on a physician interviewing the subject, which is not effective in infant/children group. Moreover, patient-to-patient and age-to-age variation on seizure pattern makes such detection particularly challenging; hence we need have a "personalized symptom detection". To expand the beneficiary group to even infants, and also to effectively adapt to each patient,

a wearable form-factor, patient-specific system with machine learning is of crucial.However, the wearable environment is challenging for circuit designers due unstable skin-electrode interface, huge mismatch, and static/dynamic offset.

This webinar will cover the design strategies of patient-specific epilepsy detection System-on-Chip (SoC). We will first explore the difficulties, limitations and potential pitfalls in wearable interface circuit design, and strategies to overcome such issues. Starting from a single op-amp instrumentation amplifier (IA), we will cover various IA circuit topologies and their key metrics to deal with offset compensation. Several state-of-the-art instrumentation amplifiers that emphasize on different parameters will also be discussed. Moving on, we will cover the feature extraction and the patient-specific classification using Machine Learning technique. Finally,an on-chip epilepsy detection and recording sensor SoC will be presented, which integrates all the components covered during the webinar. We will conclude with interesting aspects and opportunities that lie ahead.

Bio: Jerald Yoo (S'05-M'10-SM'15)received the B.S., M.S., and Ph.D. degrees in Department of Electrical Engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 2002, 2007, and 2010, respectively.

From 2010 to 2016, he was with the Department of Electrical Engineering and Computer Science, Masdar Institute, Abu Dhabi, United Arab Emirates, where he was an Associate Professor. From 2010 to 2011, he was also with Microsystems Technology Laboratories (MTL), Massachusetts Institute of Technology, as a visiting scholar. Since 2017, he has been with the Department of Electrical and Computer Engineering, National University of Singapore, Singapore, where he is currently an Associate Professor. He has pioneered researches on low-energy body-area-network (BAN) transceivers and wearable body sensor network using the planar-fashionable circuit board for continuous health monitoring system. He authored book chapters in IoT Physical Layer - Design and Implementation (Springer, 2019), Enabling the Internet of Things-From Circuits to Networks (Springer, 2017) and in Biomedical CMOS ICs (Springer, 2010). His current research interests include low-energy circuit technology for wearable bio signal sensors, flexible circuit board platform, BAN transceivers, ASIC for piezoelectric Micromachined Ultrasonic Transducers (pMUT) and System-on-Chip (SoC) design to system realization for wearable healthcare applications.

Dr. Yoo served as an IEEE Solid-State Circuits Society's Distinguished Lecturer (2017-2018). He is the recipient or a co-recipient of several awards: the IEEE International Circuits and Systems (ISCAS)2015 Best Paper Award (BioCAS Track), ISCAS 2015 Runner-Up Best Student Paper Award, the Masdar Institute Best Research Award in 2015 and the IEEE Asian Solid-State Circuits Conference (A-SSCC) Outstanding Design Awards (2005). He served as the Vice Chair of IEEE Solid-State Circuits Society (SSCS) United Arab Emirates (UAE) Chapter. Currently, he serves as a Technical Program Committee Member of the IEEE A-SSCC, IEEE Custom Integrated Circuits Conference (CICC), and the Secretary of the IEEE International Solid-State Circuits Conference (ISSCC) Student Research Preview (SRP). He is also an

Analog Signal Processing Technical Committee Member of IEEE Circuits and Systems Society.

Starting January 1, 2019, SSCS will be charging for CEU's and PDH's. Attendees of webinars will have to pay a fee to obtain CEU's and PDH's. However, webinar attendees can obtain a complimentary certificate of attendance.

SSCS Members Elevated to Fellow in 2019

Congratulations to the SSCS members who were elevated to the IEEE Grade of Fellow in 2019. The IEEE Grade of Fellow is conferred by the Board of Directors upon a person with an extraordinary record of accomplishments in any of the IEEE fields of interest. **Click here** for more information.

Elad Alon - for contributions to mixed-signal integrated circuit design and methodology

Lucien Breems - for contributions to over-sampled converters using complementary metal-oxide-semiconductor technology

Meng-Fan Chang - for contributions to static and nonvolatile memories for embedded systems

Christian Enz - for contributions to low-power analog circuit design

Maysam Ghovanloo - for contributions to implantable wireless integrated circuits and systems

Hossein Hashemi - for development of radio-frequency and optical phased-array integrated circuits

Nitin Jain - for leadership in the development of physics-based models for mm-wave System-on-Chip Ics

Chris Hyung-il Kim - for contributions to on-chip circuit reliability evaluation and characterization

Lee-sup Kim - for contributions to energy-efficient multimedia processor architectures

Farinaz Koushanfar - for contributions to hardware and embedded systems security and to privacy-preserving computing

Pui-in Mak - for contributions to radio-frequency and analog circuits

Katsufumi Nakamura - for contributions to integrated circuits for digital imaging

Samar Saha - for contributions to compact modeling of silicon field-effect transistors

Shaojun Wei - for leadership in integrated circuits engineering of smart cards and reconfigurable devices

Jared Zerbe - for contributions to the development of high-performance serial interfaces

Lin Zhong - for contributions to the development of energy-efficient driver circuits for organic light-emitting diodes

Higher Grade SSCS Members Can Join

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As a High Grade Member of the IEEE Solid-State Circuits Society, you can add **IEEE Circuits and Systems Society (CASS)** annual membership for just $5.

If you have not yet renewed for 2019, join CASS for just $5 by entering promotion code **SSCXCAS2019** at checkout. If you have already renewed for 2019, sign in with your **IEEE account** and the discounted CASS membership will appear in your cart.

Please note that this offer is **NOT** for Students or Graduate Students.

If you have any questions, please contact Lauren Caruso at **l.caruso@ieee.org**

PUBLICATIONS

The latest in SSCS Flagship Publications...

IEEE Solid-State Circuits Letters

Volume 1, Issue 6, June 2018

A Method to Improve Reliability in a 65-nm SRAM PUF Array **Yizhak Shifman ; Avi Miller ; Osnat Keren ; Yoav Weizmann ; Joseph Shor**
A Fully Integrated 11.2-mm2a-IGZO EMG Front-End Circuit on Flexible Substrate Achieving Up to 41-dB SNR and 29-MÎInput Impedance **Carmine Garripoli ; Sahel Abdinia ; Jan-Laurens J. P. van der Steen ; Gerwin H. Gelinck ; Eugenio Cantatore**
1/fNoise Reduction Using In-Pixel Chopping in CMOS Image Sensors **Kapil Jainwal ; Chandani Anand ; Mukul Sarkar**
A fW- and kHz-Class Feedforward Leakage Self-Suppression Logic Requiring No External Sleep Signal to Enter the Leakage Suppression Mode **Joao P. Cerqueira ; Jiangyi Li ; Mingoo Seok**
A Digital LDO With Co-SA Logics and TSPC Dynamic Latches for Fast Transient Response **Lei Zhao ; Yan Lu ; Rui P. Martins**

IEEE Journal of Solid-State Circuits

Vol. 53, Issue 12, December 2018

Special Issue on the 2018 IEEE International Solid-State Circuits Conference (ISSCC)

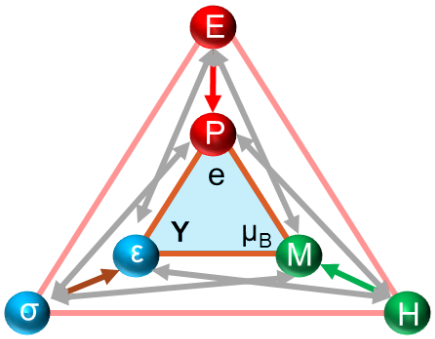
Introduction to the Special Issue on the 2018 IEEE International Solid-State Circuits Conference (ISSCC) **Yong-Ping Xu ; Tai-Haur Kuo ; Matt Straayer ; Harish Krishnaswamy ; Arun Natarajan**
A 0.25 mm2-Resistor-Based Temperature Sensor With an Inaccuracy of 0.12°C (3σ) From -55°C to 125 °C **Sining Pan ; Kofi A. A. Makinwa**
A Compact Resistor-Based CMOS Temperature Sensor With an Inaccuracy of 0.12 °C and a Resolution FoM of 0.43 pJ K2 in 65-nm CMOS **Woojun Choi ; Yongtae Lee ; Seonhong Kim ; Sanghoon Lee ; Jieun Jang ; Junhyun Chun ; Kofi A. A. Makinwa ; Youngcheol Chae**
A ±4-A High-Side Current Sensor With 0.9% Gain Error From -40°C to 85°C Using an Analog Temperature Compensation Technique **Long Xu ; Johan H. Huijsing ; Kofi A. A. Makinwa**
A Low Quiescent Current, Low THD+N Class-D Audio Amplifier With Area-Efficient PWM-Residual-Aliasing Reduction **Shih-Hsiung Chien ; Yi-Wen Chen ; Tai-Haur Kuo**
A CMOS Dual-RCFrequency Reference With Â±200-ppm Inaccuracy From -45°C to 85°C **Çağrı Gürleyük ; Lorenzo Pedalà ; Sining Pan ; Fabio Sebastiano ; Kofi A. A. Makinwa**
A cm-Scale 2.4-GHz Wireless Energy Harvester With NanoWatt Boost Converter and Antenna-Rectifier Resonance for WiFi Powering of Sensor Nodes **Kamala Raghavan Sadagopan ; Jian Kang ; Yogesh Ramadass ; Arun Natarajan**
MISIMO: A Multi-Input Single-Inductor Multi-Output Energy Harvesting Platform in 28-nm FDSOI for Powering Net-Zero-Energy Systems **Sally Safwat Amin ; Patrick P. Mercier**
A Shock-Optimized SECE Integrated Circuit **Adrien Morel ; Anthony Quelen ; Pierre Gasnier ; Romain Grézaud ; Stéphane Monfray ; Adrien Badel ; Gaël Pillonnet**
A 1-2-MHz 150-400-V GaN-Based Isolated DC-DC Bus Converter With Monolithic Slope-Sensing ZVS Detection **Lin Cong ; Hoi Lee**
Integrated Gate Drivers Based on High-Voltage Energy Storing for GaN Transistors **Achim Seidel ; Bernhard Wicht**
Algorithmic Voltage-Feed-In Topology for Fully Integrated Fine-Grained Rational Buck-Boost Switched-Capacitor DC-DC Converters **Yang Jiang ; Man-Kay Law ; Pui-In Mak ; Rui P. Martins**
A 15.2-ENOB 5-kHz BW 4.5-uW Chopped CT Delta Sigma-ADC for Artifact-Tolerant Neural Recording Front Ends **Hariprasad Chandrakumar ; Dejan Marković**
A 13-ENOB Second-Order Noise-Shaping SAR ADC Realizing Optimized NTF

Zeros Using the Error-Feedback Structure **Shaolan Li ; Bo Qiao ; Miguel Gandara ; David Z. Pan ; Nan Sun**
A 280uW Dynamic Zoom ADC With 120 dB DR and 118 dB SNDR in 1 kHz BW **Shoubhik Karmakar ; Burak Gönen ; Fabio Sebastiano ; Robert van Veldhoven ; Kofi A. A. Makinwa**
A 24-72-GS/s 8-b Time-Interleaved SAR ADC With 2.0-3.3-pJ/Conversion and >30 dB SNDR at Nyquist in 14-nm CMOS FinFET **Lukas Kull ; Danny Luu ; Christian Menolfi ; Matthias Brändli ; Pier Andrea Francese ; Thomas Morf ; Marcel Kossel ; Alessandro Cevrero ; Ilter Ozkaya ; Thomas Toifl**
A 16-bit 12-GS/s Single-/Dual-Rate DAC With a Successive Bandpass Delta-Sigma Modulator Achieving <-67-dBc IM3 Within DC to 6-GHz Tunable Passbands **Shiyu Su ; Mike Shuo-Wei Chen**
An Inverse-Class-F CMOS Oscillator With Intrinsic-High-Q First Harmonic and Second Harmonic Resonances **Chee Cheow Lim ; Harikrishnan Ramiah ; Jun Yin ; Pui-In Mak ; Rui P. Martins**
A Sub-mW Fractional-N ADPLL With FOM of -246 dB for IoT Applications **Hanli Liu ; Dexian Tang ; Zheng Sun ; Wei Deng ; Huy Cu Ngo ; Kenichi Okada**
A Type-I Sub-Sampling PLL With a100x100 um2 Footprint and a -255-dB FOM **Ahmad Sharkia ; Shahriar Mirabbasi ; Sudip Shekhar**
A 23-GHz Low-Phase-Noise Digital Bang-Bang PLL for Fast Triangular and Sawtooth Chirp Modulation **Dmytro Cherniak ; Luigi Grimaldi ; Luca Bertulessi ; Roberto Nonis ; Carlo Samori ; Salvatore Levantino**
A PVT-Tolerant >40-dB IRR, 44% Fractional-Bandwidth Ultra-Wideband mm-Wave Quadrature LO Generator for 5G Networks in 55-nm CMOS **Farshad Piri ; Matteo Bassi ; Niccolò R. Lacaita ; Andrea Mazzanti ; Francesco Svelto**
A Linear High-Efficiency Millimeter-Wave CMOS Doherty Radiator Leveraging Multi-Feed On-Antenna Active Load Modulation **Huy Thong Nguyen ; Taiyun Chi ; Sensen Li ; Hua Wang**
A 128-Pixel System-on-a-Chip for Real-Time Super-Resolution Terahertz Near-Field Imaging **Philipp Hillger ; Ritesh Jain ; Janusz Grzyb ; Wolfgang Förster ; Bernd Heinemann ; Gaëtan MacGrogan ; Patrick Mounaix ; Thomas Zimmer ; Ullrich R. Pfeiffer**
A 60-GHz Transceiver and Baseband With Polarization MIMO in 28-nm CMOS **Kaushik Dasgupta ; Saeid Daneshgar ; Chintan Thakkar ; Shinwon Kang ; Anandaroop Chakrabarti ; Shuhei Yamada ; Nathan Narevsky ; Debabani Choudhury ; James E. Jaussi ; Bryan Casper**
A Millimeter-Wave Polarization-Division-Duplex Transceiver Front-End With an On-Chip Multifeed Self-Interference-Canceling Antenna and an All-Passive Reconfigurable Canceller **Taiyun Chi ; Jong Seok Park ; Sensen Li ; Hua Wang**
A 60-GHz 144-Element Phased-Array Transceiver for Backhaul Application **Tirdad Sowlati ; Saikat Sarkar ; Bevin George Perumana ; Wei Liat Chan ; Anna Papio Toda ; Bagher Afshar ; Michael Boers ; Donghyup Shin ; Timothy R. Mercer ; Wei-Hong Chen ; Alfred Grau Besoli ; Seunghwan Yoon ; Sissy Kyriazidou ; Phil Yang ; Vipin Aggarwal ; Nooshin Vakilian ; Dmitriy Rozenblit ; Masoud Kahrizi ; Joy Zhang ; Alan Wang ; Padmanava Sen ; David Murphy ; Ali Sajjadi ; Alireza Mehrabani ; Evangelos Kornaros ; Khim Low ; Koji Kimura ; Vincent Roussel ; Hongyu Xie ; Venkat Kodavati**
All-Digital PLL for Bluetooth Low Energy Using 32.768-kHz Reference Clock and <0.45-V Supply **Chao-Chieh Li ; Min-Shueh Yuan ; Chia-Chun Liao ; Yu-Tso Lin ; Chih-Hsien Chang ; Robert Bogdan Staszewski**

A DPLL-Centric Bluetooth Low-Energy Transceiver With a 2.3-mW Interference-Tolerant Hybrid-Loop Receiver in 65-nm CMOS Hanli Liu ; Zheng Sun ; Dexian Tang ; Hongye Huang ; Tohru Kaneko ; Zhijie Chen ; Wei Deng ; Rui Wu ; Kenichi Okada
An 802.11ax 4x4 High-Efficiency WLAN AP Transceiver SoC Supporting 1024-QAM With Frequency-Dependent IQ Calibration and Integrated Interference Analyzer Shusuke Kawai ; Rui Ito ; Kengo Nakata ; Yutaka Shimizu ; Motoki Nagata ; Tomohiko Takeuchi ; Hiroyuki Kobayashi ; Katsuyuki Ikeuchi ; Takayuki Kato ; Yosuke Hagiwara ; Yuki Fujimura ; Kentaro Yoshioka ; Shigehito Saigusa ; Hiroshi Yoshida ; Makoto Arai ; Toshiyuki Yamagishi ; Hirotsugu Kajihara ; Kazuhisa Horiuchi ; Hideki Yamada ; Tomoya Suzuki ; Yuki Ando ; Kensuke Nakanishi ; Koichiro Ban ; Masahiro Sekiya ; Yoshimasa Egashira ; Tsuguhide Aoki ; Kohei Onizuka ; Toshiya Mitomo

IEEE Journal on Exploratory Solid-State Computational Devices and Circuits

Volume 4, 2018



Circuit Models for Spintronic Devices Subject to Electric and Magnetic Fields Meshal Alawein ; Hossein Fariborzi
Complementary Logic Implementation for Antiferromagnet Field-Effect Transistors Chenyun Pan ; Azad Naeemi
Evaluation of Operating Margin and Switching Probability of Voltage- Controlled Magnetic Anisotropy Magnetic Tunnel Junctions Jeehwan Song ; Ibrahim Ahmed ; Zhengyang Zhao ; Delin Zhang ; Sachin S. Sapatnekar ; Jian-Ping Wang ; Chris H. Kim
Towards a Strong Spin-Orbit Coupling Magnetoelectric Transistor Peter A. Dowben ; Christian Binek ; Kai Zhang ; Lu Wang ; Wai-Ning Mei ; Jonathan P. Bird ; Uttam Singisetti ; Xia Hong ; Kang L. Wang ; Dmitri Nikonov
Using Programmable Graphene Channels as Weights in Spin-Diffusive Neuromorphic Computing Jiaxi Hu ; Gordon Stecklein ; Yoska Anugrah ; Paul A. Crowell ; Steven J. Koester
BCB Evaluation of High-Performance and Low-Leakage Three-Independent-Gate Field Effect Transistors Jorge Romero-Gonzalez ; Pierre-Emmanuel Gaillardon
Tunnel FET Analog Benchmarking and Circuit Design Hao Lu ; Paolo Paletti ; Wenjun Li ; Patrick Fay ; Trond Ytterdal ; Alan Seabaugh
Improving Energy Efficiency of Low Voltage Logic by Technology-Driven Design Kaushik Vaidyanathan ; Daniel H. Morris ; Uygar E. Avci ; Huichu Liu ; Tanay Karnik ; Hong Wang ; Ian A. Young
Inversion Charge Boost and Transient Steep-Slope Induced by Free-Charge-Polarization Mismatch in a Ferroelectric-Metal-Oxide-Semiconductor Capacitor

Sou-Chi Chang ; Uygar E. Avci ; Dmitri E. Nikonov ; Ian A. Young
Performance Characterization and Majority Gate Design for MESO-Based Circuits **Zhaoxin Liang ; Meghna G. Mankalale ; Jiaxi Hu ; Zhengyang Zhao ; Jian-Ping Wang ; Sachin S. Sapatnekar**

JxCDC papers listed in order of popularity can be found online HERE.

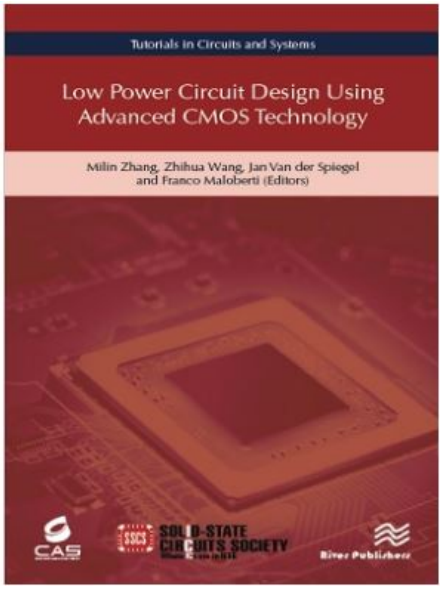
For paper submission details, click HERE.

EDUCATION

January 2019 Distinguished Lectures

SSCS Singapore	Energy-Efficient High-Resolution ADCs, Presented by Youngcheol Chae	January 14, 2019	National University of Singapore **For more information, please click here**

New eBook Available for Free for SSCS Members



Low Power Circuit Design Using Advanced CMOS Technology (Editors Milin Zhang, Zhihua Wang, Jan Van der Spiegel, and Franco Maloberti) is available for free for all SSCS Members on the SSCS Resource Center.

Click here to download

This book is a summary of lectures from the first Advanced CMOS Technology School (ACTS) summer 2017. The slides are selected from the handouts, while the text was edited according to the lecturers talk.

ACTS is an example of high-level continuous education for junior engineers, teachers in academe, and students. ACTS was the results of a successful collaboration between societies, the local chapter leaders, and industry leaders. This summer school was the brainchild of Dr. Zhihua Wang, with strong support from volunteers from both the IEE SCS and CASS. In addition, the local companies, Synopsys China and Beijing IC Park, provided financial support.

CONFERENCES

Upcoming SSCS-Sponsored Conferences

2019 IEEE International Solid-State Circuits Conference (ISSCC) San Francisco, CA	**February 17 - 19, 2019**
2019 Design, Automation & Test in Europe Conference and Exhibition Florence, Italy	**March 25 - 29, 2019**
2019 IEEE Custom Integrated Circuits Conference (CICC) Austin, TX	**April 21 - 24, 2019**
2019 International Symposium on VLSI Design, Automation and Test (VLSI-DAT) Hsinchu, Taiwan	**April 22 - 25, 2019**
2019 IEEE Radio Frequency Integrated Circuits Symposium (RFIC) Boston, MA	**June 2 - 4, 2019**
ESSCIRC 2019 - IEEE 45th European Solid-State Circuits Conference (ESSCIRC) Cracow, Poland	**September 23 - 26, 2019**
2019 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS) Nashville, TN	**November 3 - 6, 2019**

SSCS-Sponsored Conferences: Proceedings

Click the links below to access 2018 SSCS-Sponsored conference proceedings.

2018 IEEE International Solid-State Circuits Conference (ISSCC)
2018 IEEE Custom Integrated Circuits Conference (CICC)
2018 IEEE Symposium on VLSI Circuits (VLSI)
2018 IEEE 44th European Solid-State Circuits Conference (ESSCIRC)
2018 IEEE Asian Solid-State Circuits Conference

ISSCC 2019 Advance Registration is Now Open

Advance Registration is open through January 27, 2019. Early Registration rates available through January 8, 2019.

CLICK HERE FOR MORE INFORMATION

The International Solid-State Circuits Conference (ISSCC) will be held February 17-21, 2019 at the San Francisco Marriott Marquis, San Francisco, California. ISSCC is the foremost global forum for presentation of advances in solid-state circuits and systems-on-a-chip. The Conference offers a unique opportunity for engineers

working at the cutting edge of IC design and application to maintain technical currency, and to network with leading experts.

Plenary Talks (Monday, February 18, 2019)

- The Next Challenge in AI: Self-Supervised Learning - Yann LeCun, Facebook AI Research and New York University, New York, NY
- Intelligence on Silicon: From Deep Neural Network Accelerators to Brain-Mimicking AI-SoCs - Hoi-Jun Yoo, KAIST, Daejeon, Republic of Korea
- Integration of Photonics and Electronics - Meint K. Smit, Eindhoven University of Technology, Eindhoven, The Netherlands
- 5G Wireless Communication: An Inflection Point - Vida Ilderem, Intel, Hillsboro, Oregon

Tutorials (Sunday, February 17, 2019)

- Fundamentals of Integrated Radars - Brian Ginsburg, Texas Instruments, Dallas, TX
- Fundamentals of Power Conversion Topologies - Robert Pilawa-Podgurski, University of California, Berkeley, Berkeley, CA
- Advances and Prospects for In-Memory Computing - Naveen Verma, Princeton University, Princeton, NJ
- Fundamentals of Efficient IoT Microcontrollers - James Myers, ARM, Cambridge, United Kingdom
- Noise Shaping in Data Converters - Venkatesh Srinivasan, Texas Instruments, Dallas, TX
- Basics of Clock and Data Recovery Circuits - Amir Amirkhany, Samsung Electronics, San Jose, CA
- Hardware Security - from Basics to ASICs - Massimo Alioto, National University of Singapore, Singapore
- Current-Sensing Techniques - Mahdi Kashmiri, Robert Bosch Research and Technology Center, Sunnyvale, CA
- Calibration Techniques for Wireless Transceivers - David McLaurin, Analog Devices, Raleigh, NC
- Low-Noise Sensor Interfaces - Pedram Lajevardi, Robert Bosch Research and Technology Center, Sunnyvale, CA

Forums (February 17 and February 18, 2019)

- Sub-6GHz 5G Radio Circuits and Systems: From Concepts to Silicon
- Memory-Centric Computing from IoT to Artificial Intelligence and Machine Learning
- The Complete ADAS Sensing Network
- Intelligence at the Edge: How Can We Make Machine Learning More Energy Efficient?
- 56Gb/s to 112Gb/s and Beyond - Design Challenges and Solutions in Wireline Communications
- The Right Tool for the Job: Application Optimized Data Converters

Evening Events (February 17 - 19, 2019)

- Women in Circuits Workshop: "How to Save a Life with Circuits"
- Moving to 'The Dark Side'
- How Can Hardware Designers Reclaim the Spotlight?

Student Activities (Sunday, February 17, 2019)

- Student Research Preview (SRP): Short Presentations with Poster Session
- Silkroad Award: Scholarships awarded for Far-East full-time students

Industry Showcase (February 18, 2019)

Demonstration Session (February 18 - 19, 2019)

Technical Sessions (February 18 - 20, 2019)

Short Course (February 21, 2019)
Integrated Phased Arrays: Theory, Practice, and Implementation for 5G and Beyond

- Introduction to Phased Array Technology from mmWave to Optics - Hossein Hashemi, University of Southern California, Los Angeles, CA
- Scalable mmWave Phased Arrays for Imaging and 5G Communications - Bodhisatwa Sadhu, IBM Thomas J. Watson Research Center, Yorktown Heights, NY
- Challenges and Architectures for Large-Scale Next-Generation Phased Arrays and 5G Systems - Shahriar Shahramian, Bell Laboratories/Nokia, Murray Hill, NJ
- Emerging Topics in Phased Arrays and the Path to THz - Ehsan Afshari, University of Michigan, Ann Arbor, MI

DATE 2019 in Florence: Advance Program now Available

View the advance program here: https://www.date-conference.com/programme

The DATE conference will take place from 25 to 29 March 2019 at the Firenze Fiera in Florence, Italy. It combines the world's favorite electronic systems design and test conference with an international exhibition for electronic design, automation and test, from system-level hardware and software implementation right down to integrated circuit design.

On the first day of the DATE week, six in-depth technical tutorials on the main topics of DATE as well as two industry hands-on tutorials will be given by leading experts in their respective fields. The topics cover Machine Learning for Manufacturing and Test, OpenCL Design Flows for FPGAs, Approximate Computing, Hardware-based Security, Co-simulation, and Safety and Security in Automotive, while the hands-on tutorials are on Quantum Computing with IBM Q and on Python Productivity for Xilinx Zynq.

During the Opening Ceremony on Tuesday, plenary keynote lectures will be given by Kenneth P. Caviasca, Vice President of Internet of Things Group and General Manager of Architecture, Silicon and Platform Engineering at Intel, and Jürgen Bortolazzi, Director Driver Assistance Systems at Porsche. On the same day, the Executive Track offers a series of business panels with executive speakers from companies leading the design and automation industry, discussing hot topics. Furthermore, a talk by Claudio Giorgione, Curator of the Leonardo Department at the National Museum of Science and Technology Milano, will give insight into live and work of Leonardo da Vinci in line with the 500th anniversary of his death, which is celebrated in Florence in 2019.

The main conference programme from Tuesday to Thursday includes 58 technical sessions organized in parallel tracks from the four areas:

D - Design Methods & Tools
A - Application Design
T - Test, Reliability, and Robustness
E - Embedded and Cyber-physical Systems

and from several special sessions on Hot Topics, such as Emerging Design Technologies, Design and Test of Secure Systems, IoT Security, Embedded Systems for Deep Learning, Augmented Living and Personalized Healthcare, Robotics and Industry 4.0., as well as results and lessons learned from European projects. Additionally, there are numerous Interactive Presentations which are organized into five IP sessions.

Two Special Days in the programme will focus on areas bringing new challenges to the system design community: Embedded Meets Hyperscale and HPC and Model-Based Design of

Intelligent Systems. Each of the Special Days will have a full programme of keynotes, panels, tutorials and technical presentations.

Heterogeneous computing with multiple, specialized processors and application-specific accelerators is vital for embedded systems to meet performance, latency, and efficiency targets. The same goals of fast, efficient, and cost-effective processing are also gating factors for the evolution of hyperscale data center (DC) and high-performance computing (HPC) and Moore's law no longer provides the necessary efficiency gains. The theme of the special day Embedded Meets Hyperscale and HPC is to highlight this confluence of methods and technologies to better understand, how heterogeneous computing is shaping the future of hyperscale DCs and HPC.

The special day on Model-Based Design of Intelligent Systems will explore all that is needed to lift model-based design into the era of intelligent systems. Topics addressed are, among others, model-based design frameworks for IoT systems, model-based machine learning, and application of model-based design in safety-critical and autonomous systems. The special day will also highlight the upcoming challenges in this domain and invite the DATE community to help overcome them.

To inform attendees on commercial and design-related topics, there will be a full programme in the Exhibition Theatre which will combine presentations by exhibiting companies, best-practice reports by industry leaders on their latest design projects and selected conference special sessions. Two of the highlights here will be a career session called Inspiring Futures!,where interested companies may introduce their work and job portfolios, and the newly created Publisher's Session.
The conference is complemented by an exhibition, running for three days (Tuesday - Thursday), including exhibition booths from companies, and collaborative research initiatives including EU project presentations.The exhibition provides a unique networking opportunity and states the perfect venue for industries to meet University Professors to foster University Programme and especially for PhD Students to meet future employers.

On Friday, 10 full-day workshops cover several hot topics from areas like (a) Open Source and Machine Learning in EDA, (b) Emerging Techniques for Memories, Interconnections, and Quantum Computing, (c) Hardware Design, Synthesis, and Approximate Computing, as well as EDA in application domains such as (d) Autonomous Systems and IoT.

For further information please visit: **www.date-conference.com**

CALL FOR PAPERS

2019 IEEE Symposia on VLSI Circuits -Call for Papers

The VLSI Symposia is an international conference on semiconductor technology and circuits that offers an opportunity to interact and synergize on topic ranging from process technology to systems-on-chip.

The 2019 Symposia on VLSI Technology and Circuits will be held June 9 - 14 in Kyoto, Japan at the RIHGA Royal Hotel.

The Circuits Symposium is placing special emphasis on several Innovative System focus areas, and encourages paper submissions on:

- Machine and deep learning
- Internet of Things
- Industrial electronics

- Big Data management
- Biomedical Applications
- Robotics and autonomous transportation

New focus sessions comprising invited and contributed papers will be offered.

In addition, submissions are welcomed in all of the following circuits areas:

- Processors, SoCs, and Machine Learning
- Digital circuits, signal integrity, and IOs
- Hardware security
- Memory circuits, architectures, and interfaces
- Biomedical circuits
- Sensors, imagers, and display circuits
- Power conversion circuits
- Analog, amplifier and filter circuits
- Wireless receivers and transmitters
- Data converters
- Frequency generation and clock circuits
- Wireline receivers and transmitters

Call for Workshop - The call for proposals for the Sunday Workshop is now open. You organize the workshop, VLSI provides the venue. Check the details in: **www.vlsisymposium.org**.

Prospective authors must submit two-page camera-ready papers and abstracts using the Symposia's website, **www.vlsisymposium.org**.

Accepted papers will be published as submitted, with no revisions permitted. Authors must follow detailed instructions provided within the "Authors" section of the website, including the Authors' Guide and Pre-publication Policy. Extended versions of selected papers from the Symposium will be published in a Special Issue of the IEEE Journal of Solid-State Circuits.

Paper Submission Deadline is Monday, January 28, 2019 at 23:59 JST.

CALL FOR PAPERS
RFIC 2019: IEEE Radio Frequency Integrated Circuits Symposium

The 2019 IEEE Radio Frequency Integrated Circuits Symposium (RFIC 2019) will be held 2-4 June 2019 at the Boston Convention and Exhibition Center in Boston, MA, USA. For the latest information, please visit: rfic-ieee.org.

Electronic Paper Submission/Communication: Technical papers must be submitted via the RFIC 2019 website at rfic-ieee.org. Hard copies will not be accepted. Complete information on how and when to submit a paper can be found on the RFIC 2019 website. As in last year, a double-blind review process will be followed.

Technical Areas: The symposium solicits papers describing original work in all areas related to RF and millimeter-wave integrated circuits and systems. Work

should be demonstrated through integrated-circuit hardware results.

Original contributions are solicited in areas including but not limited to the following:

- **Wireless Cellular and Connectivity:** innovative circuit and system-on-chip concepts related to wireless applications below 6GHz, including those designed for existing and emerging standards such as 2G/3G/4G/5G (sub-6GHz), LTE, WWAN, WLAN, BT, GPS, FM, and UWB.
- **Low Power Transceivers:** RF circuits designed for extremely low power or harvested-energy operation, wake-up receivers, SOCs designed for operation within emerging RFID, NFC, Zigbee, 802.15.4, WPAN, WBAN, Biomedical, Sensor Nodes, or IR-UWB applications
- **Receiver Components and Circuits:** LNAs, mixers, VGAs, stand-alone phase shifters, T/R switches, integrated FEM, amplifiers, filters, demodulators, for RF through millimeter-wave frequencies
- **Analog and Mixed-Signal Blocks and SOCs:** RF and baseband converters (ADC/DAC), sub-sampling/over-sampling circuits, converters for digital beamforming, converters for emerging TX and RX architectures, power (DC-DC) converters for RF applications, I/O transceivers and CDRs for wireline and optical connectivity
- **Reconfigurable and Tunable Front-Ends:** SDR/cognitive radio, N-path receivers/filters, wideband/multi-band front-ends, interference cancellation, full-duplex, adaptive front-ends
- **Transmitter Sub-Systems and Power Amplifiers:** power amplifiers, drivers, modulators, digital transmitters, advanced TX circuits, linearization and efficiency enhancement techniques, for RF through millimeter-wave frequencies
- **Oscillators:** VCOs, injection-locking frequency dividers/multipliers
- **Frequency Synthesis:** PLLs, DLLs, MDLLS, DDS, LO drivers, frequency dividers
- **Device Technologies, Packaging, Modeling, and Testing:** RF device technology (both silicon and compound semiconductors) MEMS, integrated passives, photonic, reliability, packaging, modeling and testing, EM modeling/co-simulation, built-in-self-test (BIST)
- **Millimeter- and Sub-Millimeter Wave Communication and Sensing Systems:** >20GHz SoCs/SiPs for wireless communication (5G mm-wave, WiGig, 802.11ay), phased-arrays, imaging, radar, spectroscopy, and remote sensing
- **Emerging Circuit Technologies (NEW This Year):** RF circuits and systems incorporating MEMs sensors and actuators, heterogeneous and 3D ICs, silicon photonics, quantum computing ICs, hardware security, and machine learning applications, Wearable systems, Biomedical applications, autonomous systems e.g. automotive and drones Implantable systems

Electronic Submission Deadlines:
Technical Paper in PDF Format - 14 January 2019
Final Manuscripts for the Digest and USB - 22 March 2019

All submissions must be made at **rfic-ieee.org** in PDF form. Hard copies are not accepted.

UPCOMING EVENTS

Students and Young Professionals Micro-Mentoring and Career Coaching Session at ISSCC 2019

Sponsored by the IEEE Solid-State Circuits Society Young Professionals

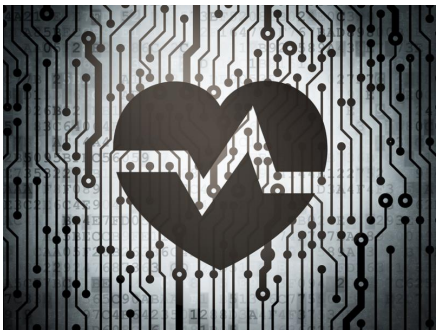
Tuesday, February 19, 2019
6:00 PM - 7:00 PM
Pacific A/B Room
San Francisco Marriott Marquis

Complimentary event for all students, faculty, and engineers within 15 years of their first degree.

- **Leading experts from industry and academia, IEEE SSCS Executives, and Distinguished Leaders will share their experiences**
- **1 on 1 answers to all your questions on publications, entrepreneurship, industry vs. academia and career coaching.**
- **Complimentary giveaways for attendees**
- **Free SSCS student membership offer for event attendees**

Learn about SSCS member benefits for young engineers & students, such as complimentary tutorials and short courses, webinars, distinguished lecturers to present at your region, networking with 10,000 + SSCS members around the globe, latest technical content, Student fellowships programs and more.

Click here to RSVP (walk-in's welcome!)



ISSCC Evening Event - How to Save Lives with Circuits

Sunday, February 17, 2019 at 6:00 PM
San Francisco, California Marriott Marquis

The workshop highlights circuits and their impact on healthcare-related industries. The goal of the panel is to provide perspectives from system architects, security experts and circuit designers on where we should be heading with the large amount of data that is being generated from more-advanced tests and increased monitoring of our current health status.

Distinguished Speakers

6:00 - 6:30 PM
Catalyzing Growth and Innovation
Sue Siegel
GE Chief Innovation Officer and CEO, GE Business Innovations

6:30 - 7:00 PM
Better Circuits for a Better World
Dr. Jennifer Lloyd
VP, Healthcare and Consumer, Analog Devices

Invited Talks

7:00 - 7:20 PM
Unravelling the Brain with High-Density CMOS Neural Probes
Dr. Carolina Mora Lopez
Team Leader Circuits for Neural Interfaces at imec

7:20 - 7:40 PM
Neurotechnology: where engineering meets neuroscience
Dr. Hyunjoo J. Lee
Assistant Professor Electrical Engineering, KAIST

Panel: What Can Circuit Designers Do to Bolster Security in AI-driven Healthcare

7:45 - 9:00 PM
Moderator: Ingrid Verbauwhede, KU Leuven, Leuven, Belgium

Distinguished Speaker

7:45 -8:15 PM
Perspectives on Machine Learning and Cryptography By Turning Award Winner Shafi Goldwasser
Shafi Goldwasser
Professor Electrical Engineering and Computer Sciences, University of California at Berkeley, Berkeley, CA

Panelists

Alison Burdett, Sensium Healthcare, Abingdom, United Kingdom
Shafi Goldwasser, University of California at Berkeley, Berkeley, CA
Rikky Muller, University of California at Berkeley, Berkeley, CA
Sugako Otani, Renesas Electronics Corporation, Tokyo, Japan
Vivienne Sze, Massachusetts Institute of Technology, Cambridge, MA
Wenyuan Xu, Zhejiang University, Hangzhou, China

IEEE NEWS

2019 IEEE Medals & Recognitions to Be Presented at 2019 IEEE VIC Summit & Honors Ceremony

The **IEEE Vision, Innovation, and Challenges (VIC) Summit** brings together leading innovators, visionaries, and disruptors in technology to discuss, explore, and uncover what is imminent, what is possible, and what these

emerging technologies mean for our future. This is a unique opportunity to connect with, learn from, and build partnerships with some of the technology "Giants" in the world. Topics at the 2019 VIC Summit will include AI/Machine Learning, IoT/Smart Networks, Cybersecurity ... and more!

The VIC Summit culminates with the **Honors Ceremony Gala**, an evening's festivities that will include the celebration of the contributions of some of the greatest minds of our time who have made a lasting impact on society for the benefit of humanity.

Visit **http://ieee-vics.org/** for information.

For more information about the IEEE Awards Program, visit **www.ieee.org/awards** or e-mail **awards@ieee.org**.

Seeking News

Please send any chapter news or happenings (Distinguished Lecturer visits, events hosted by your SSCS chapter, awards received by members, etc) to Abira Altvater, SSCS Magazine News Editor, for inclusion in an upcoming issue of the magazine. Please email - **Abira.Altvater@ieee.org**. We look forward to receiving your news articles!

For more chapter news, check out the Fall 2018 issue of the Solid-State Circuits Magazine.