IEEE SOLID-STATE CIRCUITS SOCIETY

Where ICs are in IEEE

August 2018

NEWS

UPCOMING WEBINAR

Design Techniques for Scalable, Sub-pJ/b Serial I/O Transceivers
Wednesday, September 12th
1:00 PM ET

Abstract: In order to meet the inter-chip bandwidth demands of future systems and comply with limited IC power budgets, both chip-to-chip data rates and I/O energy efficiency must improve. This is a significant challenge for electrical interconnect architectures, which currently offer the lowest-cost solutions, as the frequency-dependent loss of conventional electrical channels prohibit significant data rate scaling without efficient equalizer circuits. This talk will discuss key design techniques that enable scalable, sub-pJ/b serial I/O transceivers. The first part of the talk will discuss low power transmitter and receiver designs capable of low-voltage operation and fast power-state transitioning. Next, low-complexity clocking architectures are detailed. The talk concludes with a discussion on low-power equalizer circuits that enable the support of higher data rates over lossy channels.

Bio: Samuel Palermo(S'98-M'07-SM'17) received the B.S. and M.S. degrees in electrical engineering from Texas A&M University, College Station, TX in 1997 and 1999, respectively, and the Ph.D. degree in electrical engineering from Stanford University, Stanford, CA in 2007. From 1999 to 2000, he was with Texas Instruments, Dallas, TX, where he worked on the design of mixed-signal

integrated circuits for high-speed serial data communication. From 2006 to 2008, he was with Intel Corporation, Hillsboro, OR, where he worked on high-speed optical and electrical I/O architectures. In 2009, he joined the Electrical and Computer Engineering Department of Texas A&M University where he is currently an associate professor. His research interests include high-speed electrical and optical interconnect architectures, RF photonics, high performance clocking circuits, and integrated sensor systems. Dr. Palermo is a recipient of a 2013 NSF-CAREER award. He is a member of Eta Kappa Nu and IEEE. He is currently an associate editor for IEEE Solid-State Circuits Letters and has previously served as an associate editor for IEEE Transactions on Circuits and System - II from 2011 to 2015. He has also served on the IEEE CASS Board of Governors from 2011 to 2012. He is currently a distinguished lecturer for the IEEE Solid-State Circuits Society. He was a coauthor of the Jack Raper Award for Outstanding Technology-Directions Paper at the 2009 International Solid-State Circuits Conference, the Best Student Paper at the 2014 Midwest Symposium on Circuits and Systems, and the Best Student Paper at the 2016 Dallas Circuits and Systems Conference. He received the Texas A&M University Department of Electrical and Computer Engineering Outstanding Professor Award in 2014 and the Engineering Faculty Fellow Award in 2015.

CLICK HERE TO REGISTER

Two Exciting SSCS Sponsored Events at ESSCIRC/ESSDERC 2018

Diversity Luncheon at ESSCIRC/ESSDERC 2018

Sponsored by the IEEE Solid-State Circuits Society Women in Circuits

Tuesday, September 4th, 2018
12:30 PM - 2:00 PM
Room CHE/0183/U - Chemie Building

This luncheon will feature talks and interactive discussion on how to increase diversity in the ESSCIRC and ESSDERC community.

Speakers for this event are:

Andreia Cathelin (STMicroelectronics)
Sven Mattisson (Ericsson and Lund University)
Jan Van der Spiegel (University of Pennsylvania)
Alice Wang (PsiKick)

The registration fee is € 10,00 (VAT INCLUDED) to be added to ESSDERC/ESSCIRC registration fee. Register for the event by ticking "SSCS Diversity Luncheon" in the ESSDERC/ESSCIRC Registration Form.

If you already registered for ESSCIRC/ESSDERC and would like to attend the luncheon, please email **essxxrc@sistemacongressi.com**.

This event is open to everyone of all ages and genders.

Students and Young Professionals Micro-Mentoring and Career Coaching Session

Sponsored by the IEEE Solid-State Circuits Society Young Professionals

Wednesday, September 5th, 2018
5:00 PM - 6:00 PM
Room CHE/0183/U - Chemie Building

Complimentary event with light refreshments for all students, faculty, and engineers within 15 years of their first degree.

- Leading experts from industry and academia, IEEE SSCS Executives, and Distinguished Leaders will share their experiences
- 1 on 1 answers to all your questions on publications, entrepreneurship, industry vs. academia and career coaching.
- Complimentary giveaways for attendees
- Free SSCS student membership offer for event attendees

Learn about SSCS member benefits for young engineers & students, such as complimentary tutorials and short courses, webinars, distinguished lecturers to present at your region, networking with 10,000 + SSCS members around the globe, latest technical content, Student fellowships programs and more.

Introducing - SSCS Chip Chat

SSCS' educational programming has expanded to include a podcast called SSCS Chip Chat. This interview style podcast focuses on the stories of engineers and scientists behind the integrated circuits that power the world.

The podcast can be listened to by searching SSCS Chip Chat in the Apple Podcast App or whatever podcast app you use for your mobile device.

You can also listen to the podcast online. **Click here to listen!**

Episode 1: Dr. Gert Cauwenberghs
Episode 2: Albert Theuwissen
Episode 3: Shanthi Pavan
Episode 4: R. Jacob Baker

EDUCATION

September 2018 Distinguished Lectures

SSCS Singapore	On-Chip Epilepsy Detection: Where Machine Learning Meets Wearable, Patient-Specific Seizure Monitoring - by Prof. Jerald Yoo High-performance MEMS Gyroscope - By Prof. Yong Ping Xu	September 27, 2018	Fusionopolis, Franklin room @ FP1 Connexis South Tower **Click here for more information**

CONFERENCES

Upcoming Conferences

ESSCIRC/ESSDERC 2018 - 44th European Solid-State Circuits Conference/44th European Solid-State Device Research Conference Dresden, Germany	**September 3 - 6, 2018**
2018 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS) San Diego, CA	**October 14 - 17, 2018**
2018 IEEE Biomedical Circuits and Systems Conference (BioCAS) Cleveland, OH	**October 17 - 19, 2018**
2018 IEEE Asian Solid-State Circuits Conference (A-SSCC) Tainan, Taiwan	**November 5 - 7, 2018**
2019 IEEE International Solid-State Circuits Conference (ISSCC) San Francisco, CA	**February 17 - 19, 2019**

CALL FOR PAPERS

ISSCC 2019 - Call for Papers

Theme: Envisioning the Future

ISSCC 2019 is seeking innovations that will inspire the future of solid-state circuits and systems. Innovative and original papers are solicited in subject areas including (but not limited to) the following:

ANALOG: Amplifiers, comparators, oscillators, filters, references; nonlinear analog circuits; digitally-assisted analog circuits; MEMS/sensor interface circuits.

DATA CONVERTERS: Nyquist-rate and oversampling A/D and D/A converters; embedded and application-specific A/D and D/A converters; analog to information conversion; time-to-digital converters.

DIGITAL ARCHITECTURES & SYSTEMS: Microprocessors, micro-controllers, application processors, graphics processors; digital systems for communications, video and multimedia,

machine-learning, deep-learning, neuromorphism, cryptography, security and trusted computing, special-function acceleration, processing-in-memory; reconfigurable systems, near- and sub-threshold systems, digital architectures and systems for emerging applications (e.g. virtual reality - AR/VR and autonomous vehicles).

DIGITAL CIRCUITS: Building blocks for 2D/3D SoC such as intra-chip communication circuits, clock distribution techniques, soft-error and variation-tolerant circuits. Circuits for power management in digital applications: including voltage regulators, adaptive digital circuits, digital sensors; Near- and sub-threshold circuits; PLLs for digital clocking applications. Circuits for neuro-computing; Hardware security circuits including PUFs, TRNG, and attack-detection sensors.

IMAGERS, MEMS, MEDICAL, & DISPLAY: Image sensors and SoCs; automotive, LIDAR, and ultrasonic sensors; MEMS sensor systems; wearable, implantable, ingestible electronics, biomedical SoCs, neural interfaces and closed-loop systems; biosensors, microarrays, and lab-on-a-chip; display electronics, displays with sensing functionality; sensing for AR/VR.

MEMORY: Static, dynamic, and non-volatile memories for stand-alone and embedded applications; memory/SSD controllers; high-bandwidth I/O interfaces; memories based on phase-change, magnetic, spin-transfer-torque, ferroelectric, and resistive materials; array architectures and circuits to improve low-voltage operation, power reduction, reliability, and fault tolerance; memory-subsystem enhancements, including in-memory logic functions, machine learning, artificial intelligence, and AR/VR.

POWER MANAGEMENT: Power control and management circuits, regulators; switched-mode power converter ICs using inductive, capacitive, and hybrid techniques; energy-harvesting circuits and systems; wide-bandgap topologies and gate-drivers; power and signal isolators; circuits for lighting, wireless power.

RF CIRCUITS and WIRELESS SYSTEMS: Building blocks and complete solutions at RF, mm-Wave and THz frequencies for receivers, transmitters, frequency synthesizers, transceivers, SoCs, and SiPs. Innovative circuit-level and system-architecture solutions for established wireless standards and future systems or applications such as radar, sensing, and imaging.

TECHNOLOGY DIRECTIONS: Emerging IC and system solutions for: biomedical, sensor interfaces, analog signal processing, power management, computation, data storage, and communication; analog/mixed-signal techniques for security and machine learning; non-silicon-, carbon-, organic-, metal-oxide-, compound-semiconductor- and new-device-based circuits; nano, flexible, large-area, stretchable, printable, quantum, optical, and 3D-integrated electronics; spintronics.

WIRELINE: Receivers/transmitters/transceivers for wireline systems, including backplane transceivers, optical links, chip-to-chip communications, 2.5/3D interconnect, copper-cable links, and equalizing on-chip links; exploratory I/O circuits for advancing data rates, power efficiency, and equalization; wireline transceiver building blocks (such as AGCs, front ends, equalizers, clock-generation and distribution circuits including PLLs, clock-and-data recovery, line drivers, and hybrids).

INDUSTRY SHOWCASE
SSCC 2019 will host an Industry Showcase Evening Session. The goal of this event is to highlight the role of solid-state circuits and systems-on-chip (SoCs) in the creation of novel products. It will feature short presentations, as well as interactive demonstrations where attendees can have a hands-on experience with each featured innovation. The outstanding demonstration(s) will be recognized at next-year's Conference. To be considered for participation in the Industry Showcase, proposals consisting of a one-page description of the potential demonstration, including a maximum of two illustrative figures, must be uploaded to the ISSCC submission website (https://submissions.mirasmart.com/ISSCC2019). Firm deadline for electronic submission is Monday, September 10, 2018, 3:00PM Eastern Daylight Time (19:00 GMT).Only proposals with an industrial affiliation will be considered. Feedback on the proposals will be given by October 31, 2018. Refer to the ISSCC Website for further information (http://isscc.org).

The submission website will be available starting July 1, 2018.

Please **click here** for details on submission guidelines and requirements.

DEADLINES
Paper Submissions: September 10, 2018, 3:00 PM ET
Electronic Submission Proposals for Industry Showcase: September 10, 2018, 3:00 PM ET

2019 VLSI-DAT - Call for Papers

2019 International Symposium on VLSI Design, Automation, and Test

The 2019 International Symposium on VLSI Design, Automation and Test will be held on April 22-25, 2019 at the Ambassador Hotel, Hsinchu, Taiwan. Original and unpublished papers on all aspects of VLSI Design, Automation and Test are solicited, including but not limited to:

ANALOG DESIGN	DIGITAL DESIGN	EDA	TEST
RF, Analog and Mixed Signal Circuits	Digital Circuits and ASICs	Logic and Behavioral Synthesis	Test Generation and Compression
Sensor and Interface Circuits	CPU, DSP and Multicore Architectures	Physical Design and Verification	Design-for-Testability and BIST
Memory Circuits and Systems	Multimedia Processing Designs	Design for Manufacturability	RF, Analog and Mixed-Signal Test
Biomedical Circuits	Communication Designs	Power/Thermal Estimation and Optimization	Memory Test
Energy-Harvesting and Power Circuits	Hardware Security and Trust	Design Verification	SOC and System Level Test
Ultra Low-Power Circuits and Systems	Designs for Edge Computing	Modeling and Simulation	Silicon Debug and Diagnosis
Memristive and Neuromorphic Circuits	Designs for Machine Learning	Electronic System Level Design	3D IC and Interposer-Based IC Test
Security Circuits for IoT and AI	SOC and NOC Architectures	Hardware/Software Co-Design	Yield and Reliability Enhancement
	Embedded System and Software	Machine Learning for EDA	On-Chip Monitoring
	System-in-Package Designs	Analog EDA	Test Data Mining and Learning
		EDA for Microfluidic Biochips	Test Standards

The length of the submitted paper must be 2-4 pages. The submission should also include an 80-100 word abstract. VLSI-DAT adopts the Double Bind Review process. Please do not reveal your name and/or affiliation anywhere in the submitted manuscript for the first paper submission.

Deadlines:

Prospective authors must submit a self-contained paper with figures and tables electronically through the conference website by **October 19, 2018**.
Notification of acceptance - Dec 28, 2018
Final Paper Submission Deadline - Jan 31, 2019
Author Registration Deadline - Feb 28, 2019

CLICK HERE FOR MORE INFORMATION

PUBLICATIONS

Effective October 1, 2018 : Mandatory Overlength Page Charges for IEEE Journal of Solid-State Circuits

The IEEE Solid-State Circuits Society Board has decided to implement overlength page charges in order to maintain the competitive and financial health of the IEEE Journal of Solid-State Circuits. The continued success of the journal serves our technical community and keeps our flagship publications competitive within the IEEE family.

Starting October 1, 2018, the SSCS is implementing mandatory overlength page charges for the J-SSC. If a manuscript exceeds ten pages in length, overlength charges are applied beginning at the 11th page. Charges are assessed when galley proofs are prepared, which is the last step before final publication in the Journal. The page count does not include references or author biographies. However, an overlength charge will be applied if text other than references or author biographies is included on a reference/biography page. The rate for overlength submissions is $185 per page.

This policy applies only to the J-SSC, and does not apply to Solid-State Circuits Letters (L-SSC), or other SSCS publications (e.g., SSC Magazine).

The SSCS policy on page limits is strictly enforced. Payment for overlength pages - if any - must be received at the time galley proofs are approved and submitted by the author.
SSCS values its authors, members, and volunteers. This policy protects your body of work and ensures the sustainability of the J-SSC for the future.

For more information on IEEE Overlength Length Page Charges, **click here**.

The latest in SSCS Flagship Publications...

IEEE Solid-State Circuits Letters

Volume 1, Issue 4, April 2018

A Subranging-Based Nonuniform Sampling ADC With Sampling Event Filtering **Tzu-Fan Wu ; Mike Shuo-Wei Chen**
A Wide-Tuning-Range Low-Phase-Noise mm-Wave CMOS VCO With Switchable Transformer-Based Tank **Milad Haghi Kashani ; Amirahmad Tarkeshdouz ; Reza Molavi ; Ehsan Afshari ; Shahriar Mirabbasi**
A 0.083-mm225.2-to-29.5 GHz Multi-LC-Tank Class-F234VCO With a 189.6-dBc/Hz FOM **Hao Guo ; Yong Chen ; Pui-In Mak ; Rui P. Martins**
Measurement and Analysis of Input-Signal Dependent Flicker Noise Modulation in Chopper Stabilized Instrumentation Amplifier **Hyunsoo Ha ; Chris Van Hoof ; Nick Van Helleputte**
A ± 12-A High-Side Current Sensor With 25 V Input CM Range and 0.35% Gain Error From 40 °C to 85 °C **Long Xu ; Saleh Heidary Shalmany ; Johan H. Huijsing ; Kofi A. A. Makinwa**
An Accurate dB-Linear CMOS VGA Based on Double Duplicate Biasing Technique **Xiong Song ; Zheng Hao Lu ; Xiao Peng Yu**
A 91-GHz Fundamental VCO With 6.1% DC-to-RF Efficiency and 4.5 dBm Output Power in 0.13-Î¼m CMOS **Amirahmad Tarkeshdouz ; Ali Mostajeran ; Shahriar Mirabbasi ; Ehsan Afshari**

IEEE Journal of Solid-State Circuits

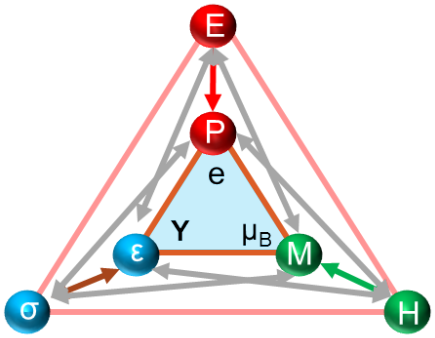
Vol. 53, Issue 8, August 2018

High-Efficiency Millimeter-Wave Single-Ended and Differential Fundamental Oscillators in CMOS Hao Wang ; Jingjun Chen ; James T. S. Do ; Hooman Rashtian ; Xiaoguang Liu
A High-Fractional-Bandwidth, Millimeter-Wave Bidirectional Image-Selection Architecture With Narrowband LO Tuning Requirements Najme Ebrahimi ; James F. Buckwalter
Analysis and Design of Ultra-Wideband mm-Wave Injection-Locked Frequency Dividers Using Transformer-Based High-Order Resonators Jingzhi Zhang ; Yixuan Cheng ; Chenxi Zhao ; Yunqiu Wu ; Kai Kang
Analysis and Design of Commutation-Based Circulator-Receivers for Integrated Full-Duplex Wireless Negar Reiskarimian ; Mahmood Baraani Dastjerdi ; Jin Zhou ; Harish Krishnaswamy
Design and Analysis of a Low Loss, Wideband Digital Step Attenuator With Minimized Amplitude and Phase Variations Ickhyun Song ; Moon-Kyu Cho ; John D. Cressler
An 80-Gb/s 44-mW Wireline PAM4 Transmitter Yikun Chang ; Abishek Manian ; Long Kong ; Behzad Razavi
A Wirelessly Powered UWB RFID Sensor Tag With Time-Domain Analog-to-Information Interface Dongxuan Bao ; Zhuo Zou ; Majid Baghaei Nejad ; Yajie Qin ; Li-Rong Zheng
Oversampling Successive Approximation Technique for MEMS Differential Capacitive Sensor Longjie Zhong ; Xinquan Lai ; Donglai Xu
An Ultra-High Input Impedance Analog Front End Using Self-Calibrated Positive Feedback Jinseok Lee ; Geon-Hwi Lee ; Hyojun Kim ; SeongHwan Cho
Toward Temperature Tracking With Unipolar Metal-Oxide Thin-Film SAR C-2C ADC on Plastic Nikolas P. Papadopoulos ; Florian De Roose ; Jan-Laurens P. J. van der Steen ; Edsger C. P. Smits ; Marc Ameys ; Wim Dehaene ; Jan Genoe ; Kris Myny
A 19.8-mW Eddy-Current Displacement Sensor Interface With Sub-Nanometer Resolution Vikram Chaturvedi ; Johan G. Vogel ; Kofi A. A. Makinwa ; Stoyan Nihtianov
A Front-End ASIC With High-Voltage Transmit Switching and Receive Digitization for 3-D Forward-Looking Intravascular Ultrasound Imaging Mingliang Tan ; Chao Chen ; Zhao Chen ; Jovana Janjic ; Verya Daeichin ; Zu-Yao Chang ; Emile Noothout ; Gijs van Soest ; Martin D. Verweij ; Nico de Jong ; Michiel A. P. Pertijs

A 22 V Compliant 56Î¼W Twin-Track Active Charge Balancing Enabling 100% Charge Compensation Even in Monophasic and 36% Amplitude Correction in Biphasic Neural Stimulators Natalie Butz ; Armin Taschwer ; Sebastian Nessler ; Yiannos Manoli ; Matthias Kuhl
A 1.08-nW/kHz 13.2-ppm/°C Self-Biased Timer Using Temperature-Insensitive Resistive Current Jaehong Jung ; Ik-Hwan Kim ; Seong-Jin Kim ; Yoonmyung Lee ; Jung-Hoon Chun
A Time-Resolved Four-Tap Lock-In Pixel CMOS Image Sensor for Real-Time Fluorescence Lifetime Imaging Microscopy Min-Woong Seo ; Yuya Shirakawa ; Yoshimasa Kawata ; Keiichiro Kagawa ; Keita Yasutomi ; Shoji Kawahito
A 65-nm CMOS Low Dropout Regulator Featuring >60-dB PSRR Over 10-MHz Frequency Range and 100-mA Load Current Range Jize Jiang ; Wei Shu ; Joseph S. Chang
An AC Input Inductor-Less LED Driver for Efficient Lighting and Visible Light Communication Yuan Gao ; Lisong Li ; Philip K. T. Mok
A 1.24uA Quiescent Current NMOS Low Dropout Regulator With Integrated Low-Power Oscillator-Driven Charge-Pump and Switched-Capacitor Pole Tracking Compensation Raveesh Magod ; Bertan Bakkaloglu ; Sanjeev Manandhar
A Fully Integrated Energy-Efficient H.265/HEVC Decoder With eDRAM for Wearable Devices Mehul Tikekar ; Vivienne Sze ; Anantha P. Chandrakasan
A 2.267-Gb/s, 93.7-pJ/bit Non-Binary LDPC Decoder With Logarithmic Quantization and Dual-Decoding Algorithm Scheme for Storage Applications Yuta Toriyama ; Dejan Marković
Low-Power Noise-Immune Nanoscale Circuit Design Using Coding-Based Partial MRF Method Yan Li ; Yufeng Li ; I-Chyn Wey ; Jianhao Hu ; Fan Yang ; Xuan Zeng ; Xiaoxue Jiang ; Jie Chen
Reducing Power Side-Channel Information Leakage of AES Engines Using Fully Integrated Inductive Voltage Regulator Monodeep Kar ; Arvind Singh ; Sanu K. Mathew ; Anand Rajan ; Vivek De ; Saibal Mukhopadhyay
A Double Sensing Scheme With Selective Bitline Voltage Regulation for Ultralow-Voltage Timing Speculative SRAM Jun Yang ; Hao Ji ; Yichen Guo ; Jizhe Zhu ; Yuan Zhuang ; Zhi Li ; Xinning Liu ; Longxing Shi
Low-Area TCAM Using A Donâ€™t Care Reduction Scheme Ki-Chan Woo ; Byung-Do Yang

IEEE Journal on Exploratory Solid-State Computational Devices and Circuits

Volume 4



Towards a Strong Spin-Orbit Coupling Magnetoelectric Transistor **Peter A. Dowben ; Christian Binek ; Kai Zhang ; Lu Wang ; Wai-Ning Mei ; Jonathan P. Bird ; Uttam Singisetti ; Xia Hong ; Kang L. Wang ; Dmitri Nikonov**
Using Programmable Graphene Channels as Weights in Spin-Diffusive Neuromorphic Computing **Jiaxi Hu ; Gordon Stecklein ; Yoska Anugrah ; Paul A. Crowell ; Steven J. Koester**
BCB Evaluation of High-Performance and Low-Leakage Three-Independent-Gate Field Effect Transistors **Jorge Romero-Gonzalez ; Pierre-Emmanuel Gaillardon**
Tunnel FET Analog Benchmarking and Circuit Design **Hao Lu ; Paolo Paletti ; Wenjun Li ; Patrick Fay ; Trond Ytterdal ; Alan Seabaugh**
Improving Energy Efficiency of Low Voltage Logic by Technology-Driven Design **Kaushik Vaidyanathan ; Daniel H. Morris ; Uygar E. Avci ; Huichu Liu ; Tanay Karnik ; Hong Wang ; Ian A. Young**
Inversion Charge Boost and Transient Steep-Slope Induced by Free-Charge-Polarization Mismatch in a Ferroelectric-Metal-Oxide-Semiconductor Capacitor **Sou-Chi Chang ; Uygar E. Avci ; Dmitri E. Nikonov ; Ian A. Young**

JxCDC papers listed in order of popularity can be found online HERE.

For paper submission details, click HERE.

Seeking News

Please send any chapter news or happenings (Distinguished Lecturer visits, events hosted by your SSCS chapter, awards received by members, etc) to Abira Sengupta, SSCS Magazine News Editor, for inclusion in an upcoming issue of the magazine. Please email - **Abira.Sengupta@ieee.org**. We look forward to receiving your news articles!

For more chapter news, check out the Summer 2018 issue of the Solid-State Circuits Magazine.

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