August 2017

NEWS

Upcoming Webinar

Auto-adaptive digital-circuits - Application to low-power Multicores and ultra-low power Wireless Sensor Nodes

Presented by Edith Beigne

Thursday, September 14 @ 12 PM (ET)

*Professional Development Hours can be requested for this webinar*

CLICK HERE TO REGISTER!

This webinar was prerecorded. Edith Beigne will be available during the presentation to answer questions regarding content, formulas, or theories. Please follow the link to register for the webinar which is free and open to all SSCS members.
Abstract: Today's sources of variations are affecting a lot circuits' energy efficiency: this talk will bring innovative technological, circuit and architectural techniques for efficient automatic performance regulation. Given the numerous sources of variations encountered by today's integrated systems, it becomes very challenging to implement highly energy efficient circuits. Whether the variations are in the process, in the application needs or in the environmental characteristics, the common solution is adaptation. This talk is exploring automatic adaptation techniques at architectural, circuit and technological levels applied to MPSoCs as well as autonomous Wireless Sensor Nodes.

Bio: Edith Beigné joined CEA-LETI, Grenoble, France, in 1998. Since 2017, she is the scientific director of the circuit design division. Since 2009, she is a senior scientist in the digital and mixed-signal design lab where she researches low power and adaptive circuit techniques, exploiting asynchronous design and advanced technology nodes like FDSOI 28nm and 14nm for many different applications from high performance MPSoC to ultra-low power IoT applications. She is part of ISSCC TPC since 2014 and part of VLSI's symposium since 2015. She is a distinguished Lecturer for SSCS for 2016 and 2017.

SSCS Young Professionals & Students Mentoring & Career Coaching Event

The mentoring event will be held in conjunction with ESSCIRC 2017 in Leuven, Belgium on Wednesday, September 13th at 15:45 (after the sessions and before the gala dinner) in the Agora Building (ground level) in the Flexispace 00.D01 Room.

Click here to RSVP, walk-in's are welcome.

Upcoming ESSCIRC/ESSDERC Women in Circuits Luncheon

DATE: Tuesday, September 12th
TIME: 12 - 1:30 PM
LOCATION: ESSCIRC/ESSDERC Venue, Agora Learning Center, Leuven, Belgium
COST: € 10,00 (VAT included)

The luncheon registration fee can be added to ESSDERC/ESSCIRC registration fee. Register for the event by ticking "IEEE Women in Circuits Luncheon" on
If you've already registered and would like to add the luncheon to your registration, please write an email to registration@sistemacongressi.com.

This luncheon is an opportunity to hear from an accomplished female leader in the field, Francoise Chombar (CEO, Melexis, Belgium) and to get to know fellow women in the profession and discuss a range of topics including leadership, work-life balance, and professional development. Both men and women eager to discuss and stimulate female presence in the field are more than welcome to attend.

For more information, please click here!

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Do you Qualify for IEEE Senior Member Grade?

Senior Member is the highest grade for which IEEE members can apply. IEEE members can self-nominate or be nominated for Senior Member grade.

Benefits include professional recognition, a senior member plaque, leadership eligibility to hold executive IEEE volunteer positions, and more.

For more information on IEEE Senior Member Grade, please click here. If you have any questions or concerns, or need assistance obtaining references, email sscs-membership@ieee.org.

The next Senior Member review panel is in October. Become a Senior Member now!

BEGIN SENIOR MEMBER APPLICATION

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The IEEE Design & Test Magazine is Now Available in Digital Version for Subscribers!

The IEEE Design & Test Magazine is now available in digital version for subscribers at no extra cost.

For fast browsing, subscribers also have access to the PDF version of the entire issue. The magazine is available through IEEE Xplore and the print version.

Not a subscriber? The complete electronic, digital, and print subscription is $54 USD a year for IEEE members of select societies (including the Solid-State Circuits Society).

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New offering for SSCS members
In an effort to increase member benefits, SSCS has created the SSCS Resource Center. This informational hub will house technical information such as past webinar videos and slides, ISSCC tutorials and short courses, and more.

**Top 5 Downloaded Products on the SSCS Resource Center:**

1. **ISSCC 2015 Tutorial: High Speed Current Steering DACs**, Presented by Jan Mulder
2. **Webinar: Trends in Broadband Converters**, Presented by David H. Robertson
3. **ISSCC 2006 Short Course: Pipelined A/D Converters**, Presented by Bang-Sup Song
5. **Webinar: The X Files, Sheerluck Ohms and the 33dB Solution**, Presented by Paul Brokaw

[Click here to visit the SSCS Resource Center.](#)

**Earn Continuing Education Hours**

Have you attended an SSCS webinar? Attendees of upcoming and past webinars have the opportunity to earn professional development hours. Certificates of completion are offered to participants who view a webinar. A certificate of completion confirms one hour of professional development. After you attend the webinar, you may request a certificate of completion by completing the form [HERE](#).

**EDUCATION**

**Upcoming Distinguished Lecturer Events in September**

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<td>September 23</td>
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AWARDS

2018 IEEE Donald O. Pederson Award in Solid-State Circuits

The recipients of the 2018 IEEE Donald O. Pederson Award are William S. Carter, Fellow, Xilinx, San Jose, California and Stephen M. Trimberger, Fellow, Xilinx, San Jose, California for "Contributions to field-programmable gate array technology". The award will be presented at the Plenary Session at the 2018 International Solid-State Circuits Conference (ISSCC) in San Francisco, California.

CONFERENCES

Upcoming Conferences

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<td>2017 European Solid-State Circuits Conference (ESSCIRC)</td>
<td>Sept 11 - 14, 2017</td>
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<td>Belgium</td>
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<tr>
<td>2017 IEEE Biomedical Circuits and Systems Conference (BioCAS)</td>
<td>October 19 - 21, 2017</td>
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<td>Italy</td>
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<tr>
<td>2017 IEEE Bipolar/BiCMOS Circuits and Technology Meeting - BCTM</td>
<td>October 19 - 21, 2017</td>
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<td>Florida</td>
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<td>Korea (South)</td>
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<tr>
<td>2018 International Solid-State Circuits Conference (ISSCC)</td>
<td>February 11 - 15, 2018</td>
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<td>San Francisco, CA</td>
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CALL FOR PAPERS

2018 IEEE International Solid-State Circuits Conference (ISSCC) - Call for Papers

Continued advances in solid-state circuits and systems have brought evermore powerful communication and computation capabilities into mobile form factors. These ubiquitous smart devices lie at the heart of a revolution shaping how we connect, collaborate, build relationships, and share information. Such social technology allows people to maintain connections and support networks that otherwise would not be possible; it provides the ability to access information instantaneously and from any location, helping to shape the world’s events and culture. Thereby, citizens of all nations are more empowered than ever before, and social networks allow worldwide communities to develop and bond through common interests. ISSCC 2018 is seeking innovations that will bring further progress in developing a truly-connected social world.

Innovative and original papers are solicited in subject areas including (but not limited to) the following:
ANALOG: Amplifiers, comparators, oscillators, filters, references; nonlinear analog circuits; digitally-assisted analog circuits; sensor interface circuits.

DATA CONVERTERS: Nyquist-rate and oversampling A/D and D/A converters.

DIGITAL ARCHITECTURES & SYSTEMS: Microprocessors, micro-controllers, applications processors, graphics processors; systems for communications, video and multimedia, machine-learning, deep-learning, neuromorphism, cryptographics, special function acceleration, processing-in-memory, FPGA/reconfigurable systems, system-level power management, near-threshold/subthreshold systems, digital architectures and systems for emerging applications (e.g. virtual reality, autonomous vehicles).

DIGITAL CIRCUITS: Building blocks for 2D/3D SoC, including: special-purpose digital circuits, intra-chip communication circuits, clock-distribution techniques, soft-error and variation-tolerant circuits; Circuits for power management in digital applications, including, digital/synthesizable voltage regulators and PLLs, digital sensors, adaptive circuits; Subthreshold and Near-threshold circuits; Circuits for neuro-computing; Hardware-security circuits including PUFs, TRNGs, crypto-circuits, side-channel-attacks mitigation.

IMAGERS, MEMS, MEDICAL, & DISPLAY: Image sensors and companion chips; image-sensor SoCs; MEMS-based integrated systems; ultrasonic sensors, neural interfaces and closed-loop systems; biosensors, microarrays, and lab-on-a-chip; wearable electronics; biomedical SoCs; display and touch electronics, flexible displays, and displays with integrated sensing functionality.

MEMORY: Static, dynamic, and non-volatile memories for stand-alone and embedded applications; memory/SSD controllers; high-bandwidth I/O interfaces; memories based on phase-change, magnetic, spin-transfer-torque, ferroelectric, and resistive materials; array architectures and circuits to improve low-voltage operation, power reduction, bit-error management, reliability, and fault tolerance; memory-subsystem enhancements, including in-memory logic functions.

POWER MANAGEMENT: Power control and management circuits, regulators; switched-mode power supplies, using inductive, capacitive, and hybrid techniques; energy harvesting circuits and systems; circuits for lighting.

RF CIRCUITS and WIRELESS SYSTEMS: Building blocks and complete solutions at RF, mm-Wave and THz frequencies for receivers, transmitters, frequency synthesizers, transceivers, SoCs and SiPs; Innovative circuit-level and system architecture solutions for established wireless standards and future systems or applications, including wireless sensing, radar and localization.

TECHNOLOGY DIRECTIONS: Emerging IC and system solutions for: biomedical applications, sensor interfaces, analog signal processing, power management, computation, data storage, security, and communication; non-silicon, carbon, organic, metal-oxide-, compound, wide-bandgap-semiconductor, and nano electronics circuits; flexible, large-area, stretchable, and printable electronics; 3D integration; spintronics; quantum, optical, new-device, and non-transistor-based circuits.

WIRELINE: Receivers/transmitters/transceivers for wireline systems, including backplane transceivers, optical links, chip-to-chip communications, 2.5/3D interconnect, copper cable links, and equalizing on-chip links; exploratory I/O circuits for advancing data rates, power efficiency, and equalization; building blocks for wireline transceivers (such as AGCs, analog and ADC/DAC-based front ends, equalizers, clock generation and distribution circuits including PLLs, line drivers, and hybrids).

NEW FIRM DEADLINE FOR REGISTERING INTENT TO SUBMIT: Thursday, September 7, 2017, 3:00 PM ET

FIRM DEADLINE FOR PAPER SUBMISSION: Monday, September 11, 2017, 3:00 PM ET

Authors should submit 2 items for review: 1) An informative and quantitative Abstract; 2) A Draft Manuscript for the Digest of Technical Papers. Also, read the Pre-Publication Guidelines (summarized below) carefully!

The submission Website is now available.
To submit a paper, go to: [http://submissions.mirasmart.com/ISSCC2018](http://submissions.mirasmart.com/ISSCC2018) to upload the manuscript and provide the requested additional information. Authors must register their intent to submit on the website by September 7, 2017, this will require upload of an abstract and completion of a submission questionnaire. The full manuscript must be submitted by September 11, 2017. During the submission process you will be asked for a suggested subject area, however this subject area may be changed by the ISSCC organization to streamline the review process.

A sample abstract and draft Digest paper can be found at the ISSCC Website (single-column double-spaced format is required for the paper-review process).

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**RFIC 2018: IEEE Radio Frequency Integrated Circuits Symposium - Call for Papers**


The conference is soliciting papers describing original work in RFIC circuits, systems engineering, design methodology, RF modeling and CAD simulation, RFIC technologies, devices, fabrication, testing, reliability, packaging and modules to support RF applications in areas such as, but not limited to:

- **Wireless Cellular and Connectivity**: 2G/3G/4G/5G (sub-6GHz), LTE, WWAN, WLAN, BT, GPS, FM, UWB
- **Low Power Transceivers**: RFID, NFC, Zigbee, 802.15.4, WPAN, WBAN, Biomedical, Sensor Nodes, IR-UWB, Wake-up Receivers
- **Receiver Sub-Systems and Circuits**: LNAs, Mixers, VGAs, phase shifters, switches, Integrated FEM, amplifiers, filters, demodulators
- **Mixed-Signal RF and Data Converters**: RF and baseband converters (ADC/DAC), Sub-sampling/Over-sampling Circuits
- **Reconfigurable and Tunable Front-Ends**: SDR/Cognitive Radio, Wideband/Multi-band Front-Ends, Interference Cancellation, Full-Duplex, Adaptive Front-Ends
- **Transmitter Sub-Systems and Power Amplifiers**: Power Amplifiers, Drivers, modulators, digital transmitters, Advanced TX circuits, linearization and efficiency enhancement techniques
- **Oscillators**: VCOs, injection-locking frequency dividers/multipliers
- **Frequency Synthesis**: PLLs, DLLs, MDLLs, DDS, LO drivers, frequency dividers
- **Millimeter-and SubMillimeter Wave Systems**: >20GHz SoCs/SiPs for wireless communication (5G mm-Wave, WiGig, 802.11ay), phased-arrays, imaging, radar, remote sensing
- **High-Speed Data Transceivers**: Wireline, Optical Transceivers, and CDRs for High-Speed Data links

*NEW THIS YEAR* - A double-blind review process will be used to ensure anonymity for both authors and reviewers.

**Electronic Submission Deadlines** - Technical Paper Summaries in PDF Format are due 12 January 2018, Final Manuscripts for the Digest and USB are due 22 March 2018.

Submissions must be made at [rfic-ieee.org](http://rfic-ieee.org).

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**PUBLICATIONS**

**IEEE Author Center**
The IEEE Author Center is now live. The **IEEE Author Center** is a standalone site for journal authors that provides a one-stop shop to learn about publishing with IEEE. This comprehensive source of up-to-date content is written from the author's perspective in simple, engaging language and is easily viewed on mobile. The content is organized to follow the author's path through the publishing process, from writing the article through to post-publication.

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**The latest in SSCS Flagship Publications...**

![IEEE Journal of Solid-State Circuits](image)

**IEEE Journal of Solid-State Circuits**  
**Vol. 52, Issue 9, September 2017**

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### IEEE Journal on Exploratory Solid-State Computational Devices and Circuits

**Mid-Year Highlights**

In the first half of 2017, the Journal on Exploratory Solid-State Computational Devices and Circuits had top five of the papers published which already appear in the top 8 of the journal’s most accessed papers. These papers include:

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<td>Nonboolean Pattern Recognition Using Chains of Coupled CMOS Oscillators as Discriminant Circuits</td>
<td>Vahnood Pourahmad ; Sasikanth Manipatruni ; Dmitri Nikonov ; Ian Young ; Ehsan Afshari</td>
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<td>Compact Modeling of Distributed Effects in 2-D Vertical Tunnel FETs and Their Impact on DC and RF Performances</td>
<td>Jie Min ; Peter M. Asbeck</td>
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<td>Nonvolatile Spintronic Memory Array Performance Benchmarking Based on Three-Terminal Memory Cell</td>
<td>Chenyun Pan ; Azad Naeemi</td>
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<td>CoMET: Composite-Input Magnetoelectric- Based Logic Technology</td>
<td>Meghna G. Mankalale ; Zhaoxin Liang ; Zhengyang Zhao ; Chris H. Kim ; Jian-Ping Wang ; Sachin S. Sapatnekar</td>
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<td>Electrical-Spin Transduction for CMOS-Spintronic Interface and Long-Range Interconnects</td>
<td>Rouollah Mousavi Iraei ; Sasikanth Manipatruni ; Dmitri E. Nikonov ; Ian A. Young ; Azad Naeemi</td>
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JxCDC papers listed in order of popularity can be found online HERE.

For paper submission details, click HERE.

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**Seeking News**

Please send any chapter news or happenings (Distinguished Lecturer visits, events hosted by your SSCS chapter, awards received by members, etc) to Abira Sengupta, SSCS Magazine News Editor, for inclusion in an upcoming issue of the magazine. Please email - Abira.Sengupta@ieee.org. We look forward to receiving your news articles!

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**For more chapter news, check out the Summer 2017 issue of the Solid-State Circuits Magazine.**

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**FEEDBACK**

Let us know what you think! Please email us to send us your comments about the newsletter, what you would like to see included each month, or any other comments.

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