



**IEEE SOLID-STATE
CIRCUITS SOCIETY**
Where ICs are in IEEE

August 2017

NEWS



Upcoming Webinar

**Auto-adaptive digital-
circuits - Application to
low-power Multicores and
ultra-low power Wireless
Sensor Nodes**

Presented by Edith Beigne

**Thursday, September 14 @ 12 PM
(ET)**

Professional Development Hours can be requested for this webinar

[CLICK HERE TO REGISTER!](#)

This webinar was prerecorded. Edith Beigne will be available during the presentation to answer questions regarding content, formulas, or theories. Please follow the link to register for the webinar which is free and open to all SSCS members.

Abstract: Today's sources of variations are affecting a lot circuits' energy efficiency: this talk will bring innovative technological, circuit and architectural techniques for efficient automatic performance regulation. Given the numerous sources of variations encountered by today's integrated systems, it becomes very challenging to implement highly energy efficient circuits. Whether the variations are in the process, in the application needs or in the environmental characteristics, the common solution is adaptation. This talk is exploring automatic adaptation techniques at architectural, circuit and technological levels applied to MPSoCs as well as autonomous Wireless Sensor Nodes.

Bio: Edith Beigné joined CEA-LETI, Grenoble, France, in 1998. Since 2017, she is the scientific director of the circuit design division. Since 2009, she is a senior scientist in the digital and mixed-signal design lab where she researches low power and adaptive circuit techniques, exploiting asynchronous design and advanced technology nodes like FDSOI 28nm and 14nm for many different applications from high performance MPSoC to ultra-low power IoT applications. She is part of ISSCC TPC since 2014 and part of VLSI'symposium since 2015. She is a distinguished Lecturer for SSCS for 2016 and 2017.



SSCS Young Professionals & Students Mentoring & Career Coaching Event

The mentoring event will be held in conjunction with [ESSCIRC 2017](#) in Leuven, Belgium on Wednesday, September 13th at 15:45 (after the sessions and before the gala dinner) in the Agora Building (ground level) in the Flexispace 00.D01 Room.

[Click here to RSVP](#), walk-in's are welcome.

Upcoming ESSCIRC/ESSDERC Women in Circuits Luncheon

DATE: Tuesday, September 12th
TIME: 12 - 1:30 PM
LOCATION: ESSCIRC/ESSDERC Venue, Agora Learning Center, Leuven, Belgium
COST: € 10,00 (VAT included)



The luncheon registration fee can be added to ESSDERC/ESSCIRC registration fee. Register for the event by ticking "IEEE Women in Circuits Luncheon" on

the [ESSDERC/ESSCIRC Registration Form](#).

If you've already registered and would like to add the luncheon to your registration, please write an email to registration@sistemacongressi.com.

This luncheon is an opportunity to hear from an accomplished female leader in the field, Francoise Chombar (CEO, Melexis, Belgium) and to get to know fellow women in the profession and discuss a range of topics including leadership, work-life balance, and professional development. Both men and women eager to discuss and stimulate female presence in the field are more than welcome to attend.

[For more information, please click here!](#)

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New offering for SSCS members



In an effort to increase member benefits, SSCS has created the SSCS Resource Center. This informational hub will house technical information such as past webinar videos and slides, ISSCC tutorials and short courses, and more.

[Top 5 Downloaded Products on the SSCS Resource Center:](#)

- 1). [ISSCC 2015 Tutorial: High Speed Current Steering DACs](#), Presented by Jan Mulder
- 2). [Webinar: Trends in Broadband Converters](#), Presented by David H. Robertson
- 3). [ISSCC 2006 Short Course: Pipelined A/D Converters](#), Presented by Bang-Sup Song
- 4). [Webinar: Enabling and Exploiting Machine Learning in Ultra-low-power Devices](#), Presented by Naveen Verma
- 5). [Webinar: The X Files, Sheerluck Ohms and the 33dB Solution](#), Presented by Paul Brokaw

[Click here to visit the SSCS Resource Center.](#)

Earn Continuing Education Hours

Have you attended an SSCS webinar? Attendees of upcoming and past webinars have the opportunity to earn professional development hours. Certificates of completion are offered to participants who view a webinar. A certificate of completion confirms one hour of professional development. After you attend the webinar, you may request a certificate of completion by completing the form [HERE](#).

EDUCATION

Upcoming Distinguished Lecturer Events in September

	SPEAKER	CHAPTER	TOPIC
September 23	Vivek De	SSCS/EDS/CAS Ottawa	Topic: Fine-Grain Power Management in Many-Core System-On-Chip (SoC) For more information, please click here

AWARDS

2018 IEEE Donald O. Pederson Award in Solid-State Circuits

The recipients of the 2018 IEEE Donald O. Pederson Award are William S. Carter, Fellow, Xilinx, San Jose, California and Stephen M. Trimberger, Fellow, Xilinx, San Jose, California for "Contributions to field-programmable gate array technology". The award will be presented at the Plenary Session at the 2018 International Solid-State Circuits Conference (ISSCC) in San Francisco, California.

CONFERENCES

Upcoming Conferences

2017 European Solid-State Circuits Conference (ESSCIRC) Belgium	Sept 11 - 14, 2017
2017 IEEE Biomedical Circuits and Systems Conference (BioCAS) Italy	October 19 - 21, 2017
2017 IEEE Bipolar/BiCMOS Circuits and Technology Meeting - BCTM Florida	October 19 - 21, 2017
2017 IEEE Asian Solid-State Circuits Conference (A-SSCC) Korea (South)	November 6 - 8, 2017
2018 International Solid-State Circuits Conference (ISSCC) San Francisco, CA	February 11 - 15, 2018

CALL FOR PAPERS

2018 IEEE International Solid-State Circuits Conference (ISSCC) - Call for Papers

Continued advances in solid-state circuits and systems have brought evermore powerful communication and computation capabilities into mobile form factors. These ubiquitous smart devices lie at the heart of a revolution shaping how we connect, collaborate, build relationships, and share information. Such social technology allows people to maintain connections and support networks that otherwise would not be possible; it provides the ability to access information instantaneously and from any location, helping to shape the world's events and culture. Thereby, citizens of all nations are more empowered than ever before, and social networks allow worldwide communities to develop and bond through common interests. ISSCC 2018 is seeking innovations that will bring further progress in developing a truly-connected social world.

Innovative and original papers are solicited in subject areas including (but not limited to) the following:

ANALOG: Amplifiers, comparators, oscillators, filters, references; nonlinear analog circuits; digitally-assisted analog circuits; sensor interface circuits.

DATA CONVERTERS: Nyquist-rate and oversampling A/D and D/A converters.

DIGITAL ARCHITECTURES & SYSTEMS: Microprocessors, micro-controllers, applications processors, graphics processors; systems for communications, video and multimedia, machine-learning, deep-learning, neuromorphism, cryptographics, special function acceleration, processing-in-memory, FPGA/reconfigurable systems, system-level power management, near-threshold/subthreshold systems, digital architectures and systems for emerging applications (e.g. virtual reality, autonomous vehicles).

DIGITAL CIRCUITS: Building blocks for 2D/3D SoC, including: special-purpose digital circuits, intra-chip communication circuits, clock-distribution techniques, soft-error and variation-tolerant circuits; Circuits for power management in digital applications, including, digital/synthesizable voltage regulators and PLLs, digital sensors, adaptive circuits; Subthreshold and Near-threshold circuits; Circuits for neuro-computing; Hardware-security circuits including PUFs, TRNGs, crypto-circuits, side-channel-attacks mitigation.

IMAGERS, MEMS, MEDICAL, & DISPLAY: Image sensors and companion chips; image-sensor SoCs; MEMS-based integrated systems; ultrasonic sensors, neural interfaces and closed-loop systems; biosensors, microarrays, and lab-on-a-chip; wearable electronics; biomedical SoCs; display and touch electronics, flexible displays, and displays with integrated sensing functionality.

MEMORY: Static, dynamic, and non-volatile memories for stand-alone and embedded applications; memory/SSD controllers; high-bandwidth I/O interfaces; memories based on phase-change, magnetic, spin-transfer-torque, ferroelectric, and resistive materials; array architectures and circuits to improve low-voltage operation, power reduction, bit-error management, reliability, and fault tolerance; memory-subsystem enhancements, including in-memory logic functions.

POWER MANAGEMENT: Power control and management circuits, regulators; switched-mode power supplies, using inductive, capacitive, and hybrid techniques; energy harvesting circuits and systems; circuits for lighting.

RF CIRCUITS and WIRELESS SYSTEMS: Building blocks and complete solutions at RF, mm-Wave and THz frequencies for receivers, transmitters, frequency synthesizers, transceivers, SoCs and SiPs; Innovative circuit-level and system architecture solutions for established wireless standards and future systems or applications, including wireless sensing, radar and localization.

TECHNOLOGY DIRECTIONS: Emerging IC and system solutions for: biomedical applications, sensor interfaces, analog signal processing, power management, computation, data storage, security, and communication; non-silicon, carbon, organic, metal-oxide-, compound, wide-bandgap-semiconductor. and nano electronics circuits; flexible, large-area, stretchable, and printable electronics; 3D integration; spintronics; quantum, optical, new-device, and non-transistor-based circuits.

WIRELINER: Receivers/transmitters/transceivers for wireline systems, including backplane transceivers, optical links, chip-to-chip communications, 2.5/3D interconnect, copper cable links, and equalizing on-chip links; exploratory I/O circuits for advancing data rates, power efficiency, and equalization; building blocks for wireline transceivers (such as AGCs, analog and ADC/DAC-based front ends, equalizers, clock generation and distribution circuits including PLLs, line drivers, and hybrids).

NEW FIRM DEADLINE FOR REGISTERING INTENT TO SUBMIT: Thursday, September 7, 2017, 3:00 PM ET

FIRM DEADLINE FOR PAPER SUBMISSION: Monday, September 11, 2017, 3:00 PM ET

Authors should submit 2 items for review: 1) An informative and quantitative Abstract; 2) A Draft Manuscript for the Digest of Technical Papers. Also, read the Pre-Publication Guidelines (summarized below) carefully!

The submission Website is now available.

To submit a paper, go to: <http://submissions.miramart.com/ISSCC2018> to upload the manuscript and provide the requested additional information. Authors must register their intent to submit on the website by September 7, 2017, this will require upload of an abstract and completion of a submission questionnaire. The full manuscript must be submitted by September 11, 2017. During the submission process you will be asked for a suggested subject area, however this subject area may be changed by the ISSCC organization to streamline the review process.

A sample abstract and draft Digest paper can be found at the ISSCC Website (single-column double-spaced format is required for the paper-review process).

RFIC 2018: IEEE Radio Frequency Integrated Circuits Symposium - Call for Papers

The 2018 IEEE Radio Frequency Integrated Circuits Symposium (RFIC 2018) will be held in Philadelphia, PA, USA on June 10-12, 2018. For latest information, please visit rfic-ieee.org.

The conference is soliciting papers describing original work in RFIC circuits, systems engineering, design methodology, RF modeling and CAD simulation, RFIC technologies, devices, fabrication, testing, reliability, packaging and modules to support RF applications in areas such as, but not limited to:

- **Wireless Cellular and Connectivity:** 2G/3G/4G/5G (sub-6GHz), LTE, WWAN, WLAN, BT, GPS, FM,UWB
- **Low Power Transceivers:** RFID, NFC, Zigbee, 802.15.4, WPAN, WBAN, Biomedical, Sensor Nodes, IR-UWB, Wake-up Receivers
- **Receiver Sub-Systems and Circuits:** LNAs, Mixers, VGAs, phase shifters, switches, Integrated FEM, amplifiers, filters, demodulators
- **Mixed-Signal RF and Data Converters:** RF and baseband converters(ADC/DAC), Sub-sampling/Over-sampling Circuits
- **Reconfigurable and Tunable Front-Ends:** SDR/Cognitive Radio,Wideband/Multi-band Front-Ends, Interference Cancellation, Full-Duplex, Adaptive Front-Ends
- **Transmitter Sub-Systems and Power Amplifiers:** Power Amplifiers, Drivers, modulators, digital transmitters, Advanced TX circuits, linearization and efficiency enhancement techniques
- **Oscillators:** VCOs, injection-locking frequency dividers/multipliers
- **Frequency Synthesis:** PLLs, DLLs, MDLLS, DDS, LO drivers, frequency dividers
- **Device Technologies, Packaging, Modeling, and Testing:** CMOS, SOI, FinFet, SiGe, GaAs, GaN, MEMS, Integrated Passives, Photonic, Emerging Devices, Reliability, Packaging, Modeling and Testing, EM Modeling/Co-Simulation, Built-in-Self-Test (BIST)
- **Millimeter-and SubMillimeter Wave Systems:** >20GHzSoCs/SiPs for wireless communication (5Gmm-Wave, WiGig, 802.11ay), phased-arrays, imaging, radar, remote sensing
- **High-Speed Data Transceivers:** Wireline, Optical Transceivers, and CDRs for High-Speed Data links

NEW THIS YEAR - A double-blind review process will be used to ensure anonymity for both authors and reviewers.

Electronic Submission Deadlines- Technical Paper Summaries in PDF Format are due 12 January 2018, Final Manuscripts for the Digest and USB are due 22 March 2018.

Submissions must be made at rfic-ieee.org.

PUBLICATIONS

IEEE Author Center

The IEEE Author Center is now live. The [IEEE Author Center](#) is a standalone site for journal authors that provides a one-stop shop to learn about publishing with IEEE. This comprehensive source of up-to-date content is written from the author's perspective in simple, engaging language and is easily viewed in mobile. The content is organized to follow the author's path through the publishing process, from writing the article through to post-publication.

The latest in SSCS Flagship Publications...



IEEE Journal of Solid-State Circuits

Vol. 52, Issue 9, September 2017

A 76- to 81-GHz Multi-Channel Radar Transceiver Takeji Fujibayashi ; Yohsuke Takeda ; Weihu Wang ; Yi-Shin Yeh ; Willem Stapelbroek ; Seiji Takeuchi ; Brian Floyd
Multi-Purpose Fully Differential 61- and 122-GHz Radar Transceivers for Scalable MIMO Sensor Platforms Herman Jalli Ng ; Maciej Kucharski ; Wael Ahmad ; Dietmar Kissinger
A Total-Power Radiometer Front End in a 0.25-μm BiCMOS Technology With Low 1/f -Corner Satoshi Malotaux ; Masoud Babaie ; Marco Spirito
An Ultra-Low-Power Dual-Polarization Transceiver Front-End for 94-GHz Phased Arrays in 130-nm InP HBT Seong-Kyun Kim ; Robert Maurer ; Arda Simsek ; Miguel Urteaga ; Mark J. W. Rodwell
W -Band Direct-Modulation >20-Gb/s Transmit and Receive Building Blocks in 32-nm SOI CMOS Hasan Al-Rubaye ; Gabriel M. Rebeiz
A SAW-Less 2.4-GHz Receiver Front-End With 2.4-mA Battery Current for SoC Coexistence Matteo Ramella ; Ivan Fabiano ; Danilo Manstretta ; Rinaldo Castello
A 5GHz Digital Fractional- N PLL Using a 1-bit Delta-Sigma Frequency-to-Digital Converter in 65 nm CMOS Mrunmay Talegaonkar ; Tejasvi Anand ; Ahmed Elkholly ; Amr Elshazly ; Romesh Kumar Nandwana ; Saurabh Saxena ; Brian Young ; Woo-Seok Choi ; Pavan Kumar Hanumolu
A High-Speed Efficient 220-GHz Spatial-Orthogonal ASK Transmitter in 130-nm SiGe BiCMOS Chen Jiang ; Andreia Cathelin ; Ehsan Afshari
A Flash-Based Non-Uniform Sampling ADC With Hybrid Quantization Enabling Digital Anti-Aliasing Filter Tzu-Fan Wu ; Cheng-Ru Ho ; Mike Shuo-Wei Chen
Analysis and Design of Continuous-Time Delta-Sigma Converters Incorporating Chopping Sujith Billa ; Amrith Sukumaran ; Shanthi Pavan
A 950 nW Analog-Based Data Reduction Chip for Wearable EEG Systems in Epilepsy Saam Iranmanesh ; Esther Rodriguez-Villegas
A Fully Integrated Battery-Powered System-on-Chip in 40-nm CMOS for Closed-Loop Control of Insect-Scale Pico-Aerial Vehicle Xuan Zhang ; Mario Lok ; Tao Tong ; Sae Kyu Lee ; Brandon Reagen ; Simon Chaput ; Pierre-Ernie J. Duhamel ; Robert J. Wood ; David Brooks ; Gu-Yeon Wei
Fully Integrated Fluorescence Biosensors On-Chip Employing Multi-Functional Nanoplasmonic Optical Structures in CMOS Lingyu Hong ; Hao Li ; Haw Yang ; Kaushik Sengupta
A 40-Gb/s 14-mW CMOS Wireline Receiver

Abishek Manian ; Behzad Razavi

[A 50 Gb/s 190 mW Asymmetric 3-Tap FFE VCSEL Driver](#)

Guido Belfiore ; Mahdi Khafaji ; Ronny Henker ; Frank Ellinger

[A Reconfigurable 16/32 Gb/s Dual-Mode NRZ/PAM4 SerDes in 65-nm CMOS](#)

Ashkan Roshan-Zamir ; Osama Elhadidy ; Hae-Woong Yang ; Samuel Palermo

[A 2.6 \$\hat{P}\$ /W -1.2 mW Autonomous Electromagnetic Vibration Energy Harvester Interface IC with Conduction-Angle-Controlled MPPT and up to 95% Efficiency](#)

Joachim Leicht ; Yiannos Manoli

[A Nanosecond-Transient Fine-Grained Digital LDO With Multi-Step Switching Scheme and Asynchronous Adaptive Pipeline Control](#)

Fan Yang ; Philip K. T. Mok

[Near- and Sub- Vt Pipelines Based on Wide-Pulsed-Latch Design Techniques](#)

Wei Jin ; Seongjong Kim ; Weifeng He ; Zhigang Mao ; Mingoo Seok

[A Dual-Imaging Speed-Enhanced CMOS Image Sensor for Real-Time Edge Image Extraction](#)

Hyeon-June Kim ; Sun-Il Hwang ; Jae-Hyun Chung ; Jong-Ho Park ; Seung-Tak Ryu

[A Compact-Area Low-VDDmin 6T SRAM With Improvement in Cell Stability, Read Speed, and Write Margin Using a Dual-Split-Control-Assist Scheme](#)

Meng-Fan Chang ; Chien-Fu Chen ; Ting-Hao Chang ; Chi-Chang Shuai ; Yen-Yao Wang ; Yi-Ju Chen ; Hiroyuki Yamauchi

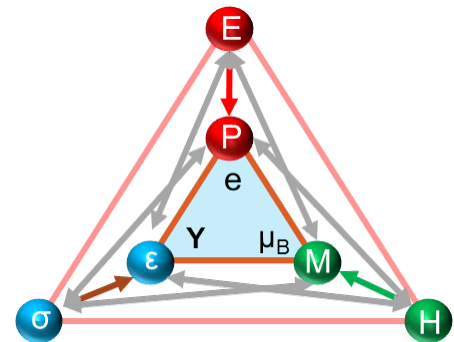
[Corrections to \$\hat{\epsilon}\$ A 10/20/30/40 MHz Feed-Forward FIR DAC Continuous-Time \$\hat{I}^{\hat{I}}\$ ADC With Robust Blocker Performance for Radio Receivers](#)

Sebastian Loeda ; Jeffrey Harrison ; Franck Pourchet ; Andrew Adams

IEEE Journal on Exploratory Solid-State Computational Devices and Circuits

Mid-Year Highlights

In the first half of 2017, the Journal on Exploratory Solid-State Computational Devices and Circuits had top five of the papers published which already appear in the top 8 of the journal's most accessed papers. These papers include:



[An Energy-Efficient Digital ReRAM-Crossbar-Based CNN With Bitwise Parallelism](#)

Leibin Ni ; Zichuan Liu ; Hao Yu ; Rajiv V. Joshi

[Nonboolean Pattern Recognition Using Chains of Coupled CMOS Oscillators as Discriminant Circuits](#)

Vahnood Pourahmad ; Sasikanth Manipatruni ; Dmitri Nikonov ; Ian Young ; Ehsan Afshari

[Compact Modeling of Distributed Effects in 2-D Vertical Tunnel FETs and Their Impact on DC and RF Performances](#)

Jie Min ; Peter M. Asbeck

[Nonvolatile Spintronic Memory Array Performance Benchmarking Based on Three-Terminal Memory Cell](#)

Chenyun Pan ; Azad Naeemi

[CoMET: Composite-Input Magnetoelectric- Based Logic Technology](#)

Meghna G. Mankalale ; Zhaoxin Liang ; Zhengyang Zhao ; Chris H. Kim ; Jian-Ping Wang ; Sachin S. Sapatnekar

[Electrical-Spin Transduction for CMOS-Spintronic Interface and Long-Range Interconnects](#)

Rouhollah Mousavi Iraei ; Sasikanth Manipatruni ; Dmitri E. Nikonov ; Ian A. Young ; Azad Naeemi

JxCDC papers listed in order of popularity can be found online [HERE](#).

For paper submission details, click [HERE](#).

Seeking News

Please send any chapter news or happenings (Distinguished Lecturer visits, events hosted by your SSCS chapter, awards received by members, etc) to Abira Sengupta, SSCS Magazine News Editor, for inclusion in an upcoming issue of the magazine. Please email - Abira.Sengupta@ieee.org. We look forward to receiving your news articles!

For more chapter news, [check out](#) the **Summer 2017 issue of the Solid-State Circuits Magazine**.

FEEDBACK

Let us know what you think! Please [email us](#) to send us your comments about the newsletter, what you would like to see included each month, or any other comments.

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