IEEE SOLID-STATE CIRCUITS SOCIETY
Where ICs are in IEEE

April 2018

NEWS

UPCOMING SSCS WEBINAR

Low Power Techniques for Successive Approximation ADCs

Thursday, May 24, 2018
11:00 AM ET
Presenter: Professor Pieter Harpe, Eindhoven University of Technology

Abstract: Successive Approximation (SAR) ADCs have received an increasing amount of interest in the past decade, covering a broad range of specifications and applications. Large contributors to their success are their inherent power efficiency, simplicity of design, and process scalability. In particular, this webinar covers the design of low power SAR ADCs, suitable for the Internet-of-Things, wearable sensors, and other low-power applications. Being on the border between analog and digital domains, the optimization of SAR ADCs has challenges and opportunities on both sides, giving ample room for creative solutions at various levels. This talk starts with an overview of possibilities at circuit, layout, architecture and algorithm levels covering all of the components in a SAR ADC. Examples from literature are used for illustration. Next, the talk will discuss practical SAR ADC implementations in detail, emphasizing the techniques being used to boost the ADCs' efficiency and resolution. The talk concludes with an outlook regarding limitations as well as future challenges and opportunities.

Bio: Pieter Harpe (SM'15) received the M.Sc. and Ph.D. degrees from the Eindhoven University of Technology, The Netherlands, in 2004 and 2010, respectively. From 2008 to 2011, he was a researcher at Holst Centre/imec, The Netherlands, where he worked on ultra low-power wireless transceivers,

with a main focus on ADC research and design. In April 2011, he joined Eindhoven University of Technology where he is currently an Associate Professor on low-power mixed-signal circuits. Dr. Harpe is co-organizer of the yearly workshop on Advances in Analog Circuit Design (AACD) and TPC member for ESSCIRC, where he chairs the analog track. He also served as TPC member for ISSCC, was IEEE Solid-State Circuits Society Distinguished Lecturer in 2016-2017, and is recipient of the ISSCC 2015 Distinguished Technical Paper Award.

Please note that moving forward all SSCS webinar registrations will be processed through the SSCS Resource Center. SSCS webinars are a members-only benefit. If you are not an SSCS member and would like to attend an SSCS webinar, a fee will be charged. If you have any questions about this policy, please email sscs-staff@ieee.org.

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Women in Engineering Networking Event at VLSI Symposium 2018

Tuesday, June 19th
6 PM
TAPA 3 Room
Hilton Hawaii Village, Honolulu, Hawaii

Special Guest: Barbara De Salvo, Chief Scientist and Deputy Director of CEA-Leti, Grenoble, France

Build and sustain a community among women in engineering. Meet and network with female luminaries in engineering.

This event is open to all genders and everyone in all phases of their careers.

CLICK HERE TO RSVP
Walk-in's are also welcome!

SSCS & EDS Joint Mentoring Session at VLSI Symposium 2018

Wednesday, June 20th
6 PM
TAPA 3 Room, Hilton Hawaiian Village,
Honolulu, Hawaii

- Complimentary event for all students, faculty, & engineers within 15 years of their first degree, even if not registered for the conference.
- Leading experts from industry and academia, IEEE SSCS & EDS Executives and Distinguished Leaders will share their experiences
- 1 on 1 answers to all your questions on publications, entrepreneurship, industry vs. academia and career coaching.
- Free T-Shirt to event attendees and all student participants get complimentary SSCS & EDS membership.
- Learn about SSCS & EDS member benefits for young engineers & students

CLICK HERE TO RSVP
Walk-in's are also welcome!

SSCS Members can Join CASS for Just $5

As a member of the IEEE Solid-State Circuits Society, you can add **IEEE Circuits and Systems Society (CASS)** annual membership for just $5.

More than 20% of SSCS members are already members of CASS.

If you have not yet renewed for 2018, join CASS for just $5 by entering promotion code SSCXCAS2018 at checkout. If you have already renewed for 2018, sign in with your **IEEE account** and the discounted CASS membership will be present in your cart.

EDUCATION

May 2018 Distinguished Lectures

CHAPTER	TALK DETAILS	DATE	LOCATION
SSCS Boston	Data Converters and their performance metrics by Ahmed Ali	May 4, 2018	Tufts University **Click here for more information**
SSCS Central Texas	Talk Title TBD by Youngcheol Chae	May 11, 2018	Location TBD

			Click here for more information
SSCS Tokyo	Jitter in Data Converters and Wireline Circuits	May 17, 2018	University of Tokyo **Click here for more information**
SSCS Montreal	Hybrid PLL architectures and implementations by Daniel Friedman	May 18, 2018	Polytechnique Montreal **Click here for more information**
SSCS Montreal	Sensor Interface Circuits by Nick Van Helleputte	May 18, 2018	Polytechnique Montreal **Click here for more information**
SSCS Italy	Talk Title TBD by Jun Ohta	May 25, 2018	Politecnico di Torino, Torino, Italy **Click here for more information**

CONFERENCES

Upcoming Conferences

2018 IEEE Radio Frequency Integrated Circuits Symposium (RFIC) Philadelphia, PA	**June 10 - 12, 2018**
2018 IEEE Symposium on VLSI Technology Honolulu, HI	**June 18 - 22, 2018**
2018 IEEE Symposium on VLSI Circuits Honolulu, HI	**June 18 - 22, 2018**
2018 IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED) Seattle, WA	**July 23 - 25, 2018**
ESSCIRC/ESSDERC 2018 - 44th European Solid-State Circuits Conference/44th European Solid-State Device Research Conference Dresden, Germany	**September 3 - 6, 2018**
2018 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS) San Diego, CA	**October 14 - 17, 2018**
2018 IEEE Biomedical Circuits and Systems Conference (BioCAS) Cleveland, OH	**October 17 - 19, 2018**
2018 IEEE Asian Solid-State Circuits Conference (A-SSCC) Tainan, Taiwan	**November 5 - 7, 2018**

2018 RFIC Symposium

June 10 - 12, 2018

Philadelphia, Pennsylvania

We cordially invite you to participate in the **2018 IEEE Radio Frequency Integrated Circuits Symposium (RFIC 2018)**. This international event will be held in Philadelphia, PA from 10-12 June, 2018. The RFIC Symposium is the premier integrated circuit (IC) design conference focused exclusively on the latest advances in RF, microwave, and millimeter-wave IC technologies and designs, as well as innovations in high-frequency analog/mixed-signal ICs and ultra-low power radios. With a wide range of papers from industry and academia, all attendees will find plenty of relevant and technically interesting topics to choose from!

The RFIC Symposium is an annual IEEE conference that is co-located with the International Microwave Symposium (IMS), ARFTG, and the Industry Exhibition to form "Microwave Week", the largest worldwide RF/microwave technical meeting of the year. This year, the Microwave week key themes are "Microwaves, Medicine, and Mobility", and the 2018 International Microwave Biomedical Conference (IMBioC) will be part of the Microwave Week in parallel to IMS, RFIC, and ARFTG. The Microwave Week will be held at the Pennsylvania Convention Center in Philadelphia, PA. In addition to the vast array of technical content, attendees will have the opportunity to interact with world experts, expand their networks, and leave invigorated with new ideas and a drive to innovate.

The 2018 RFIC Symposium will begin on Sunday, 10 June 2018, with 12 RFIC focused workshops (8 full day and 4 half day). In addition, there will be several joint RFIC/IMS workshops on Sunday and Monday. These workshops cover a wide range of advanced topics in RFIC technology and IC design, including 5G systems and beyond.

12 Sunday RFIC Focused Workshops include the following topics:

- RFIC Design in CMOS FinFET and FD-SOI
- ICs for Quantum Computing and Quantum Technologies
- 5G mm-Wave Power Amplifiers, Transmitters, and Beamforming Techniques with Massive MIMO
- eXtreme-bandwidth architecture for RF and mmW transceivers in nanoscale CMOS
- Integrated mm-wave & THz sensing technology for automotive, industrial and healthcare
- Advanced integrated RF filtering circuits and techniques
- Synthesizer Design and Frequency Generation/Synchronization Schemes for High-Performance Wireless Systems
- High-performance WLAN Transceiver Design and Calibration Techniques
- High Efficiency Power Amplification for Emerging Wireless Communication Solutions from Devices to Circuits and Systems
- Millimeter-wave Systems, Manufacturing, Packaging and Built-in Self-Test
- Towards Direct Digital RF Transceivers
- Ultra Low-Power Transceiver SoC Designs for IoT Applications

Following the full day of workshops, the RFIC Plenary Session will be held on Sunday evening beginning with conference highlights, the presentation of the Student Paper Awards, and the Industry Paper Awards. The plenary session talks begin with Mr. Zachary J. Lemnios, Vice President of Science, Technology, and Government programs at IBM research, who will talk about "Compact Silicon Integrated mmWave Circuits: From Skepticism to 5G and Beyond"; the second talk will be given by NXP's Automotive Chief Technology Officer, Mr. Lars Reger, who will share his vision on "The road ahead for autonomous cars - what's in for RFIC". Immediately following the plenary session will be the RFIC reception that will highlight our industry showcase and student paper finalists in an engaging social and interactive technical evening event supported by the RFIC Symposium corporate sponsors. You will not want to miss the RFIC Reception this year!

On Monday and Tuesday, RFIC will have multiple tracks of oral technical paper sessions as well as the popular Interactive Forum poster session.

17 Technical Paper Sessions on Monday and Tuesday include the following topics:

- Building Blocks for 5G Transceivers
- Advances in Packaging, Modeling and Optical Phased Arrays
- Techniques for High-Performance Frequency Synthesis
- 28 GHz Phased Arrays, Beamformers and Sub-Components for 5G Applications
- Technology Optimization for RF Applications
- ADC-Based RF/Mixed-Signal Systems and Wireline Transceiver Techniques
- RF Front-Ends for Emerging Wireless Paradigms
- Mixed Signal Transmitters and Power Amplifiers
- cm/mm-Wave CMOS Integrated Phased-Array Building Blocks
- Ultra-Low Power Radios for Security, Ranging and Connectivity
- Silicon Integrated mm-Wave Transmitters
- Highly Efficient mm-Wave Oscillators with Wide Tuning Range
- mm-Wave Power Amplifiers
- Submillimeter Wave and Terahertz ICs
- mm-Wave Radar and Beamforming Transceivers
- mm-Wave LNAs and RF Receiver Front-Ends
- Wireless Transceivers and Transmitters for Connectivity and Cellular

Enlightening lunchtime panels focusing on the Microwave Week key themes will be featured on both days. The Monday panel session, titled "How will the future self-driving cars see? Lidar vs Radar", will cover the state of the art in radar and lidar technologies and attempt to draw contrasts between the two approaches in the context of self-driving cars. The Tuesday panel session, titled "Can a residential wireless Gbps internet connection compete with wired alternatives?", will convene expert panelists to discuss some of the technology advancements that are enabling Gbps internet connections and will debate the merits of both the wired and wireless technology alternatives. Please make sure to bring your engaging opinions and questions to both panel sessions and they will be highly interactive!

The 5G Summit technical sessions on Tuesday will provide high-level 5G overview presentations that will complement the 5G-focused RFIC technical sessions on Monday morning. A separate registration will be required for the 5G Summit sessions.
On behalf of the RFIC Steering and Executive Committees, we welcome you to join us at the 2018 RFIC Symposium in Philadelphia, Pennsylvania!

Please visit the RFIC 2018 website **(http://rfic-ieee.org/)** for more details and updates.

2018 Symposia on VLSI Technology and Circuits

June 18 - 22, 2018
Honolulu, Hawaii

Registration is open now, and the deadline for the early discount is May 24th.

The **2018 Symposia on VLSI Technology & Circuits** will deliver a unique perspective built around the theme of "Technology, Circuits & Systems for Smart Living." The Symposia program integrates advanced technology developments, innovative circuit design, and the applications that they enable as part of our global society's adoption of smart, connected devices and systems that change the way humans interact with each other.

This weeklong conference is packed with technical presentations, a demonstration session, panel discussions, and focus sessions. There will be two full-day short courses on "Designing for the Next Wave of Cloud Computing" and "Bio-Sensors, Circuits, and Systems for Wearable and Implantable Medical Devices." The plenary sessions will explore the impact of circuits on higher-level systems, including Bill Dally of nVidia speaking on artificial intelligence, and Tsuneo Komatsuzaki of SECOM discussing security service platforms.

New to the Hawaii Symposia is a Friday Forum, June 22nd, on "Machine Learning Today and Tomorrow", which will include talks from academia and industry thought leaders, providing insight into the complex and dynamic landscape of machine-learning algorithms, their uses, and the technological trends driving their progression.

We look forward to seeing you all at 2018 VLSI Symposia in Honolulu!

Click here for more information.

CALL FOR PAPERS

BioCAS 2018: Call for Papers
Biomedical Circuits and Systems Conference

October 17 - 19, 2018
Cleveland, OH

BioCAS 2018 is a premier international forum for presenting the interdisciplinary research and development activities at the crossroads of medicine, life sciences, physical sciences and engineering that shape tomorrow's medical devices and healthcare systems.
This conference brings together members of our communities to broaden their knowledge in emerging areas of research at the interface of the life sciences and the circuits and systems engineering. The three-day single-track program for BioCAS 2018 is multidisciplinary in topics including but not limited to:

Biomedical Technologies
* Assistive, Rehabilitation, and Quality of Life Technologies
* Biofeedback, Neuromodulation, and Closed-Loop Systems
* Bio-Inspired and Neuromorphic Circuits and Systems
* Biosensor Devices and Interface Circuits
* Biotelemetry and Energy Harvesting/Scavenging Circuits and Systems
* Body Area/Sensor Network and Wireless/Wearable Health Monitoring
* Electronics for Neuroscience
* Implantable Medical Electronics
* Lab-on-Chip and BioMEMS

Biomedical Applications
* Point-of-Care Technologies for Healthcare
* Biomedical Imaging and Image Processing
* Biosignal Recording, Processing, and Machine Learning
* Genomics and Systems Biology
* Human-Machine Interfaces
* Medical Information Systems and Bioinformatics

Submission Guidelines
The complete 4-page paper (in standard IEEE double-column format), including the title, authors' names, affiliations and e-mail addresses, as well as a short abstract and an optional

demonstration video link (3 minute max) are requested. Papers must be submitted electronically in PDF format through **www.biocas2018.org.**

Important Dates
Monday, June 11, 2018: Regular Paper Submission Deadline
Monday, July 16, 2018: Live Demo Session deadline
Monday, August 13, 2018: Author Notification Date
Friday, August 31, 2018: Author Registration/Final Paper Submission Deadline

A-SSCC 2018: Call for Papers
IEEE Asian Solid-State Circuits Conference

Conference Theme: Silicon Enabling Mobile Intelligence

The miniaturized silicon technology enabled big success in the realization of software solutions such as machine learning, big data, virtual and augmented realty in the image and speech recognition, the medical diagnosis and the autonomous driving automobiles. The current software solutions, however, consume huge power by employing cloud computers along with many graphic processing units and a large amount of memory. Nowadays, the integrated circuit design community tries to develop efficient low-power mobile intelligence solutions by taking challenges in the design of digital and analog circuits, processor architecture, and system for compact IoT devices.

Prospective authors are invited to submit four-page or two page (NEW) manuscripts, including figures, tables, and references to the official A-SSCC 2018 website. The two-page submission can include two-page supplements with figures and figure captions. All papers will be handled and reviewed electronically.

Papers are solicited in the following categories:

Regular Session

1. **Analog Circuits & Systems:** Amplifiers, comparators, switched capacitor circuits, continuous-time & discrete-time filters, voltage/current references;DC- DC converters, power-control circuits; IF/baseband analog circuits, AGC/VGA; non-linear analog circuits.

2. **Data Converters**: Nyquist-rate and oversampling A/D and D/A converters, time-to-digital converters, and capacitance-to-digital converters; sub-circuits for data converters including sample-and-hold circuits, calibration circuits, etc.

3. **Digital Circuits & Systems**: Design, fabrication, and test of digital VLSI systems; high-speed low-power digital circuits, power-reduction and management methods for digital VLSI, ultra-low-voltage and sub-threshold logic design; leakage reduction techniques; clock distribution, I/O circuits, reconfigurable logic-array circuits; supply/substrate noise measurement and cancellation for digital VLSI, variation and fault-tolerant circuits.

4. **SoC & Signal Processing Systems:** System-on-chip(including 3D integration), microprocessors, network processors, baseband communication processing system & architectures, system-level power management; multimedia and recognition processing systems; cryptographic, security, machine-learning, deep-learning, and neuromorphic circuits and systems; bio-medical/neural-network processors and sensor network systems.

5. **RF:** Receivers/transmitters/transceivers for wireless systems; narrowband RF, ultra-wideband and millimeter-wave circuits; circuits and building-blocks including RF front-end, LNA, mixer, power amplifiers, VCOs, frequency synthesizers, RF filters, RF switches, power detectors, active antennas.

6. **Wireline:** Receivers/transmitters/transceivers for wireline systems; optical/electrical data links and backplane transceivers; power-line communication; clock generation circuits, PLL, DLL, spread-spectrum clock generation; building blocks for high-speed wireline communication; analog-digital mixed-mode circuits.

7. **Emerging Technologies and Applications:** Advanced system designs and circuit solutions for technologies and applications including state-of-the-art devices and packaging technologies; flexible and printable electronics; smart sensors and transducers; MEMS for analog, RF, and sensor applications; image sensors and displays; energy harvesting systems; transceiver systems; medical/bio-electronics/bio-inspired chip design and silicon systems.

8. **Memory**: Volatile and Non-volatile memory; new memory designs for 3D/2D architectures, emerging devices such as resistive-/phase change-/magnetic-/ferro-electric- memory devices; data storage and multi-bit-cell memory design; cache-memory system, multi-port memory, memory subsystem, processing in memory, and CAM design; yield-enhancing and ECC techniques; memory testing and built-in self-test.

Special Session

1. Industry Program: This special category accepts only papers based on state-of-the-art industrial products. Strong emphasis on systems realized by silicon chips is encouraged. The papers should cover architecture, circuits, process technology, packaging and testing, including characterization results, die and system photos, as well as product demos.

2. Student Design Contest: A student design contest is held among the accepted papers with system prototypes or measurement results of which operations can be demonstrated on-site. Refer to the web for further information.

3. FPGA Session (NEW) : This session accepts papers describing FPGA implementation with novel algorithm and/or architecture. The demo results(eg. video or slide) must be included in the paper submission. The authors of accepted papers are required to participate in demo sessions.

Papers related to integrated circuits for intelligent systems are highly solicited. Papers on low-power and/or low-voltage approaches, signal integrity, noise, test, and manufacturability for all the above categories are welcomed. Measurement results are highly recommended, especially for analog, and RF categories. Design methodologies for SiP, and SoC are included in the scope of the conference; the papers only describing CAD tools and CAD algorithms are not considered. Authors must follow detailed instructions provided within the "Authors" section of the website, including the Authors' Guide and Pre-publication Policy. The technical content beyond the abstract of the accepted paper must not be announced, published, or in any way put in the public domain prior to the Conference. Extended versions of selected papers from the Conference will be published in a Special Issue of the IEEE Journal of Solid-State Circuits.

Important Dates

Paper Submission: June 3, 2018 (20:00 GMT)
Acceptance Notification: August 6, 2018
Final Paper Submission: September 9, 2018

PUBLICATIONS

The latest in SSCS Flagship Publications...

IEEE Solid-State Circuits Letters

Volume 1, Issue 2, February 2018

A 99% Current Efficient Three-Transistor Regulator With Built-In 80 ppm/Â°C Reference, for 0-10 mA Loads Gajendranath Chowdary ; T. R. Aashish ; Shouri Chatterjee
A 0.7-V 0.43-pJ/cycle Wakeup Timer Based on a Bang-Bang Digital-Intensive Frequency-Locked-Loop for IoT Applications Ming Ding ; Zhihao Zhou ; Yao-Hong Liu ; Stefano Traferro ; Christian Bachmann ; Kathleen Philips ; Fabio Sebastiano
Energy-Efficient Wide-Range Voltage Level Shifters Reaching 4.2 fJ/Transition Reza Lotfi ; Mehdi Saberi ; S. Rasool Hosseini ; Amir Reza Ahmadi-Mehr ; Robert Bogdan Staszewski
A 0.25-1.7-GHz, 3.9-13.7-mW Power-Scalable, -10-dBm Harmonic Blocker-Tolerant Mixer-First RF-to-Digital Receiver for Massive MIMO Applications Konstantin Trotskovsky ; Amy Whitcombe ; Gregory Lacaille ; Antonio Puglielli ; Pengpeng Lu ; Zhongkai Wang ; Nathan Narevsky ; Gregory Wright ; Ali M. Niknejad ; Borivoje Nikolić ; Elad Alon
A 0.87-pJ/b 115-Gb/s 27 -1 PRBS Generator in 130-nm SiGe:C BiCMOS Technology P. Rito ; I. García López ; M. Ko ; A. C. Ulusoy ; D. Kissinger
A 26-Gb/s 0.31-pJ/bit Receiver With Linear Sampling Phase Detector for Data and Edge Equalization Guang Zhu ; Yipeng Wang ; C. Patrick Yue
A 1.66 mV FOM Output Cap-Less LDO With Current-Reused Dynamic Biasing and 20 ns Settling Time Chirag Desai ; Debashis Mandal ; Bertan Bakkaloglu ; Sayfe Kiaei

IEEE Journal of Solid-State Circuits

Vol. 53, Issue 5, May 2018

Introduction to the Special Section on the 2017 RFIC Symposium Osama Shana'a
A 28-GHz CMOS Direct Conversion Transceiver With Packaged 2times4 Antenna Array for 5G Cellular System Hong-Teuk Kim ; Byoung-Sun Park ; Seong-Sik Song ; Tak-Su Moon ; So-Hyeong Kim ; Jong-Moon Kim ; Ji-Young Chang ; Yo-Chul Ho

A Low-Cost Scalable 32-Element 28-GHz Phased Array Transceiver for 5G Communication Links Based on a 2times2 Beamformer Flip-Chip Unit Cell
Kerim Kibaroglu ; Mustafa Sayginer ; Gabriel M. Rebeiz

A 25-30 GHz Fully-Connected Hybrid Beamforming Receiver for MIMO Communication
Susnata Mondal ; Rahul Singh ; Ahmed I. Hussein ; Jeyanandh Paramesh

A Wideband Class-AB Power Amplifier With 29-57-GHz AM-PM Compensation in 0.9-V 28-nm Bulk CMOS
Marco Vigilante ; Patrick Reynaert

A 16-Element 4-Beam 1 GHz IF 100 MHz Bandwidth Interleaved Bit Stream Digital Beamformer in 40 nm CMOS
Sunmin Jang ; Jaehun Jeong ; Rundao Lu ; Michael P. Flynn

High-Power Radiation at 1 THz in Silicon: A Fully Scalable Array Using a Multi-Functional Radiating Mesh Structure
Zhi Hu ; Mehmet Kaynak ; Ruonan Han

A Dual-Loop Synthesizer With Fast Frequency Modulation Ability for 77/79 GHz FMCW Automotive Radar Applications
Jakob Vovnoboy ; Run Levinger ; Nadav Mazor ; Danny Elad

Frequency and Power Scaling in mm-Wave Colpitts Oscillators
Alireza Imani ; Hossein Hashemi

Enhanced-Selectivity High-Linearity Low-Noise Mixer-First Receiver With Complex Pole Pair Due to Capacitive Positive Feedback
Yuan-Ching Lien ; Eric A. M. Klumperink ; Bernard Tenbroek ; Jon Strange ; Bram Nauta

A Wideband Linear I/Q -Interleaving DDRM
Mohammadreza Mehrpoo ; Mohsen Hashemi ; Yiyu Shen ; Leo C. N. de Vreede ; Morteza S. Alavi

Outphasing Class-E Power Amplifiers: From Theory to Back-Off Efficiency Improvement
Ali Ghahremani ; Anne-Johan Annema ; Bram Nauta

An Interferer-Tolerant CMOS Code-Domain Receiver Based on N-Path Filters
Abhishek Agrawal ; Arun Natarajan

A Wideband Receiver Employing PWM-Based Harmonic Rejection Downconversion
Heechai Kang ; Wei-Gi Ho ; Vineet Kumar Singh ; Ranjit Gharpurey

802.11g/n Compliant Fully Integrated Wake-Up Receiver With âˆ'72-dBm Sensitivity in 14-nm FinFET CMOS
Erkan Alpman ; Ahmad Khairi ; Richard Dorrance ; Minyoung Park ; V. Srinivasa Somayazulu ; Jeffrey R. Foerster ; Ashoke Ravi ; Jeyanandh Paramesh ; Stefano Pellerano

A 2.4-GHz, Sub-1-V, 2.8-dB NF, 475- u W Dual-Path Noise and Nonlinearity Cancelling LNA for Ultra-Low-Power Radios
Mustafijur Rahman ; Ramesh Harjani

A SAW-Less Tunable RF Front End for FDD and IBFD Combining an Electrical-Balance Duplexer and a Switched-LC N-Path LNA
Gengzhen Qi ; Barend van Liempd ; Pui-In Mak ; Rui P. Martins ; Jan Craninckx

A Fully On-Chip 80-pJ/b OOK Super-Regenerative Receiver With Sensitivity-Data Rate Tradeoff Capability
Vahid Dabbagh Rezaei ; Kamran Entesari

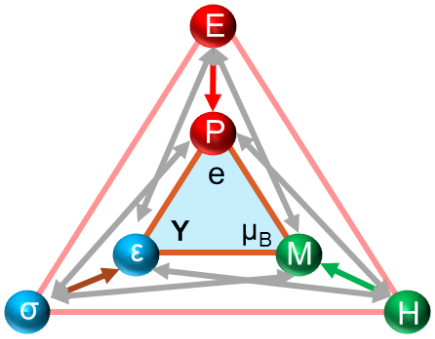
Analysis and Design of a 30- to 220-GHz Balanced Cascaded Single-Stage Distributed Amplifier in 130-nm SiGe BiCMOS
Paolo Valerio Testa ; Corrado Carta ; Udo Jörges ; Frank Ellinger

Analysis and Design of a 20-MHz Bandwidth, 50.5-dBm OOB-IIP3, and 5.4-mW TIA for SAW-Less Receivers
Giacomo Pini ; Danilo Manstretta ; Rinaldo Castello

Precision Passive-Charge-Sharing SAR ADC: Analysis, Design, and Measurement

Results Baozhen Chen ; Mark Maddox ; Michael C. W. Coln ; Ye Lu ; Lalinda D. Fernando
A Nyquist Rate SAR ADC Employing Incremental Sigma Delta DAC Achieving Peak SFDR = 107 dB at 80 kS/s Ahmad AlMarashli ; Jens Anders ; Joachim Becker ; Maurits Ortmanns
A 10-bit 2.6-GS/s Time-Interleaved SAR ADC With a Digital-Mixing Timing-Skew Calibration Technique Chin-Yu Lin ; Yen-Hsin Wei ; Tai-Cheng Lee
A 50-Gb/s High-Sensitivity (âˆ'9.2 dBm) Low-Power (7.9 pJ/bit) Optical Receiver Based on 0.18- u m SiGe BiCMOS Technology Takashi Takemoto ; Yasunobu Matsuoka ; Hiroki Yamashita ; Yong Lee ; Hideo Arimoto ; Masaru Kokubo ; Tatemi Ido
A CMOS Timer-Injector Integrated Circuit for Self-Powered Sensing of Time-of-Occurrence Liang Zhou ; Kenji Aono ; Shantanu Chakrabartty
Asynchronous Approximation of a Center of Gravity for Pixel Detectorsâ€™ Readout Circuits Piotr Otfinowski ; Grzegorz W. Deptuch ; Piotr Maj

IEEE Journal on Exploratory Solid-State Computational Devices and Circuits



2018 Early Access Papers

Using Programmable Graphene Channels as Weights in Spin-Diffusive Neuromorphic Computing Jiaxi Hu ; Gordon Stecklein ; Yoska Anugrah ; Paul A. Crowell ; Steven J. Koester
BCB Evaluation of High-Performance and Low-Leakage Three-Independent-Gate Field Effect Transistors Jorge Romero-Gonzalez ; Pierre-Emmanuel Gaillardon
Tunnel FET Analog Benchmarking and Circuit Design Hao Lu ; Paolo Paletti ; Wenjun Li ; Patrick Fay ; Trond Ytterdal ; Alan Seabaugh
Improving Energy Efficiency of Low Voltage Logic by Technology-Driven Design Kaushik Vaidyanathan ; Daniel H. Morris ; Uygar E. Avci ; Huichu Liu ; Tanay Karnik ; Hong Wang ; Ian A. Young

JxCDC papers listed in order of popularity can be found online HERE.

For paper submission details, click HERE.

Seeking News

Please send any chapter news or happenings (Distinguished Lecturer visits, events hosted by your SSCS chapter, awards received by members, etc) to Abira Sengupta, SSCS Magazine News Editor, for inclusion in an upcoming issue of the magazine. Please email - **Abira.Sengupta@ieee.org**. We look forward to receiving your news articles!

For more chapter news, check out the Winter 2018 issue of the Solid-State Circuits Magazine.

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