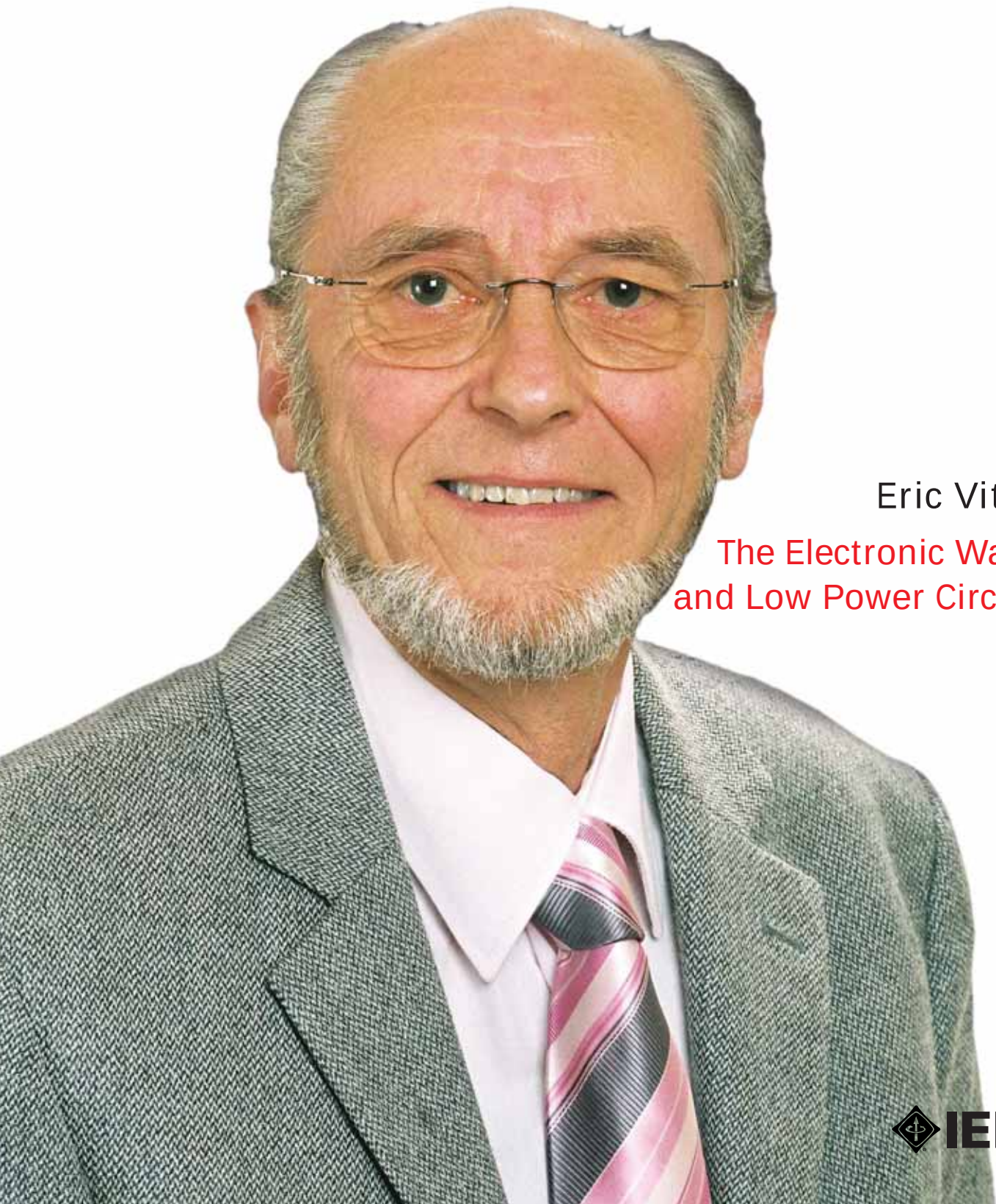
SSCS

IEEE SOLID-STATE CIRCUITS SOCIETY NEWS

Summer 2008 Vol. 13, No. 3 www.ieee.org/sscs-news



Eric Vittoz

The Electronic Watch and Low Power Circuits

IEEE

Editor's Column

Mary Y. Lanzerotti, IBM, myl@us.ibm.com

Welcome to the Summer 2008 issue of SSCS News!

As with prior issues, its goal is to be a self-contained resource, with original sources and new contributions by experts describing the current state of affairs in technology in view of the influence of the original papers and/or patents.

In Summer 2008, we feature the work and impact of Dr. Eric Vittoz, who has written an extensive lead article entitled "Electronic Watch and Low Power Circuits." I am grateful to Dr. Erik Heijne for suggesting Dr. Vittoz as a potential subject and feature author, and for his recommendations of experts who could attest to the impact of Dr. Vittoz's career on the development and commercialization of electronic Swiss watches. Please be sure to read Dr. Heijne's Introduction to this issue on page 4.

As a result, we are honored to offer:

(1) "A Short Story of the EKV MOS Transistor Model," by Christian C. Enz (Swiss Center for Electronics and Microtechnology);

(2) "Watch Microelectronics: Pioneer in Portable Consumer Electronics," by Mougahed Darwish, Marc Degrauwe, Thomas E. Gyger, Gunther Meusburger, (all at EM Microelectronic-Marin SA), Jean Claude Robert (ETA);

(3) "It's About Time: A Brief Chronology of Chronometry," by Thomas Lee (Stanford University);

(4) "History of the Development of the Swiss Watch Microprocessors," by Christian Piguet (CSEM Centre Suisse d'Electronique et de Microtechnique S.A.);

(5) "Eric Vittoz and the Strong Impact of Weak Inversion Circuits," by Yannis Tsividis (Columbia University).

Summer '08 also includes reprints of one original paper and the first two pages of two original patents by Dr. Vittoz:

(1) F. Leuenberger and E. Vittoz, "Complementary-MOS Low-Power Low-Voltage Integrated Binary Counter," Proceedings of the IEEE, Vol. 57, No. 9, September, 1969, pp. 1528-1532.

(2) E. A. Vittoz, "Frequency Divider Circuit," U. S. Patent 3,619,646, Nov. 9, 1971.

(3) W. Hammer, E. A. Vittoz, J. Hermann, H. Choffat, "Timekeeper," U. S. Patent 3,895, 485, July 22, 1975.

To accentuate the impact of Dr. Vittoz's work, I would like to include two photographs that I took of the Swatch store in Grand Central Terminal, New York, NY. (This store is directly on the walking path from the train to the subway.)

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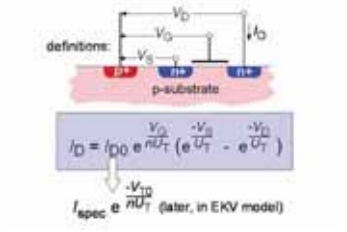
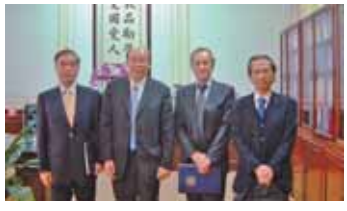
SOLID-STATE CIRCUITS SOCIETY

Where ICs are in IEEE

Summer 2008 Volume 13, Number 3

Photo of Eric Vittoz





President's Message

Willy Sansen, K. U. Leuven, willy.sansen@esat.kuleuven.be

SCS members ask me, is hardware disappearing? (They seem to be worried.) Is this an observation, or is it the conclusion of some hardware vs. software panel?

Where has hardware gone? Has it gone virtual, or has it been globalized out?

Hardware is, for example, my car. It is not gone. I sit in it and I drive it, thanks to all the software inside. The chips in my car are also hardware, but they have been realized thanks to software.

Our "Red Rag" as a Canvas

The Journal of Solid-State Circuits is also hardware. It is a thick pack of paper we are used to receiving every month by mail. We glance through, we turn pages, like walking through a painting exhibit. Once in a while we stop and allow the content to seep through. We notice the painter made it twenty years ago. We try to understand what it tries to say, but we don't. We feel something is there, but it will take more time to understand. It will take more effort as well. Right now we don't have the time. We will go through it later, somewhere, when we have more time.

The JSSC Goes Green

Today the Journal in paper form is disappearing. Environmentalists have convinced us that sending thousands of pages to readers who look at only a few makes too heavy a carbon print on our precious world. So the Journal in paper has gone virtual; it has turned into a passworded list of numbers on a website. Of course, we have kept the last paper copy in the lowest drawer of our desk so we can show it to our grandchildren; and we smile at their remarks that this is what we indulged in some time ago. So we remember and we still like the red color of that red rag. Now the red rag has gone green. It has been virtualized together, perhaps, with our desk.

Unpeeling the Circuit Paper

We need our Journal for learning. -- Learning is life, and this we need. How much have we actually learned from the JSSC?

Looking at a painting never teaches you all. Going through a paper never reveals all its secrets. Nowadays the circuit "paper" comes in layers. The title and abstract contain its entire performance, and it is searchable. As with a number of technical terms, all paintings [sorry, technical exhibits] are revealed and explained and put in a comparative table with the FOM of its kind. The next layer goes up or down. Up are all applications, down are the circuit details. The paper is organized per screen (or slide). Only one delta of understanding is added per screen. The longer we follow, the more our insight is built up. At the end we see some SPICE files and curves. Who would actually go that far? Only someone who wants to use the circuit. First some money must be paid, however. On the lowest level, I can do a redesign, according to my specs. The design procedure is then started a few layers higher, and my version is ready. More money is needed to get a hardware version, and some more time.

Has Chip Design Gone Virtual?

This circuit was submitted to the Journal only three weeks ago. Only a few comments by a few experts have been added since then. More will be added later on, I am sure. I have to add mine as well, if I use it. Otherwise much more money is required.

Thus, design has gone virtual now, or is it the hardware (chip) which has gone virtual? Has the design of this hardware gone soft?

A conference is like the premiere of a painting exhibit. We receive a catalogue beforehand. Then we get together with a few colleagues or friends to make a short tour; we exchange our impressions, and on the reception at the end, we have a drink, free for SSCS members.

Introduction

Erik H.M. Heijne, CERN, Erik.heijne@cern.ch

Microelectronics profoundly impacts consumer products and habits, and the products themselves put rigorous constraints on microelectronics. This reciprocity is perfectly illustrated by the summer 2008 issue of the SSCS News.

The historical accounts given by some of the actors show how the use of microelectronics circuits in wristwatches has forced them to improve power usage far beyond earlier limits. Also required were better understanding and improved tools for device and circuit simulation.

About a year ago, I suggested to Mary Lanzerotti and her colleagues that Eric Vittoz and his contributions to low power microelectronics might be a good subject for an issue of the Society News. Mary has implemented this in a marvelous way by contacting and stimulating the authors and by coordinating the issue that you have in hand. I am certain that the authors' enthusiasm and informed accounts will lead to new ideas and stimulate many in our community, demonstrating the dynamic of the IEEE as an international community of engineers with high profile and great potential, including expertise in the area of low power.

Symbiosis in the Technology World

Tony Harker, ISLI Alba Centre, tony.harker@sli-institute.ac.uk

Symbiosis has many subtly varied definitions depending upon your angle of attack. In broad terms it can be defined as an association between two or more bodies or groups that may benefit one or all members. When applied to the high technology world, it can manifest in multiple ways, such as straight licence arrangements between suppliers all the way up to complex multi-faceted collaborative agreements between global bodies. Either way, the outcome should be of clear benefit to all involved. Once this arrangement breaks down, it can easily move into a no-benefit situation or indeed, in extreme cases, become a parasitic relationship.

The trick in any symbiotic arrangement is to choose your partner or partners carefully. It is also vital to bound the relationship with deliverables which enable you to track and measure output to help justify your resource expenditure. In the commercial world, return on investment is king. Participants should always be willing to pause or indeed cancel arrangements which do not yield useful results.

One excellent example of where symbiosis should, and in many cases does, work effectively is in the links between the commercial and academic worlds. This is particularly evident within Europe, where there are multiple instances of inter- and intra- University/Industry collaborations. However, one should not overlook the complexities of such arrangements and the inherent frustrations that they may bring to all parties.

Institutions such as IMEC, based in Belgium, have a commendable research record based upon close links with the nation's industrial base. This is mirrored by similar institutions in other countries, such as the Fraunhofer Institutes throughout Germany, LETI based in France, and the Institute for System Level Integration (iSLI) & Scottish Universities Physics Alliance (SUPA), both of which are based in the UK.

Potential investors, collaborative partners, staff and students mix at iSLI's 2008 open day.

In addition to the research groupings, there are also significant collaborations in which young companies assist one another by pooling resources and aim generally to represent the core of industry through broad based representation. Speaking for the UK and Ireland, there are several excellent examples of such activity: The National Microelectronics Institute (NMI) acts as a trade representative body which, amongst other things, brokers help to the overall industry to understand who and what is available to further their business. The SetSquared partnership amongst analogous organisations in the UK is based in the South of England and aims to assist young companies through incubation by providing direct help from seasoned entrepreneurs to access funding sources. MIDAS, based in Ireland, is a group comprised of individual companies, local offices of multinationals, and Universities who pool their needs to help create a local critical mass and share training resources.

More information on these bodies can be found at:

www.imec.be
www.fraunhofer.de
www.leti.fr
www.sli-instititute.ac.uk
www.supa.ac.uk
www.setsquared.co.uk
www.midas.com

Cross Border Collaboration – The EU Model

The recently announced European Institute of Technology (EIT) is a good example of a response to a perceived need in a specific geographical area. First broached during 2005, this pan-European entity was envisaged as helping to produce useable, wealth generating output whilst also fostering academic growth in the relevant institutions - a clear example of a true symbiotic relationship. The EIT has now gone through the consultative process and has been granted a budget in excess of 300M Euro to cover 2008-2013. The aim of the EIT is simple: to allow more wealth generation for the European Union by integrating education, research, and business-based innovation into the

"Knowledge Triangle." The proposed "hub and spoke" model includes a central governing body surrounded by "Innovation Communities" that are expected to relate closely to their localised needs. A key attribute in this case is the inclusion of the business community, which will aid the generation of useable outcome. Whilst still in its formative stages, the EIT promises to be an interesting, large scale attempt at bridging the academic and commercial world to bring benefits to all stakeholders.

For more information see ec.europa.eu/eit

Demonstrating prototypes to potential investors and researchers can pay dividends in product development.

Academic and Commercial Drivers

When dealing with the academic and commercial worlds, it is vital to realise that there are fundamental differences in the way that they are administered, how they function, and how goals and targets are set and met. Typically, academic bodies are set up to research "blue sky" topics and any fruits of this research are captured in the papers and kudos generated therein. The net contribution of such bodies is typically at a high level and adds to the net intellectual capital of countries and associated communities.

In many cases, blue sky research can spin off opportunities for more practical or applied research with more potential for commercial exploitation. It is more usual for symbiosis to manifest itself at this node than any other. The reason is very simple – there is opportunity for money to be made here in many different forms including IP licensing, spinout company formation, and contract-based, focused research/development.

The commercial world is driven by very different factors. Companies are in business to create wealth for their shareholders. They constantly need to stay ahead of competition through innovation, typically enslaved to a constantly evolving market. In the commercial world, particularly in the consumer market, products may have lifetimes counted in months before significant revisions are required. This in turn heaps more pressure on the development cycle and inherently more pressure on the innovation environment. Staying one step ahead of the game whilst maintaining margins keeps a lot of senior executives awake at night. It is therefore not surprising that many companies favour close relationships with academic partners to help fuel the innovative process.

Such relationships need to be handled carefully since they can be fraught with frustration on both sides. Some of the more commercially focused institutions have dedicated groups that specialize in the commercial interface. Commonly known as "Technology Transfer" or "Research and Enterprise" entities, such bodies are tasked with translating the needs and deliverables between the two worlds. People in these groups typically hail from both sides of the fence in that they can relate to the sometimes orthogonal requirements.

Engagement Models

When considering how to engage with any partner, it is fundamental to set down the terms and expected outcomes. Whilst this may seem obvious, it is surprising how many relationships can break down due to mismatches in expectation. It is therefore worthwhile building a reporting and measurement mechanism whereby progress can be measured. This can also aid in staged payment deals and acts as a convenient brake if a project starts to go off the rails. Importantly, the extent to which this structure is put in place heavily depends upon the parties involved and the nature of the programme. In some cases the value may lie in the unbounded, free thinking that academics can bring into the dynamics. In other cases closely confined, structured research may be more applicable to match the aspirations of the commercial partner. Either way, whatever is decided needs to be agreed upfront and be manageable. It can be easily argued that reporting and monitoring is not a value add activity. Indeed over-monitoring can stifle creativity and ultimately reduce the effectiveness of the partnership.

Large and small companies tend to be driven towards different engagement models. This is primarily driven by their spending power and their ability to mitigate the risk of slippage or failure to deliver a money-making result (not all research ends in a positive answer). Large companies tend to deal with more left field research since they are more easily able to offset this against other revenue generating

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The Electronic Watch and Low-Power Circuits

Eric A. Vittoz, IEEE Life Fellow member, evittoz@ieee.org

A New Research Laboratory

This story starts in 1962 with the foundation of CEH (Centre Electronique Horloger or "Watchmakers Electronic Center"). The bipolar junction transistor (BJT) was 14 years old and had already replaced the vacuum tube in most electronic systems. A few years had passed since the invention of the integrated circuit, followed by that of the planar process by Swiss born physicist Jean Hoerni.

The Swiss watch industry was flourishing, exporting about 45 million watches per year for a total value of 1.4 billion Swiss francs. But it was undergoing a deep structural mutation from its traditional organisation based on corporatism. The whole watch industry was of a fully mechanical nature and most of the technical managers had been educated as traditional watchmakers. However, for several years, a very few visionary managers had been watching the recent development taking place on the other side of the Atlantic Ocean, in this strange new domain for them called solid-state electronics.

Led by Gerard Bauer, the dynamic director of the Federation of the Swiss Watch Industry (FH), a research group representing the major Swiss manufacturers was created, to evaluate if and how this new electronics could once be applicable in some way to the wristwatch itself. Through the long existing LSRH ("Swiss Laboratory for Watch Research", founded in the 40's for research in all aspects of the mechanical watch), they entrusted the Swiss Technical Universities with some limited contracts to evaluate these possibilities. They received rather negative conclusions, but however decided that a new joint center would be created to search for possible new watch systems based on electronics. After receiving enthusiastic support from Sydney de Coulon, the general Director of Ebauches SA, the powerful producer of all Swiss watch components, they hired Roger Wellinger as technical Director to lead the project. A Swiss electrical engineer, Roger had spent 15 years in the USA, first as an Associate Professor of EE at Illinois State University in Urbana, then with General Electric in Schenectady.

In 1962 CEH, the new joint research laboratory, was founded in Neuchâtel by several organisations representing most of the Swiss watch industry, with a tentative global budget of 5 million Swiss Francs, to be released year after year. The general mission of CEH was to develop new time-keeping devices. This goal was soon refined into that of developing an electronic wristwatch, with at least one advantage with respect to existing watches. No need to say that, at that time, few people could imagine that one of the main advantages would be a much lower production cost for a better precision.

There was no real market pull: most people were happy with the precision of their automatic mechanical watch. Some electrical watches had recently appeared on the market, replacing the mechanical drive by an electromagnetic actuator driven from a small mercury battery through a mechanical switch. A French patent was proposing to replace the switch by a transistor (which was realized a few years later). However, this modest change did not bring much advantage, and those approaches were soon abandoned.

The only really new wristwatch was the Accutron that had been developed for Bulova by Swiss engineer Max Hetzel. Based on a metallic tuning fork oscillating at 360Hz and activated by a single transistor, this revolutionary watch had been commercialized in 1960. It was, however, still essentially mechanical, with a complex wheel-ratchet system driving the set of gears, and at a frequency too low to avoid being affected by gravity.

The electronic quartz clock had already been invented by Warren Marrisson in 1928, and transistorized quartz marine chronometers were just available. Their volume was 1.5dm^3, and their power consumption larger than 100mW. Hence a quartz wristwatch did not have to be invented: it already existed as a system. The "only" challenge was to reduce its volume to less than 3cm^3, and to lower its power consumption by 4 orders of magnitude, down to less than 10μW. This was the maximum acceptable power consumption to ensure more than one year of life for the 1.35V mercury button cell compatible with the wristwatch volume. This new lab was initially lodged just under the roof of the LSRH building in Neuchâtel (Fig. 1). In May 1962, I was the very first electrical engineer hired at CEH by Roger Wellinger.

Fig. 1: LSRH building in Neuchâtel, Switzerland. During its first year, CEH was lodged just under the roof of the main building at the left. It then moved to this wing, where the process line was installed.

A Passion for Electricity

I was born in 1938 in Lausanne. As far as I can remember, I have always been fascinated by electricity. My grandfather was an electrical engineer working for a local power company. His cellar was a cave of treasures, full of various discarded electricity counters. Back home, I used to take them apart, collecting the various parts. Most interesting was the sub-millimeter isolated copper wire of the coils. When I was about six years old, my first applications for it were 220V in-house electrical networks. To connect the meccano-made switches and light bulbs, I just had to scratch the isolation at the wire end with my teeth, bend it, and put it into the power plug. I learned the hard way the meaning of closing an electrical loop when I put my hands both sides of the switch! Nobody seemed to be really worried by the number of shocks I received during this early learning period. However, my father (also an engineer, but in civil engineering) finally decided that I should go to low voltage and he mounted an old radio transformer in a wooden box with just the 6.3V for filament heating available from outside.

My education was in classical literature, with the threat of "descending" to scientific if my results were not good enough (so was the hierarchy of matters at that time!). But I lost no opportunity to communicate my passion to my classmates. When their presentations to the class were about poets and musicians, mine were about electronic recording and electrical transformers (with a demo based on a self-made high-voltage transformer driven by a 4.5V battery chopped by an electric doorbell!). Applications of Ohm's law were the subject of a summer technical contest for which I built a series of demonstrators.

My interest soon concentrated on electronics, which at that time was almost synonymous to radio. At 14, I had built from scratch my first short-wave receiver, winding the thousands of turns of the 2x350V high voltage and manually sawing and bending the aluminium plates to mount the components. I passed my ham radio license at 18 and came "on the air" with a self-made transmitter, with an output power of 10W delivered by a Telefunken RL12P35 power tube (Fig. 2 shows a later version of my station). This was my first contact with the USA and an excellent opportunity to start practicing my school English. I still feel the excitement of waiting for an "opening" of the 10 meters band to contact American or Australian stations as if they were next door! With the Internet, the excitement of distant communication is lost nowadays, but at that time it was achieved with nothing more than my homemade rig.

I received my technical education from the "Ecole Polytechnique de l'Université de Lausanne" (EPUL, that later became EPFL, the Swiss Federal Institute of Technology), where the only professor of electronics was Roger Dessoulavy. I watched him as a god until I could finally attend his courses, during the 4th and last year. Most of the course was based on the vacuum tube, with just two sessions devoted to the transistor. Upon my request, my diploma project was part of a transistorized A/D converter. I then spent one year as a research assistant, working in the ancient gardener's house of EPUL and helping to speed up this converter to audio frequencies. That's where Wellinger found me and asked me to join his new team. We moved to Neuchâtel with my young wife Monique. She was going to provide me with an essential support all along my career.

Fig. 2: At my homemade ham radio station HB9VZ in 1959.

Initial Research Period

My very first task was to demonstrate that a quartz clock could be operated with the power consumption compatible with a wristwatch. I delivered a demonstrator (Fig. 3) that combined an oscillator circuit with a 10kHz commercial quartz, followed by 4 divide-by-ten stages, in order to reduce the frequency down to 1Hz. These dividers were synchronized astable multivibrators using 2N1711 planar bipolar transistors produced by SGS that exhibited a large current gain much below the microampere level. All of the electronics was consuming less than 10µA at 1.5V. But the display was a commercially available electric clock using a stepping motor and consuming more than 1mW. With this simple demonstrator on the table, Roger Wellinger had his 1.8 million franc budget for 1963 accepted by the board of directors. The real work could start, but experienced engineers were needed.

Roger was a very enthusiastic and visionary manager. Using all possible means, he was able to con-

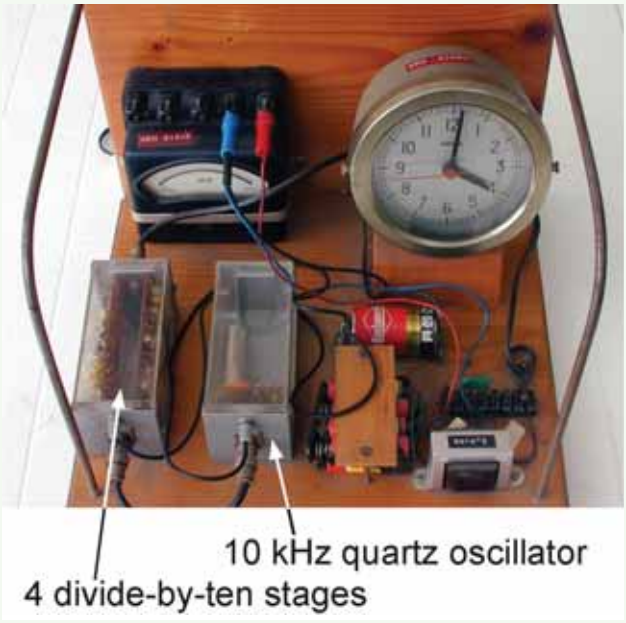

Fig. 3: Microwatt clock demonstrator.

vince a bunch of talented Swiss engineers emigrated in the USA to abandon their interesting and promising jobs to come back to Switzerland and bring their experience to CEH. Among them, Max Forrer left General Electric in Palo Alto to lead the circuit and system section (he became my direct boss for the next 27 years!), and Kurt Hübner came to lead the microelectronic section with his 5-year experience at the Shockley Semiconductor Lab. The real work then started on four parallel paths.

Most essential was the building-up of an in-house IC facility, and the development of a process adapted to low voltage and very low power. Although the first functional MOS transistors had already been published, it was decided to start concentrating on the more traditional bipolar process. A fully operational facility, including a mask shop, was installed in the west wing of the LSRH building (Fig. 1).

The second activity was the search for an adequate time base. The goal was to obtain a precision better than 10ppm (corresponding roughly to 1 second per day) at a frequency lower than 10kHz, to limit the power needed for frequency division. The size of existing quartz resonators at this frequency was much too large, and experts in the field pretended that there was no way to reduce it without drastically reducing the quality factor. Hence we first searched for various types of metallic resonators combined with piezoelectric or electromagnetic transducers. We even evaluated a statistical time base using alpha particles emitted by a radioactive source.

But none of these approaches ended successfully. It is the merit of Armin Frei, another Swiss engineer repatriated from the USA, to have attacked and solved the problem of reducing the size of a sub-10kHz

Fig. 4: First prototype of 8192Hz small size quartz resonator developed at CEH.

quartz resonator. Against all odds and predictions, he was finally able to mount a miniaturized 8192Hz quartz oscillating in flexural mode in the vacuum of a small metallic package (Fig. 4).

The third activity was a search for an adequate display system. The LCD did not exist yet and the LED had just been demonstrated. It was decided to rely on electromechanical solutions, by taking advantage of the matchmakers' skills in micromechanics. Various schemes were evaluated, using electromagnetic and piezoelectric actuators. Two electromagnetic solutions were finally retained for the first prototypes.

The fourth activity was in electronics, essentially evaluating different frequency division techniques. I was mostly involved in this development; hence, I can describe it with more details.

The planar technology was very novel, only able to combine just a few components per chip. The rate at which this number could be increased was uncertain. No low-power process was available yet, and we did not discard the possibility to build the first watch by using discrete components. Therefore, our first aim was to minimize the number of components, and we started by looking into all kinds of analog division techniques.

One possibility was to use synchronized relaxation oscillators (Fig 5a). I tried various schemes, including one based on the tunnel diode (that was considered a very promising device at that time). Another scheme consisted in the step-by-step accumulation of some quantity until a threshold would be reached (Fig. 5b). I first tried to accumulate magnetic flux in a tiny toroidal magnet (of the kind used for computer memories at that time), but the energy per cycle was too high. A better solution was to accumulate a charge in a capacitor, in a kind of switched capacitor integrator, combined with a discharge circuit made of complementary BJT's. A hybrid version of a single divide-by-eight stage mounted in a TO5 package was presented at the 1964 International Congress of Chronometry

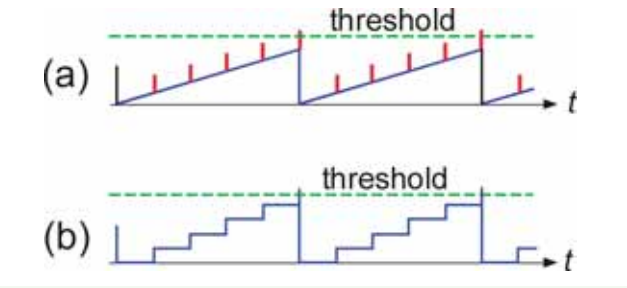

Fig. 5: Analog frequency division techniques; (a) Relaxation oscillator synchronized by pulses; (b) Step by step accumulation.

(where CEH was asked to be present, although we were normally supposed to keep our results secret!).

It is during this period that I made my first visit to the USA, to attend the ISSCC'64 that was still held in Philadelphia. During an evening panel on "Minimum power solid-state devices and circuits", I was asked by a friend of Wellinger to say a few words about our work for an electronic watch. As I can remember, this idea was considered foolish, if not impossible! This trip was also a fantastic opportunity to visit a number of companies and universities and to meet personalities whose famous names were associated with the incipient semiconductor technology.

Analog solutions were indeed limiting the number of components, but the maximum possible dividing ratio was limited by the precision of these components. No more than a factor ten per stage could be expected, even less with the intended integrated versions. So I looked for an analog solution that could provide a very large divider ratio even with low-precision components. This was based on a phaselock loop as illustrated by Fig. 6.

The loop was made of a low frequency VCO (astable multivibrator) followed by a pulse shaper, the output *p* of which sampled the high frequency input. The result

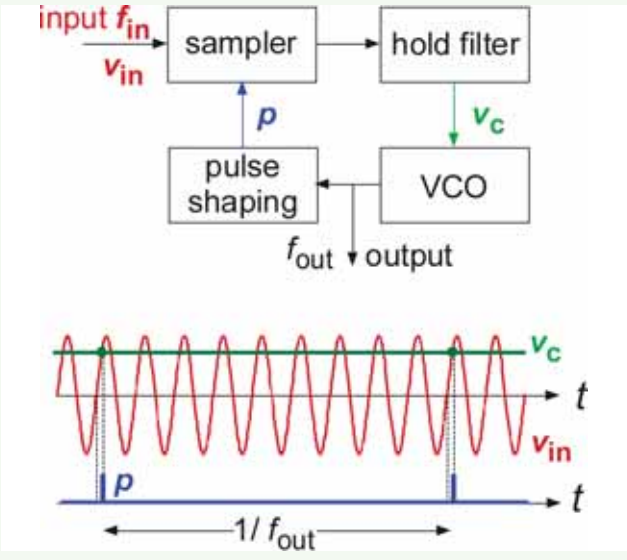

Fig. 6: Principle of phaselock loop frequency division.

was held by a second order filter that produced the voltage v_c controlling the VCO frequency. The phase of the VCO could be locked to that of the input signal for any frequency ratio $N = f_{in} / f_{out}$ that was keeping f_{out} inside the hold range of the loop. The divider ratio was controlled by the initial condition imposed to the loop (and stored in its filter). The hold range could be made large enough to compensate for even a large error in the natural frequency of the VCO. The maximum possible ratio *N* was limited by the jitter of the VCO. Indeed, this jitter was producing a phase noise proportional to *N*, thus a probability of unlocking increasing with *N*.

A breadboard implementation of this divider (which became the subject of my Ph.D. thesis) is shown in Fig. 7. Without the oscillator, this divider contained only 3 bipolar transistors, 4 discrete MOS transistors fabricated at CEH and a few resistors and capacitors. A frequency ratio as high as 1000 could be obtained by means of just a few low-precision components. Consuming a few microamperes at 1.35V, it stayed in lock during the year needed to write my dissertation. This project was a lot of fun. It was an opportunity to learn about nonlinear and discrete-time systems, and it made me love the subject of PLL. But the reliability was definitely not sufficient (risk of loosing the ratio) to consider a mass production of watches based on this approach. Fortunately, in the meantime, our in-house process developments were sufficiently advanced to consider using a cascade of integrated binary dividers instead.

Fig. 7: Experimental phaselock loop frequency divider. It includes a 8kHz oscillator based on an early quartz prototype.

The first binary divider that we developed in 1966 (Fig. 8) was a modified version of a circuit found in the literature, itself a transistor implementation of the T-Flip-Flop used with vacuum tubes. The idea of current mirrors had not been proposed yet, and neither was the implementation of lateral pnp's (although both ideas seem so obvious *a posteriori*, like so many great ideas!). Hence, high-value resistors were the only available way to reduce the power. They were implemented by using the base layer, pinched between emitter E and collector C. Their maximum frequency of operation was thus limited by a large distributed capacitor and could be maximized by letting the E and C layers unconnected (floating). Implemented with our 10

micron bipolar process, this divider could operate up to 5kHz for a current drain of 1µA.

Circuit simulators did not exist yet, so circuits had to be verified on a breadboard before integration. All parasitic capacitors were extracted manually from the layout,

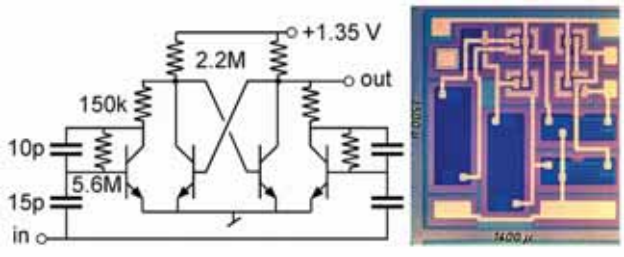

Fig. 8: First binary frequency divider.

but these were of course smaller than those associated with the breadboard itself. To circumvent this problem, the value of all extracted capacitors was multiplied by a large factor (typically 1000), whereas the frequency was reduced by the same factor. The dynamic behaviour of the integrated version could then be predicted with good precision. We used this simulation technique during many subsequent years, until circuit simulators and transistor models at very low current were finally available.

It is this integrated frequency divider that was used in the first prototypes of the electronic watch.

The First Quartz Wristwatch[1]

The efforts of the various groups at CEH came to convergence with the realization of two different prototypes of the quartz wristwatch (Fig. 9). Both used the 8192Hz quartz cantilever developed by Armin Frei, driven by a symmetrical negative resistance circuit. Prototype Beta 1 needed 13 stages of binary division followed by some logic to drive the moving coil of a 1Hz stepping motor. In order to reduce the power consumption, prototype Beta 2 had only 5 stages of division. The 256Hz output was driving an electromagnetic resonant motor, with a ratchet driving the train of wheels. In 1967, ten of these prototypes were presented at the Neuchâtel Chronometry Observatory where they pulverized all previous results. They were then disclosed to our unsuspecting shareholders in a memorable technical seminar.

The industrial production was organized by CEH in collaboration with several interested watch companies. It was decided to start from the Beta 2 prototype

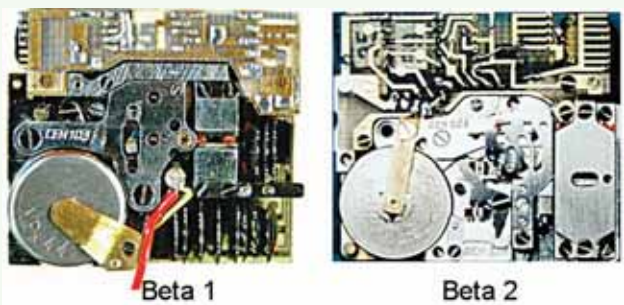

Fig. 9: First prototypes of quartz wristwatch developed by CEH.

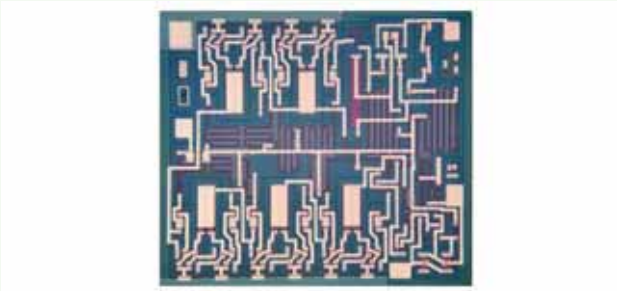

Fig. 10: First LSI circuit developed for a wristwatch.

to ensure a battery life longer than one year. All the circuitry was integrated on a single chip, under the responsibility of Raymond Guye. This very first large scale integration circuit for a watch (Fig. 10) combined 110 components (NPN transistors, high-value diffused resistors and junction capacitors) in an area of 8.7mm^2, and was consuming 12µA at 1.3V. Several other modifications of the watch prototype were introduced to realize the industrial version (Fig. 11) that was named Beta 21. An electronic module was supporting the quartz (not visible in the picture), the plastic encapsulated chip, and an adjustable trimmer capacitor for fine frequency adjustment. The latter became the source of many problems and would have to be eliminated in the future. The components were fabricated by several Swiss companies, but the circuit was produced by CEH in the IC facilities of its microelectronic division. A total of about 6000 units were delivered, and sold under different Swiss trade names.

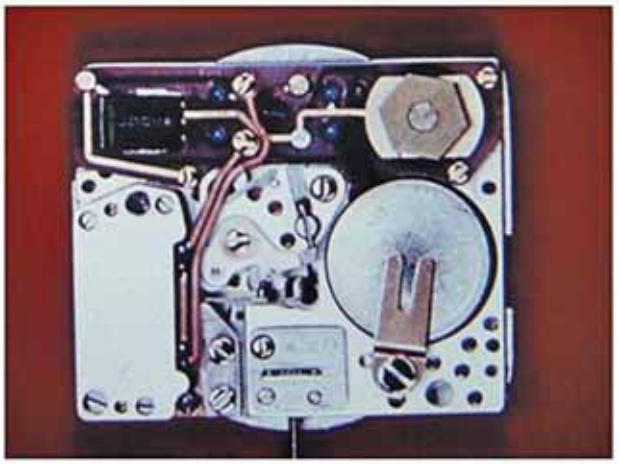

Fig. 11: Beta 21, module of the first commercial watch developed at CEH.

I personally made very few direct contributions to the development of this first industrial product. Indeed, since 1967, and in parallel with the drafting of my Ph.D. dissertation, I was involved in the very early development of low-voltage CMOS circuits.

Pioneering Low-Voltage CMOS Circuits

While most CEH collaborators were busy working on the first watch prototypes, Fritz Leuenberger was

developing a low-voltage CMOS process. Fritz had joined CEH after working in the semiconductor department of General Electric in Syracuse. Following the key paper of Wanlass and Sah at ISSCC'63[2], and strongly supported by Max Forrer, he started developing low-threshold P-channel devices (a few of them were used in my experimental PLL frequency divider) before working on a low-voltage CMOS process. In 1968, he had assembled a perfectly workable process[3]. The n-well was obtained by chemically etching the p-type silicon substrate and epitaxially refilling it with n-type material. The surface was then smoothed by mechanical polishing. A molybdenum-gold sandwich was used for the gates (and interconnections) to obtain a low threshold voltage for both types of transistors.

I was asked to design a frequency divider in this new process. A circuit based on transmission gates had been presented at ISSCC'67[4], but its topology was not suited to group P and N channel devices in two distinct areas. Instead, I carried out a direct Huffman synthesis of the divide-by-two function. The resulting logic equations were implemented by means of two 2-level gates and two inverters (Fig. 12), requiring a total of 16 transistors (after merging some transistors). I drew the layout, and Fritz successfully fabricated the circuit. We measured a current consumption of 10nA/kHz at 1.35V, about 20 times less than the bipolar dividers used in Beta 21. Since the maximum frequency at this low voltage was still about 200kHz, it became possible to increase the frequency of the oscillator and thereby reduce the size of the quartz resonator. This frequency was later fixed at 32kHz and is still used nowadays in most electronic watches.

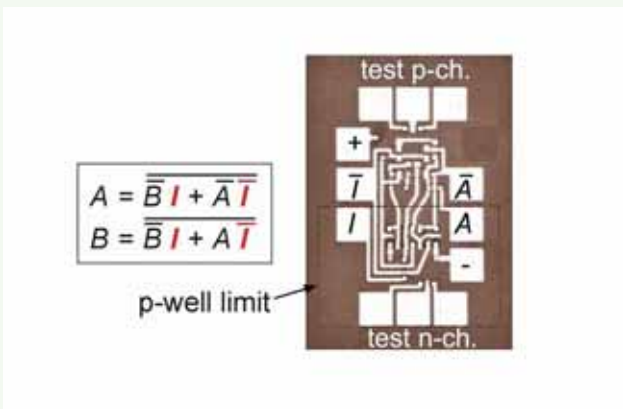

Fig. 12: First low-voltage CMOS frequency divider.

In 1970, Fritz and his team had developed a new CMOS process in which the lightly doped p-well was obtained by solid-to-solid diffusion of boron in a closed capsule. Standard aluminium gates turned out to be sufficient to obtain a threshold voltage of about 1 volt for both types of transistors. Our first CMOS LSI watch circuit was integrated in this new low-voltage process.

This experimental circuit included the first realization of digital frequency tuning. The goal was to eliminate the trimmer capacitor. Instead of adjusting the frequency of the quartz oscillator, the basic idea was to adjust the ratio of the frequency divider. The oscillator could then be optimized for a single frequency, its stability was not degraded by a trimmer capacitor and less precision (but no less stability) was required for the quartz.

We found that the most practical solution was to implement an inhibition circuit between the oscillator and a fixed-ratio divider (Fig. 13)[5]. In this scheme, the frequency of the oscillator is slightly increased, so that its exact value due to spreading is always larger or equal to 2^{15} Hz. Fine-tuning is obtained by eliminating the adequate number of pulses delivered by the oscillator within each adjustment cycle, before they enter the divider. With 20 binary stages, the adjustment cycle was 1/32s and the average frequency could be adjusted to within 1ppm. The inhibit circuit was controlled by a 7-bit word, providing 128 ppm of adjustment range.

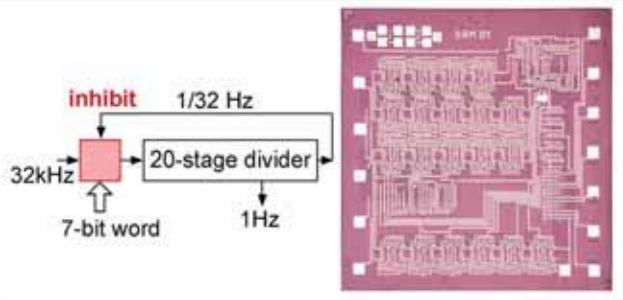

Fig. 13: Principle of digital tuning and its first experimental on-chip implementation.

Of course, the adjustment word must be specific to each device, since it depends on the exact frequency of the oscillator. It must therefore be stored in a memory. The content of the memory must be kept when the battery is changed, but no E^{2}PROM was available at that time. Hence, for this first experimental system called Beta 3, the memory was a set of very simple small switches. But various other solutions were later evaluated, until CMOS compatible E^{2}PROM became finally available.

The whole circuit (that did not yet include the oscillator, because CMOS was still considered too crude to implement analog circuits!) contained approximately 500 transistors. Since no computer aid was available, the layout was drawn with colour pencils on a large sheet of transparent graph paper (on the back side of the paper to avoid removing the frame when erasing for corrections!). The layout scale was 1000:1 for the various blocks and was 200:1 for the overall drawing.

Layout rules had to be carefully respected at each step of the drawing, since remaining errors required the complete erasing of large layout areas.

No computer assisted the mask making either. The first step was to report each mask on a special sandwich of red and white plastic called Rubylith. The red layer was manually cut on a coordinatograph according to the pattern, and manually peeled. Although all divider stages were identical (with only one layout), their cutting and peeling had to be repeated 20 times. Most critical was the mask for the contact holes. For some reason, the Rubylith had to be a negative so that each of the 1000 contact holes (2 per transistor since this was a metal-gate process) corresponded to a 2 by 2 millimeter square of red layer left on the white background. They had a natural tendency to peel away by themselves, so the final control was a real nightmare! But the masks were successfully finalized, and the circuit did work at first silicon, with a current consumption of 0.45µA at 1.5V.

It should be noticed that the chain of divider stages is asynchronous, with the advantage of consuming just a little less than twice the first stage alone. But the timing of the inhibit signal fed back from the end of the divider is totally random with respect to that of the pulses delivered by the oscillator. Therefore, the inhibition circuit was designed to operate properly, independently of the order of transition of these two logic signals. However, this turned out to be insufficient. Indeed, detailed measurements made by the customer of a subsequent implementation showed that the circuit stopped operating correctly just within a very narrow range of temperature (less than 1 degree Celsius). The problem was traced back to the fact that, at this particular temperature, the transitions were exactly simultaneous. This unexpected situation had not been considered in the synthesis of the inhibition circuit, which was later corrected. This example illustrates the difficulty of implementing asynchronous circuits, even simple ones. It also shows the necessity to analyze them in detail, and not only simulate them.

The first industrial application of digital tuning was developed for Complication SA (owner of the Piaget brand), with a special 524kHz resonator developed at CEH by Jean Hermann. Since no non-volatile memory was available yet, it was decided to store the adjustment word in a RAM and to extend it to 14 bit. We had developed a new system, called Beta 4, in which the adjustment was made automatically by the watch. Three pulses separated by exactly one second were injected into the watch by magnetic coupling. This reference was used by the watch circuit to generate the adjustment word. I can still remember the semi-discrete experimental system covering the whole surface of my test bench, including two elementary coils providing the coupling (but I have unfortunately made no photograph).

The final product came to the market in 1975 and included a control box (available at the retailer's place). The watch was placed on this box before pushing a button, and two seconds later its frequency was adjusted within 1ppm. A special very small size battery had been added to keep powering the RAM while the main battery was changed. As technical designers of the systems, we were disappointed to discover that the company never advertised its originality. "You do not want to look inside the belly of a beautiful girl" was their answer!

In the early 70's, we kept working on improving the most basic blocks of the watch, the frequency divider. It was not yet clear whether low-voltage CMOS circuits could be produced in large quantities. Thus, with my colleague Jean Fellrath, we started exploring the possibility to use purely digital binary dividers based on BJT NAND gates. Since the most simple known configurations required 6 gates, I built a specialized computer based on TTL circuits, which was searching all possible configurations of *n* gates for a possibly simpler divider-by-two. The machine found a 4-gate structure that just required the control of a race between two gates[6]. We were trying to implement it by means of the recently published Integrated Injection Logic (I^2L) when the project was abandoned in favour of CMOS solutions. And I later found my "new" circuit in the literature!

Our existing CMOS divider cell was driven by complementary input variables and was therefore sensitive to a possible race between them. With my collaborator Walter Hammer, we decided to search for race-free structures (meaning that no two gates transit simultaneously), with the goal of increasing the robustness of the frequency divider and possibly reducing its power consumption. It also meant that such structures would have a single input (or would be what was later called "single-clock circuits"), and that correct operation would be ensured independently of the relative speed of the various gates.

But at first we had to give a precise definition of a logic gate, the elementary building block of all sequential circuits. We came to the following definition[7]: a logic circuit is a gate if, and only if, it can be modelled by a single-output delay-free combinatorial circuit followed by an inertial delay (that filters out any pulse shorter that the delay value). A gate has therefore no internal memory. A two-level gate can be implemented in CMOS by means of series/parallel combinations of transistors. But it ceases to be a gate if one input is delayed by more than the output delay (such an input delay might be due to a higher threshold value, or to some delay in the input connection). An inverter is of course always a gate, but a cascade of 3 inverters cannot be considered as a single gate.

Using this definition, I carried out a computer synthesis of all race-free divider blocks possible with a

given number of gates. The computer was the IBM 1130 of the University of Neuchâtel that was fed by punched cards. I was coming in the evening with my stack of cards, retrieving the result the next morning. It took me many days until my FORTRAN program was debugged, but finally I got the results, which is still valid to-day: only one 4-gate race-free divider-by-two is possible whereas 9 solutions exist with 5 gates. The best of these 10 possibilities is the 5-gate structure illustrated in Fig. 14.

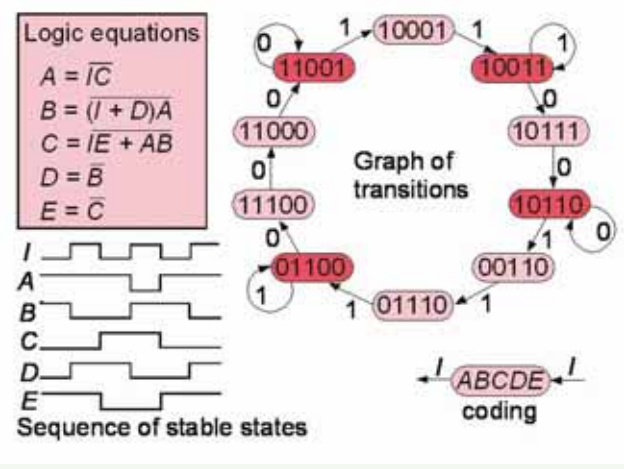

Fig. 14: Race-free divide-by-two cell.

The five gates and their interconnections are defined by the five equations (or rather logic implications). The input variable is *I*, each internal variable *A* to *E* is produced by a gate (*D* and *E* by simple inverters), and the gates are interconnected according to the set of equations. The corresponding graph of transitions shows that no more than one variable tends to transit from any given state; hence there is no race between variables. The sequence of stable states shows that each variable transits at half the input frequency and may thus be used as output of the divider stage. This circuit was integrated experimentally in a 5µm silicon gate process that had been developed in the meantime[8] (Fig. 15). At 1.35V, it was consuming only 1.2nA/kHz, thus about 10 times less than the previous realization. A maximum frequency of 2MHz made it possible to use higher quartz frequencies for special products, such as the Beta 4 mentioned previously. The process itself was running on a pilot line, producing a limited quantity of industrial circuits.

The asynchronous divide-by-two cell is the most elementary non-trivial sequential circuit, and computer synthesis of race-free solutions was not applicable to more complex cells. But our younger colleague Christian Piguet later developed a methodology applicable to various types of cells, including D and JK flip-flops[9].

Returning to 1972, an important contribution was brought by my senior colleague Henri Oguey. After

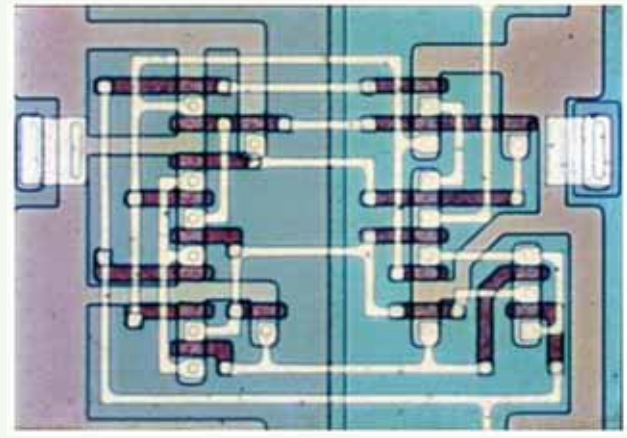

Fig. 15: First integrated race-free frequency divider.

developing display motors, Henri had been very active in the industrialization of Beta 21. Returning to circuit design, he joined our project on new CMOS frequency dividers. He soon pointed out that among all the transistors of a sequential circuit, only some are active to change the output state of each gate, by charging or discharging the output capacitor. The others are just needed to maintain established states against leakage currents. They are therefore not necessary if the frequency is high enough.

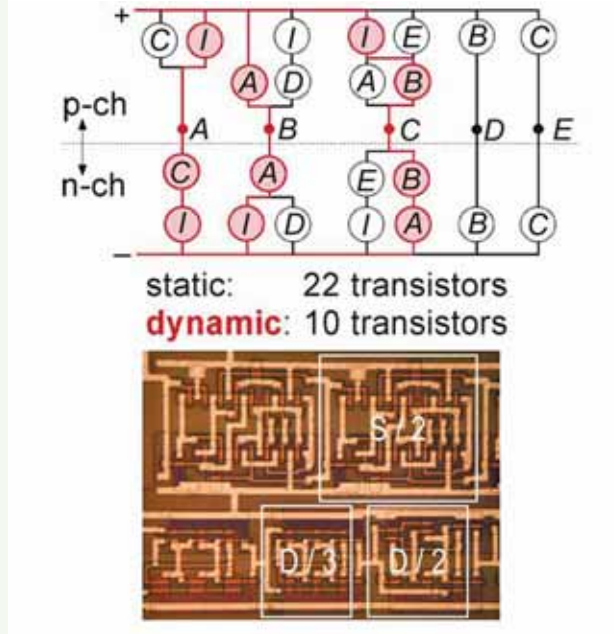

Fig. 16: Transformation of the static circuit of Figure 14 into its dynamic version. Each transistor is represented as a circle, with the name of the variable driving its gate. Only transistors shown in red are needed in the dynamic divider.

I formalized the idea[10] and immediately tried it on my new divider. I pulled the non-necessary transistors out of their sockets in my breadboard simulator.... and the divider kept working. As illustrated in Fig. 16, the

static circuit of 22 transistors was transformed into a dynamic version of only 10 transistors (the inverters were not needed any longer, since the transistors driven by them had been removed). Since the total capacitance to be switched was reduced, the power consumption was reduced by about one half. The photograph shows that the dynamic circuit (D/2) is about half the area of the static version (S/2). A dynamic divide-by-three cell (D/3) proposed by Oguey[11] is also shown.

A semi-dynamic version was also developed by exploiting the fact that the short duration of the input signal could be propagated down to low frequencies by using *A* as output variable driving the next stage. I later carried out a systematic synthesis of race-free dynamic divide-by-*N* blocks up to *N*=6. We then extended the idea of race-free dynamic CMOS to other logic blocks, including D, T and JK flip-flops.

Pioneering Weak Inversion for Analog CMOS

Most of a watch chip area is occupied by digital circuits. But the most critical part, the quartz oscillator, is indeed an analog circuit. To respect the power limitations, transistors had to be biased at unusually low current levels below 1µA. The result of my first measurement of a MOS transistor at very low current is shown in Fig. 17.

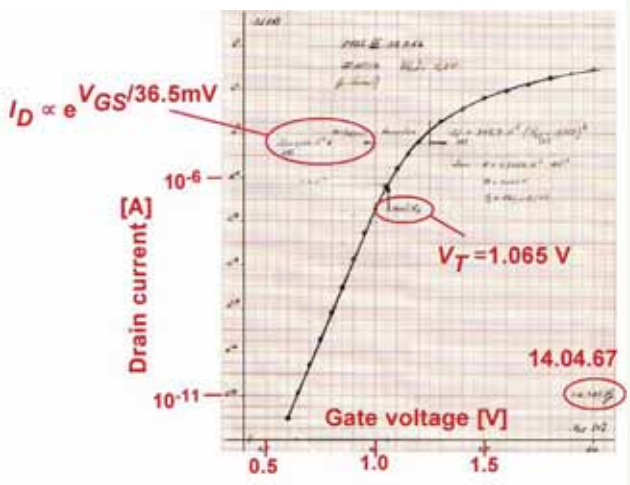

Fig. 17: First measurement of a MOS transistor at very low current (annotated copy of my notebook).

This was in April 1967. The transistor was a P-channel device fabricated in 1966 by Fritz Leuenberger, with a threshold of about 1 volt. I was deeply surprised to discover that, when the gate voltage was reduced below its threshold V_T, the transfer characteristics were nicely exponential across more than 5 decades of drain current. There was no explanation in the literature, since the transistor was always characterized by a square law behaviour. So we painfully started trying to model this strange behaviour. With my colleague Jean Fellrath, we were struck by the similarity with the BJT and very excited by the possibility to implement analog schemes developed for BJT's, but with a device needing no control current.

Jean started with a known current reference (Fig. 18a), in which the size ratio *K* between two N-channel transistors is compensated by the building up of a voltage across a resistor. On this basis, I developed an amplitude-controlled quartz oscillator (Fig. 18b). In this circuit, the oscillation voltage at the gate of the active transistor of the oscillator is filtered out (by a non-critical RC filter) at the gate of the *K*-time larger device, whereas both transistors share the same DC component. As the amplitude of oscillation increases, the bias current delivered to the oscillator decreases, until equilibrium is reached. Later, the resistor shown in green line was added to limit the start-up current, and the oscillator was separated from the regulator for more flexibility. I am still very proud of this circuit that, with these modifications, has become a standard in watch oscillators.

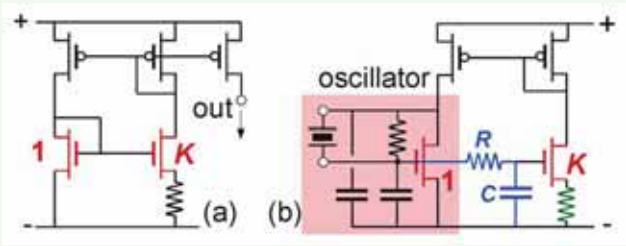

Fig. 18: Analog circuits exploiting weak inversion: (a) Current reference borrowed from BJT design. (b) Amplitude-controlled quartz oscillator.

While we were developing and testing other circuits exploiting these exponential characteristics, several authors were publishing models to describe this "weak inversion" or "sub-threshold" behaviour of MOS transistors (that appears as a DC leakage current in CMOS digital circuits). Most remarkable was the paper by Swanson and Meindl[12]. Indeed, not only did the authors bring important improvements in modelling weak inversion, but they also showed that digital CMOS circuits could operate in weak inversion at a supply voltage as low as 200mV. But the corresponding maximum frequency was so low that the idea was forgotten for the next 30 years!

We put together these various publications, and developed our own simple model that was directly applicable to hand-design (Fig. 19). The width-to-length ratio was originally not included inside current I_{D0}. This current was later decomposed in the EKV model, showing its exponential dependency on the equilibrium threshold voltage V_{T0}. This model includes several features that were kept in later developments leading to the modern EKV model: the source-drain symmetry is preserved by defining the various voltages with respect to the (local) substrate, and a slope factor *n* is introduced to characterize the reduced effect of the gate voltage. It also emphasizes the similarity with BJT's. Indeed, it corresponds to the Ebers-Moll model of a BJT with no base current. But

the MOS transistor is a 4-terminal device, with the gate voltage controlling what would be the specific current of the BJT.

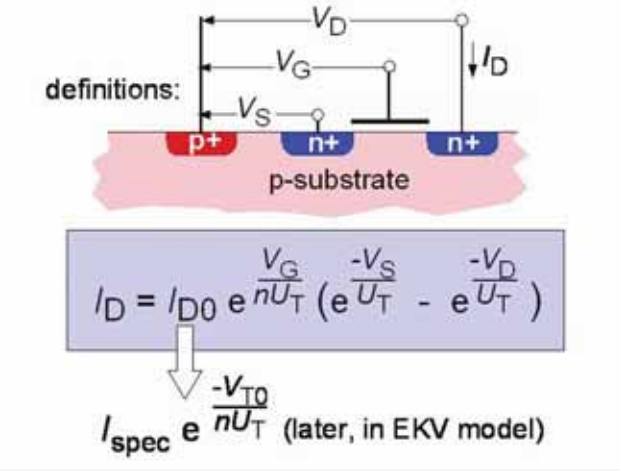

Fig. 19: Model of the MOS transistor in weak inversion. $U_T = kT/q$, n is the slope factor and V_{TO} is a bias-independent threshold voltage.

The model and our various circuits were presented at ESSCIRC'76[13], followed by an extended version in our seminal paper of 1977[14]. I still remember that, after giving the ESSCIRC paper, a comment from the floor did seriously question the reliability of analog circuits based on the "leakage current" of transistors. Of course, weak inversion is not a leakage current. It is a well-controlled mode of operation that is only slightly dependent on process parameters. Circuits operating in weak inversion have since been produced by hundreds of millions for applications in watches.

As already mentioned, all circuits were simulated on a breadboard, after scaling up the values of circuit capacitors to render those of the breadboard negligible. This approach posed a special problem for simulating quartz oscillators, because no electrical circuit could simulate the very high quality factor Q of the resonator. While debugging and optimizing the oscillator of Beta 21, I had developed a special technique to solve this problem. It was based on the fact that with such a high Q, the exchange of energy between the circuit and the resonator can only take place at the fundamental frequency. The nonlinear circuit, including the non-motional part of the quartz resonator, was measured by injecting a sinusoidal current. The resulting voltage was filtered (by means of a band pass filter precisely tuned to the measurement frequency) to obtain the amplitude and phase of its fundamental component. The result was then divided by the value of the injected current to obtain the circuit impedance for the fundamental frequency $Z_{c(1)}$ (Fig. 20).

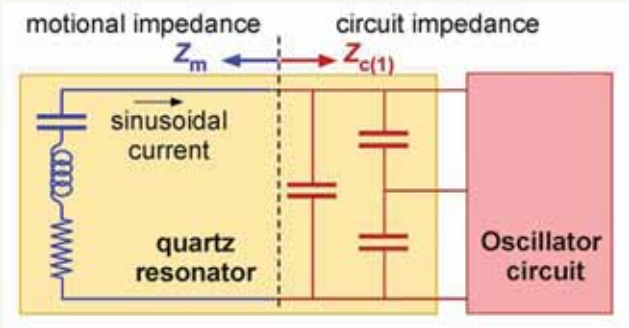

Fig. 20: Splitting of a quartz oscillator for precise simulation of amplitude and frequency. Stable oscillation is obtained for $Z_{c(1)} = Z_m$ [15].

This is a very powerful technique[15], capable of simulating not only the amplitude of oscillation, but also the precise amount by which the circuit is pulling the frequency of oscillation away from the (series) mechanical resonant frequency of the quartz. It is still very useful today, since it can be applied to computer simulation as well. It provides much more insight and precision than the standard lengthy time simulation.

An example of full-blown version of watch oscillator with very low power consumption is illustrated in Fig. 21[16]. This circuit was fabricated in a bi-doped polysilicon process: in order to minimize the threshold voltage of both types of transistor, the polysilicon gate layer was p-type for P-channel transistors, and n-type for N-channel devices. Hence, a lateral diode appeared at each transition inside the polysilicon layer (normally, it had to be short-circuited). The first application of this diode was proposed by Henri Oguey: he used its large leakage current to maintain some logic states in dynamic circuits, in a scheme called resistance-CMOS circuits[17]. In this oscillator, they were used either as floating diodes, or to replace high-value resistors, by using quads of diodes to obtain symmetrical voltage-current characteristics. As a result, no real resistor was needed, and the total current drain was less than 100nA at 32kHz, almost constant for a supply voltage ranging from 0.8 to 3 volts. The regulator itself consumed only 5% of this current.

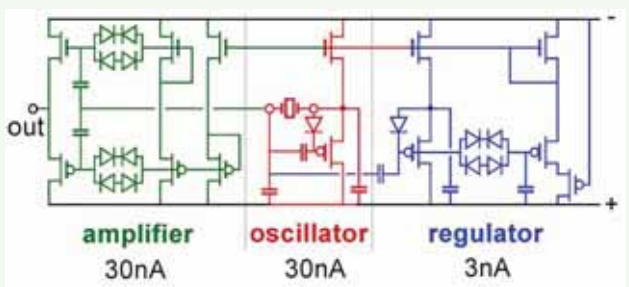

Fig. 21: Full circuit of a quartz oscillator. The regulator has been separated from the core of the oscillator, with an amplifier added to drive the frequency divider.

In 1975, I started the first course on integrated circuit design at EPFL in Lausanne. I specially empha-

sized low-power devices and circuits, thereby initiating a culture that has been pursued and expanded by several of my students. CEH had introduced a multi-circuit chip program (a precursor of multi-project wafers) that was running every three months, so my students could design small circuits and measure them after integration.

Besides the small pilot line of CEH, low-voltage CMOS circuits were produced by Faselec AG in Zurich, and by EM Microelectronic Marin SA, close to Neuchâtel.

Further Developments in Low-Power CMOS Devices and Circuits

The work on most basic circuits for the watch was terminated around 1977, but an important step still had to be made: the watch microprocessor. I must confess that, as the head of CEH circuit design activities, I was not convinced of the real need for such a development. But a workgroup was created, including partners from EPFL, from the University of Neuchâtel and from the watch industry. This group, led by my young collaborators Christian Piguet and Jean-Felix Perotto, started working on the idea of long instructions, to minimize the rate of memory access. This was the beginning of an original series of low-power microprocessors especially designed for watches (see the article by C. Piguet in this issue). The flexibility offered by the approach soon rendered it essential, and nowadays all electronic watches include a special microprocessor.

The watch also needed some auxiliary circuits. Among them was a circuit detecting the end of the battery life. Based on a voltage measurement, it required a precise voltage reference on the CMOS chip. We developed our first band gap reference by combining the base-emitter voltage of the vertical BJT available in CMOS with a PTAT voltage produced by MOS transistors in weak inversion[18]. Another reference imagined by Oguey was again exploiting the bi-doped poly process. It was using the voltage difference of about one band gap between the threshold voltage of two N-channel transistors with opposite types of gate doping[19].

At that time, our low-power CMOS circuit research had been extended much beyond traditional watch circuits, this for two main reasons. One was the need to serve customers outside the watch industry. The other was our dream to introduce many other functions in the watch. Our reasoning was that since the watch occupies a unique position on its owner's arm, it could and should provide several useful functions or services. Many possibilities were proposed: calculator, electronic money, electronic key, communication device, electronic compass, altimeter, personal data storage, and physiological check of the wearer. Even though some of these additional functions have later been introduced in special watches (including a GPS receiver that was not yet conceivable in the mid-seventies), this dream of a multifunctional watch never came to reality. The main technical reason is the difficulty to manually enter information in a small device such as a watch. Not that we did not try: a variety of input devices were developed and tested, essentially based on capacitive sensors implemented on the watch glass. Another reason is that a watch is considered a piece of jewellery rather than a technical device (unlike today's portable phones).

We were given a lot of freedom to explore a wide variety of low-power building blocks. In this framework, our colleague Henri Oguey proved to be particularly creative: his 26 notebooks are a mine of novel ideas, most of them unpublished or even not tested. A good example is the switched current mirror that he imagined in 1977 (Fig. 22). The explanation in French in this figure can be translated into "obtain the same effect as with two perfectly identical transistors". For some obscure reason, we did not apply for a patent, but I was excited by the idea and I made a test circuit in one of our multi-circuit chips. This circuit remained unmeasured (lack of time?) till the mid-80's, when I gave it to my student George Wegmann, as a starting point for his Ph. D. thesis. George made an excellent work, integrating an optimized version, and proving by extensive measurements that such a mirror could reach a precision as good a 0.1%[20]. At the end of 1988, he was ready to publish his results when Daubert *et al.* published the principle that they named a current copier[21].

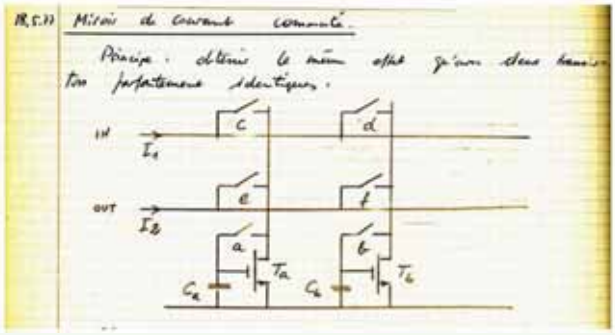

Fig. 22: Excerpt of Oguey's notebook dated May 1977.

Discussions with Henri Oguey were also at the origin of a new scheme for accurate compensation of offset in amplifiers[22]. In this scheme, an offset compensation voltage is stored, not at the main input of the amplifier, but at an auxiliary input of lower sensitivity. The effect of charge injection can thereby be reduced by a large factor.

After the idea of switched capacitor (SC) circuits was first published in 1977[23], we applied it to very low-power circuits. My first realization was a quasi-sinusoidal SC oscillator, intended as a VCO for a tracking filter, and consuming less than 50nA[24]. As I can

remember, the framework was the search for a possible watch-to-watch communication, using a very narrow bandwidth to minimize power. We later developed several versions of low-power SC circuits, in collaboration with EPFL[25, 26]. I demonstrated that operational amplifiers with low output impedance should be replaced by OTA's in order to minimize noise[27]. By operating the transistors in weak inversion, their intrinsic voltage gain was maximum, so that more than 100dB of gain could be obtained in a single cascoded stage (although a cascode is indeed a very special 2-stage configuration). Hence no phase compensation was needed and the architecture of the OTA was very simple. But slew rate limitations were aggravated by the low bias current level, and we had to develop some schemes for class AB operation[28]. The principle of one of our new schemes is illustrated in Fig. 23[29]. The tail current of the input differential pair is increased proportionally to the difference of its two output currents. For a proportionality factor $D \geq 1$, the differential transconductance increases with the input voltage, instead of decreasing to zero as in a normal differential pair ($D=0$).

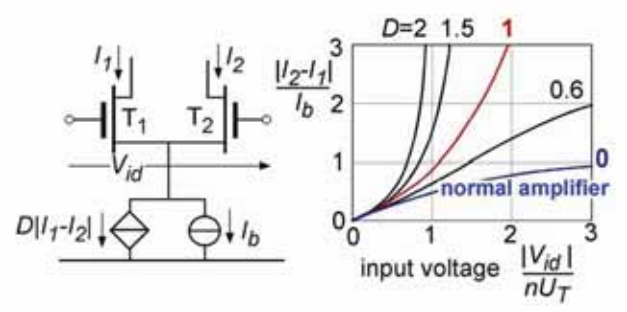

Fig. 23: Principle of a class AB amplifier and transfer characteristics in weak inversion.

At low supply voltage, the problem of charge injection by switches (also called clock feedthrough) was particularly serious. In order to be able to reduce it by a compensation technique, I carried out the first detailed analysis of this important problem. This analysis, based on an equivalent circuit, was originally only presented at a course in Leuven [27] (and also published in an obscure journal). It was later confirmed by other authors[30], and by detailed measurements in the framework of our work on switched mirrors at EPFL[31].

Latch-up was an important problem in the early time of CMOS. We discovered it accidentally, before it had been reported in the literature. My colleague Jean Hermann was developing a new type of quartz resonator, and he wanted to carry out long-term measurements inside an oven. For this purpose, I gave him one of my recently developed oscillator chips, powered by a big 10Ah battery. After a few days, he called me: the oscillator had stopped and the battery was empty. I took the system back to my lab and measured it with a new battery; it was working perfectly, so I send it back to him. This cycle was repeated several times. While I was once more measuring the circuit, the current suddenly jumped by 4 orders of magnitude when I switched on my big oscilloscope. It returned to its microampere level after switching off and on the supply voltage. Although we had stopped designing bipolar circuits, I had always kept an interest in the BJT. So I was quickly able to identify a thyristor effect. A model made it easy to understand what should be done to avoid the problem. Latch-up could easily be eliminated in sub-microampere circuits, such as watch circuits: A minimum latch-up current of about 1mA was guaranteed by applying adequate layout rules, and a 2kΩ poly resistor was placed in series with the 1.5V battery, limiting the maximum current below this value.

My sustained interest for the BJT made me suggest to operate a standard MOS transistor as a lateral BJT (which looks obvious, at least *a posteriori*, given the structural similarity of the two types of devices). After negative results obtained by some collaborators, I was not discouraged and decided to measure it myself. I took care to consider it as a 5-terminal device (the 4 terminals of the MOS transistor in its well, and the substrate), and it worked as expected. My first application was a multiple cascoded current mirror shown in Fig. 24. The same devices could be operated as MOS transistors or as lateral BJT's, to demonstrate the drastic improvement in precision. I also demonstrated a band gap voltage reference and a low-noise amplifier[59]. Figure 25 shows a later measurement of $1/f$ noise, in which the decreasing gate voltage V_G is compensated by a more negative source voltage V_S to maintain the drain current I_D constant (at 1μA). Operation is therefore progressively moved from MOS to BJT, showing a dramatic reduction of flicker noise.

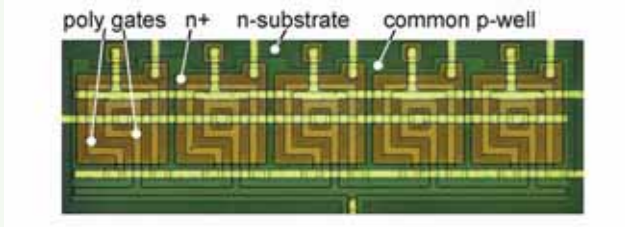

Fig. 24: Multiple cascode current mirror. Each inner concentric device can be configured as a MOS transistor or as a lateral BJT.

Weak inversion provides several advantages that can be exploited in low-power circuits. But this mode of operation also has some drawbacks, the most important being the poor precision of current mirrors. Hence, even in very low-power circuits, the various

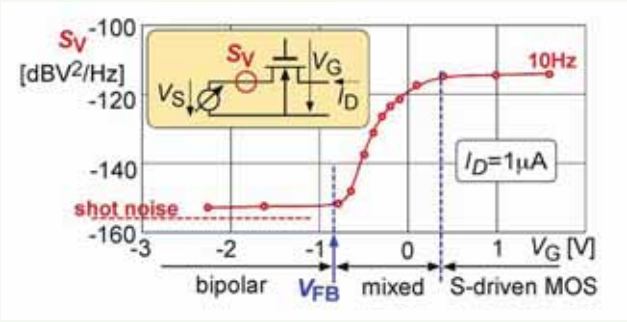

Fig. 25: Flicker noise measurements (from Stephan Cserveny, unpublished).

transistors must usually be biased with various degrees of inversion, depending on their function. This is the reason why we needed a model covering all levels of current, from weak to strong inversion. In collaboration with Stefan Cserveny, Henri Oguey developed a model called CEMOS that was an important step towards our later EKV model. They introduced the notion of control voltage (that became the pinch-off voltage in EKV). They also emphasized the symmetry of the transistor by expressing the drain current as the difference of two values of the same function, one calculated at the source, the other at the drain (these two values became the forward and reverse components of drain current in the EKV model). The function itself was changing smoothly from the exponential of weak inversion to the square law of strong inversion, by means of a mathematical interpolation.

In 1983, the CEH research laboratories were merged into CSEM (a French acronym for Swiss Centre for Electronics and Microtechnology), a newly founded organization partially supported by the Swiss government. During its more than 20 years of existence, CEH had provided a very open research environment with a lot of research freedom. The definition of most of the projects was sufficiently general to allow the researchers to explore new ideas inside wide domains. I like to compare this kind of exploration with the exploration of unknown territories of the World. We were exploring in particular the continent of very low-power circuits (we called them micropower circuits), with no predefined milestones (what are milestones in the exploration of a *terra incognita*?). The cafeteria was always a place of intense technical discussions and exchanges between designers and process specialists. We were given the time and the freedom to generalize our ideas and to conceptualize them (a very important step to progress in research). Of course, there were dead ends, but they often could be transformed into new ideas applicable elsewhere. The lack of computer resources forced us to use analytical approaches, which give much more insight than computed sets of numbers or plots (the computer is of course an invaluable complementary tool, but should not replace the analysis as is does too often nowadays). Overall, this CEH period was a fantastic adventure for all of us.

Low-Power Circuits at EPFL and CSEM

CSEM was more development-oriented, with well-defined specifications to be reached in a well-defined period of time. I moved more of my personal research to EPFL in collaboration with my Ph.D. students.

A very imaginative student, François Krummenacher had independently solved the problem of sensitivity of SC circuits to parasitic capacitors during his Diploma work. He later developed a low-power SC filter approach with intrinsic double correlated sampling to reduce the $1/f$ noise[32], and his Ph.D. thesis was about the optimisation of very low-power SC filters. As a first assistant, he later developed along the years a multiplicity of novel low-power circuits, including continuous-time filters[33].

François also helped me supervise the Ph.D. project of Christian Enz on high-precision CMOS micropower amplifiers. It is in this framework that previous developments of a MOS model at CEH were pursued and extended at EPFL. This new model was later called EKV, after its first publication by the three of us[34]. At this stage, the model was already including the dynamic behaviour and the noise, but it still used the mathematical interpolation from weak to strong inversion proposed by Oguey and Cserveny. The model was then extended year after year with the help of several students, under the leadership of Christian Enz, who had become professor. Christian also started an activity on low-power low-voltage RF CMOS circuits. Transceivers were developed that could operate below 1V of supply voltage by biasing transistors close to or in weak inversion[35, 36]. His team also demonstrated new log domain filters based on the exponential characteristics in weak inversion[37] (see the article by C. Enz in this issue).

Although CSEM was more oriented towards development and industrial projects, we kept several advanced research projects, in particular in low-power integrated circuits. Among them was a project on analog VLSI inspired by biology. The underlying idea was the following. It can be demonstrated that analog remains more power efficient than digital for carrying out tasks requiring no large signal-to-noise ratio[38, 39, 40]. This is the case for tasks of perceptive nature, like vision or audition. Instead, as our brain does, they require a massively parallel system of strongly interconnected cells to carry out collective computation.

Thus, analog VLSI appeared best suited to implement, in particular, low-power image processing systems-on-chip (often called somewhat incorrectly "artificial retinas"). One important problem was (and still is) the density of interconnections that is much lower

on-chip than in the brain. One solution is to implement connections to the neighbouring cells only. This was possible for the motion detection chip shown in Fig. 26, that we developed for a pointing device[41]. This circuit was inspired from the rabbit's eye, and evaluates separately the vertical and horizontal motion components of a pattern of dots.

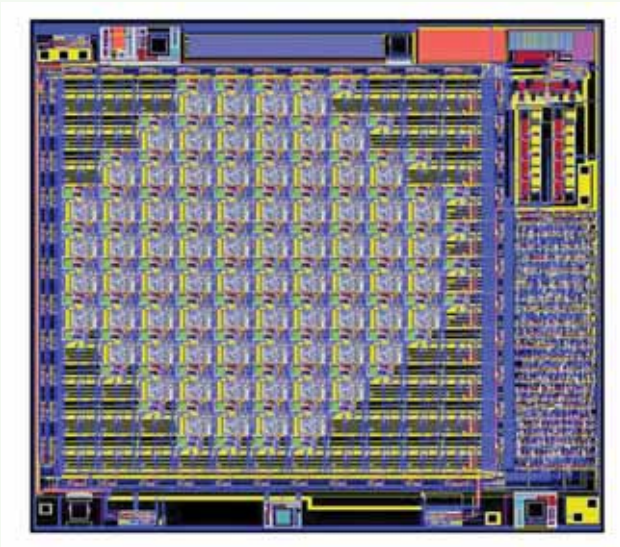

Fig. 26: Layout of a motion detection chip for pointing devices.

For more general communication the solution was to use the scheme called address-coding events (ACE)[42]. According to this scheme, each cell produces very short pulses (called events) that code their position on a common parallel bus. The analog information is carried by the frequency or by the phase of these events (both of them being continuous values). Different solutions may be used to deal with the possible collision of these asynchronous events. At EPFL, we developed our particular scheme that simply eliminates the results of collisions[43]. This scheme was applied recently by CSEM to a remarkable analog vision-sensor chip that computes at the pixel level the contrast magnitude and direction of image features[44]. For each pixel, this pair of analog values is transmitted on two separate buses as the phase of ACE's with respect to a common clock signal.

The whole project in bio-inspired analog VLSI was also intended to force the exploration of totally novel schemes by a kind of lateral thinking. One result was the idea of Oliver Landolt to represent and compute analog data by means of "place coding"[45]. This approach should be explored further, since it combines the advantages of digital and analog circuits: it allows one to increase the computational accuracy (and the immunity to many kinds of perturbations) of analog data by increasing the number of hardware cells.

Another by-product of bio-inspiration was the concept of pseudo-resistors. According to this concept, illustrated by Fig. 27, any network of linear variable resistors can be replaced by a network of MOS transistors in weak inversion if only currents are considered[46]. The value of the pseudo-resistor may be controlled directly by the gate voltage of transistor T, or by the current I_c in an associated control transistor T_c. All transistors are in the same substrate, and all control transistors may share the same voltage V_{ref}. If a node (e.g. node B) is grounded in the resistive network, it corresponds to a saturated transistor in the pseudo-resistive network (side B of T saturated), according to the concept of pseudo-ground.

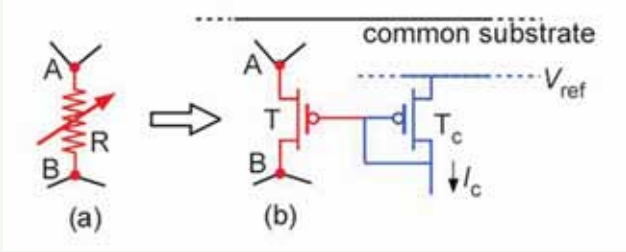

Fig. 27: Equivalent linear networks with respect to current. (a) Resistor R between nodes A and B of a network of variable resistors. (b) Corresponding pseudo-resistor T in weak inversion.

This linearity with respect to currents can be traced back to the fact that diffusion (which is the sole cause of channel current in weak inversion) is a linear process. But the principle is also applicable if the transistors leave weak inversion (the current is then no longer carried only by diffusion), provided all of them share the same gate voltage, as was first demonstrated by Bult and Geelen in 1992[47]. I formalized the concept in 1997[48] while describing a number of possible applications. I am still fascinated by this property of current linearity that was identified only 30 years after the MOS transistor was first used. This property is linked to the fundamental symmetry of the transistor, as expressed by the EKV model. In weak inversion, this symmetry is only progressively affected when the channel is shortened, whereas structural non-homogeneities along the channel also affect it in moderate and strong inversion[49]. But this functional symmetry is otherwise always independent of the shape of the channel.

Low-Power, Low-Voltage Today

All of the essential CMOS watch building blocks that have been developed in the past have been adapted to more recent fabrication processes, and they are still used in modern Swiss watches. They include the oscillator, the frequency divider and the digital tuning with an on-chip E^2PROM. The experience on low-power quartz oscillator circuits is directly applicable to MEM resonators that have the same equivalent cir-

cuit. Special microprocessors have evolved with the increasing complexity of the watch and are present in all modern electronic watches. Special devices such as the bipolar-operated MOS or the lateral diode inside the polysilicon layer are available today in all or some modern sub-micron processes, but they must be characterized before being used.

The modern version of the EKV transistor model is fully charge-based and continuous from weak to strong inversion. It includes second order effects related to submicron processes and is applicable to RF IC design as well as to very low power[50]. Although it has lost the race against the PSP model[51] to become the new standard, it is implemented in many CAD tools[52]. Based on the physical mechanisms underlying the transistor behaviour, it only requires a limited number of parameters that can be predicted from the process, and it maintains the symmetry inherent to the device (which is very useful, if not absolutely necessary, to understand and analyse some analog circuits). It provides a very precise "g_m/I"(transconductance-to-current ratio as a function of the normalized saturation current) relationship that is a very useful tool for optimum analog design. It is also coherent from its simplest form that can be used in understanding and teaching circuits, to its most detailed form applicable in CAD tools.

At the beginning of the 90's, the World has awoken to low power. First because of the increasing importance of portable devices, but also to limit on-chip heat generation and to reduce the cost of power supplies in computers. Indeed, power consumption has been moved high in the list of chip specifications (from which it was previously often simply absent). Moreover, with modern submicron processes, the maximum voltage must be limited to limit electric fields. Hence, low-voltage has also become very important nowadays. Circuit techniques developed along the years for low power and low voltage have therefore gained more importance.

For analog subcircuits, a voltage reduction does not help reducing their power consumption[40]. Worse, and especially below 1V, it tends to increase the minimum power needed to achieve a given speed and a given signal-to-noise ratio. One reason for this is the reduction of maximum voltage amplitude due to the drain to source saturation voltage V_{DSsat} of MOS transistors. The amount of channel inversion must therefore be reduced to reduce V_{DSsat}, which reaches its minimum in weak inversion. As a consequence, in any analog circuit operated below 0.5V, transistors must be biased close to or in weak inversion. This connection of weak inversion with low voltage is more fundamental than that with low current (since transistors can in principle remain in strong inversion even at a very low-current if their length-to-width ratio is increased). The special characteristics in weak inversion permit a variety of low-power, low-voltage analog circuits, including translinear loops, log domain filters and analog processors exploiting the concept of pseudo-resistors[53]. A recent experimental application of the latter is the on-line minimization of the total energy spent by a multiprocessor system-on-chip to execute a set of related tasks[54].

The idea of single-clock digital circuits has been rediscovered after 25 years for application to very high-speed circuits[55]. For digital circuits, power can be reduced by reducing the supply voltage, thereby reducing the energy per transition. The resulting reduction in speed can be compensated by using a smaller feature size and/or by resorting to parallelism[56]. But to maintain a sufficient gate voltage overhead (in order to maintain high speed), the threshold voltage must be reduced. As a result, at zero gate voltage the transistor is no more completely blocked since some non-negligible weak inversion current remains. Often called "DC leakage current", this residual off-state current tends to become an important part of the total power consumption. During its first 30 years of existence, the MOS transistor could be considered as an ideal on-off switch, and CMOS logic was only consuming energy during transitions. The power consumption of idling gates was negligible, thus their percentage did not affect power consumption.

Nowadays, the MOS transistor must be looked at as a *voltage-controlled current modulator*, with a limited on/off current ratio. Since the maximum speed is proportional to the on-current, the off-current and the resulting DC power consumption becomes proportional to the required speed. But this DC power consumed by a gate is also proportional to the idling time of this gate. It can therefore be reduced by increasing the duty factor $\alpha < 1$ of the gates, defined as the ratio between their effective switching frequency f and its maximum possible value f_{max}.

Now, for a given supply voltage (hence a given gate voltage swing), the maximum on/off current ratio is obtained in weak inversion. Thus, as I have shown in a recent analysis[57], CMOS logic circuits in weak inversion can be optimized to reach the ultimate minimum of power P for a given switching frequency and with a given process. This minimum is shown in Fig. 28 together with the corresponding optimum supply voltage V_B. The maximum possible frequency f_{max} can be selected by adjusting the off current according to the model of Fig. 19, by means of the source-substrate voltage V_S. The minimum power depends on the process via the total load capacitance C of the gate (including interconnections). It splits into a dynamic component and a static component.

Compared with 1 Volt operation (for which the static power would be negligible), a power reduction by more than 50 would be possible if a duty factor α =1 could be ensured. But this is only possible with 3-stage

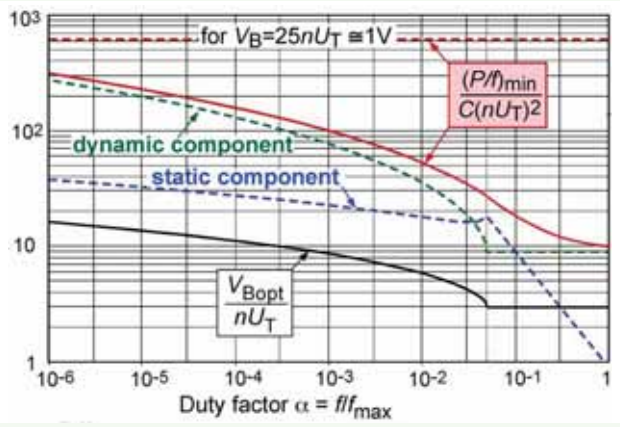

Fig. 28: Minimum power consumption *P* of a CMOS gate operated in weak inversion (red curve) for an average frequency *f* of on/off transition cycles (not to confuse with the clock frequency). Corresponding optimum supply voltage V_B (black curve).

ring oscillators (that are not very useful circuits). For a more realistic value α =1/100, the reduction can still be more than a factor 10, with a maximum possible switching frequency of about 3MHz for a 0.18 micron process (which would reach 500MHz for α=1).

This ultimate limit assumes that the off-currents of p- and n-channel transistors are adjusted to the same value (by adjusting the source-substrate voltage, which requires a true twin well process). It might not be reached in practice due to several side effects like mismatch or drain induced barrier lowering. The new century has seen the emergence of a new interest for weak inversion logic (now called subthreshold logic) with the realization of digital sub-systems operating at a clock frequency of a few kHz and a supply voltage of just a few hundred millivolts[58] (see article by J. Kwong and A. Chandrakasan in this issue). There is no doubt that further research in this direction (and further process scaling) will permit an increase in system speed. But, at ambient temperature, it will never be possible to decrease the supply voltage much lower (the absolute minimum for regenerative logic being $2\ln(n+1)\cdot U_T$). It is interesting to point out that these voltage levels are comparable to that of the action potential in the brain.

The human brain is a fantastic computing machine. With its 10^{11} neurons (or 10^{12} cells if we include the supporting glial cells), it consumes about the same power as a fast modern microprocessor. But its processing power is immensely larger. It must therefore use much more energy efficient computation strategies. Some of them are known. A massive parallelism compensates for the much lower speed of each neuron (maximum firing rate of about 2kHz). But it also makes possible the spatio-temporal representation and processing of information, by means of arrays of cells organized in maps. The system may be seen as digital, since it uses short pulses of fixed shape and amplitude (called the action potential) to carry the signal. But it is essentially analog since the information is carried by the frequency and by the phase of these pulses. Its program and data memory is distributed and is stored in the pattern of interconnections and in their variable strengths (synaptic weights). Its learning capability has inspired the approach of artificial neural networks (with interesting but limited results, due probably to an inadequate adaptation to the silicon environment). But what is known today is certainly a very small part of all the unusual schemes exploited by the brain, and new ones are being uncovered by very active teams of neurophysiologists.

Reducing the power consumption of processing chips while increasing their complexity will be possible by further developing traditional techniques, at all levels from process to software. But there will be limits, beyond which totally new approaches will be needed. Why not then try to borrow some of the schemes used by the brain, thereby harvesting the results of half a billion years of evolution? Undoubtedly, these schemes will have to be cleverly adapted to the constraints and possibilities of the silicon environment. But this adaptation will only be possible if a sufficient number of open-minded deciders in the industry and in universities organize a close collaboration of their most inventive circuit designers with the community of brain researchers.

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A Short Story of the EKV MOS Transistor Model

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I. THE EKV MOS TRANSISTOR MODEL

A. The Early Stage

The EKV MOS transistor model finds its roots in the first transistor models accounting for weak inversion that started to be published in the 70's. In 1972, M.B. Barron published a model for the grounded source device showing the exponential dependencies on drain voltage and on surface potential, with a rather complex expression relating the surface potential to the gate voltage [1]. The same year, R.M. Swanson and J.D. Meindl [2] showed that this relation could be accounted for by means of an almost constant factor, which became the slope factor n used in the EKV model. The following year, R.R. Troutman and S.N. Chakravarti [3] treated the case of non zero source voltage. Then T. Mashuhara et al. [4] showed that the current depends on a difference of exponential functions of source and drain voltages.

In the mean time, micropower analog circuit blocks were developed at the Centre Electronique Horloger (CEH)[1]. They were first published in 1976 [5], [6], together with a model applicable for weak inversion circuit design, which was based on the previously mentioned work. This model already included two important features of the EKV model: a) reference to the (local) substrate (and not to the source) for all voltages and b) full source-drain symmetry. The related small-signal model including noise was also presented [7]. A symmetrical model of the MOS transistor in strong inversion was first published by P. Jespers in 1977 [8], [9]. Based on an idea of O. Memelink, this graphical model uses the approximately linear relationship between the local mobile charge density and the local "non-equilibrium" voltage in the channel. This charge-based approach has been adopted and generalized to all levels of current in the EKV model.

Another ingredient of EKV is the representation of the drain current as the difference between a forward and a reverse component. This idea was first introduced for the MOST in 1979 by J.-D. Châtelain [10], by similarity with the Ebers-Moll model of bipolar transistors [11]. However, his definition of these two components was different from that adopted later, and was not applicable to weak inversion.

Even in micropower analog circuits, not all transistors should be biased in weak inversion. There was therefore a need for a good model continuous from weak to strong inversion. Such a model was developed at CEH by H. Oguey and S. Cserveny, and was first published in French in 1982 [12]. The only publication in English was at a summer course given in 1983 [13]. This model embodied most of the basic features that were retained later. It introduced a function of the gate voltage called control voltage, later renamed pinch-off voltage V_p. A single function of this control voltage and of either the source voltage or the drain voltage defined two components of the drain current (which became the forward and reverse components). This function was continuous from weak to strong inversion, using a mathematical interpolation to best fit moderate inversion. In the mid-80's, the model of Oguey and Cserveny was simplified by E. Vittoz for his undergraduate teaching at EPFL.

B. The Continuous Model Stage

I started to work on the EKV model as part of my Ph.D. thesis supervised by E. Vittoz. Although my Ph.D. work was on the design of a micropower low-noise amplifier, I quickly realized that I needed a better model to design my amplifier, particularly including the noise not only in weak inversion but also in moderate and strong inversion. In collaboration with E. Vittoz and F. Krummenacher, we developed the premises of what would become the EKV model on top of the original work done at CEH by H. Oguey and S. Cserveny. The model was formulated more explicitly. Noise and dynamic behavior were introduced by exploiting the fundamental source-drain symmetry. The pinch-off voltage, initially defined as the control voltage by H. Oguey and S. Cserveny only in strong inversion, was extended to the weak inversion region. The status of the model was presented at various Summer Courses [14] -[16], but curiously was never published. It was only after I joined the Electronics Lab of EPFL headed by M. Declercq as an Assistant Professor in 1992 that I realized that our model was actually never published. Together with F. Krummenacher and E. Vittoz, we decided to publish a full paper on the EKV model in 1995 [17] in a special issue of the AICSP on low-power circuit design. This publication gave its name to the model, but many important extensions were added later.

Probably the most important extension was the replacement of the current and transconductance purely mathematical interpolation functions between weak and strong inversion presented in [17] by a more physical one, derived from an explicit linearization of the inversion charge versus the surface poten-

[1] For more details about the Centre Electronique Horloger (CEH) and its history, please read the article of E. Vittoz on page 7 in this issue.

tial. The incremental linear relationship between inversion charge and surface potential was first considered by M. Bagheri and C. Turchetti [18], but the linearization of the inversion charge versus surface potential was originally proposed in 1987 by the pioneering work of M. Maher and C. Mead [19], [20]. At that time we did not realize that most of the charge-based formulation, including the effect of velocity saturation, was already present in the model of M. Maher and C. Mead. Strangely, this work was only published in the proceedings of a local workshop [19] and in the Appendix of a book by C. Mead [20]. Clearly it did not receive the recognition it actually deserved.

Several years later, different groups looked at this problem of inversion charge linearization. B. Iñiguez and E.G. Moreno [21], [22] derived an approximate explicit relation between inversion charges and surface potential which included a fitting parameter. While their first linearization was done at the source [21], they later obtained a substrate referenced model [22] based on the original EKV MOSFET model approach [17], that also included some short-channel effects. A similar approach was also proposed by A.I.A. Cunha et al. [23] - [26] who obtained an interpolate expression of the charges versus the potentials that used the basic EKV model definitions [17]. We also adopted the inversion charge linearization approach, since it offers physical expressions for both the transconductance-to-current ratio and the current that are valid from weak to strong inversion [27]-[30]. This gave rise to the charge-based formulation of the EKV model which was the basis of the compact model that was then extended and coded by my Ph.D. student M. Bucher. The inversion charge linearization principle was rediscovered once more in 2001 by H.K. Gummel and K. Singhal [31], [32]. Finally, a formal detailed analysis of the inversion charge linearization process and a rigorous derivation of the EKV model was finally published by J-M. Sallese et al. in [33]. Note that this approach actually provides voltages versus currents expressions that cannot be explicitly inverted. It can nevertheless be easily inverted by using a straightforward Newton-Raphson technique or by an appropriate approximation. Both these techniques have been used in the final model implementation.

C. The Compact Model Stage

The basic long-channel charge-based EKV model was further developed by my Ph.D. students and by members of the team of researchers to include the following additional effects:

- Non-uniform doping in the vertical direction was proposed by C. Lallement et al. in [34], [35].
- A small-signal charge-based *non-quasi-static* (NQS) model was presented by J-M. Sallese and A-S. Porret in [30], [36].
- *Polysilicon depletion and quantum effects* were also added [37]-[39].
- I extended the EKV model to also cover *high-frequency operation* for the design of RF CMOS integrated circuits [40]-[44].
- An accurate model of the extrinsic capacitances was developed by F. Prégaldiny et al. [45].
- A compact model cannot be used without an efficient *parameter extraction* methodology. The EKV model uses an original parameter extraction methodology presented in [46]-[49].
- An accurate *thermal noise* model accounting for short-channel effects was developed by A. S. Roy [50]-[52]. He also looked at the *flicker noise* model and revisited some of the fundamental concepts showing the equivalence of different noise modeling approaches. More importantly, he rigorously analyzed the effects of a longitudinal nonuniform doping in the channel and the dependence of the mobility on the longitudinal field.

Most of these developments plus some other aspects were included in the book Eric and I recently wrote, giving a complete overview of the EKV MOS transistor modeling approach [53]. But the EKV really became to be known because it could be used by circuit designers for the design of low-power circuits. This was made possible thanks to the hard work of M. Bucher who coded the EKV model and carefully implemented it in many circuit simulation tools. Thanks to its single piece continuous formulation it ran efficiently avoiding many convergence problems. The EKV model version 2.6, implemented by M. Bucher was used by designers for many years and is still used today.

A few years ago, it was recognized that threshold-based models (such as BSIM 3) were showing their limits when moving towards deep-submicron technologies and new generation models were needed [54]. An open call was launched in 2005 by the Compact Modeling Council (CMC)[2] for the next generation models and version 3.0 of the EKV model that included many of the recent developments [56] was one of the challengers. From the more than 20 models that were initially submitted, only 5 were selected after the first round, and EKV 3.0 was one of them. The CMC finally chose the PSP model to be the new industry standard for deep-submicron processes [57]. The PSP model started as the merge of two surface potential models: SP (developed at Pennsylvania State University by the team of G. Gildenblat) and MM11 (developed by Philips Research) and continued as a joint development.

More recently, the research of the EKV team at EPFL has been more oriented towards the modeling

[2] The Compact Modeling Council is an organization made of industrial and academic members promoting standardization in the use and implementation of compact models [55].

of multi-gate MOS devices and more particularly on double-gate devices [58], [59].

II. THE EKV DESIGN METHODOLOGY

One of the main features of the EKV model compared to others is the small number of parameters that it requires. This obviously simplifies the model and its implementation, but also the parameter extraction. Another feature, more important to my eyes, is its hierarchical structure: indeed the complete compact model can easily be reduced to the simple hand calculation model by setting some parameters to specific values. This allows for a step-by-step approach in the design of new circuits, starting with the simplest model coherent with the model used for hand calculation and progressively adding effects in order to evaluate their impact on the circuit performance. Actually, the EKV MOS transistor model was initially not developed with the aim of having a compact model for circuit simulation, but rather for having a simple hand calculation model that can help designing and sizing circuits that are biased in all modes of operation including strong and weak inversion but also the region in between called the moderate inversion. The available models at that time were simplistic square-law models that were often inaccurate in strong inversion and totally wrong in moderate and weak inversion. The EKV MOS transistor model introduced the powerful concept of inversion factor (also called inversion coefficient IC) as the main transistor design parameter that is more general and replaces the long-time used overdrive voltage, distinctive of strong inversion models, but meaningless in weak inversion. For more than 25 years, E. Vittoz and I have been teaching analog circuit design based on the use of this concept of inversion factor. This approach allows for expressing all the important parameters of a single transistor biased in saturation, such as small-signal parameters, including transconductances and capacitances, noise parameters, versus a single parameter: the inversion factor. Sweeping the inversion factor allows exploring all the design space for a single transistor. In 1996, I created a first sizing tool actually called Analog Designer and running on a Mac. The GUI is shown in the Fig. 1, below. It allowed calculating all the important design parameters from the inversion factor, corresponding to the top axes in the figure. Then all the other parameters were updated simultaneously when sweeping the first vertical bar. The designer, hence, could then optimize the operating point most appropriate for the particular task of the single transistor to be sized.

EKV design methodology was extended by D. M. Binkley beyond what was initially created, looking at all the different design cases that may be faced. For example, he extended the definition of the inversion

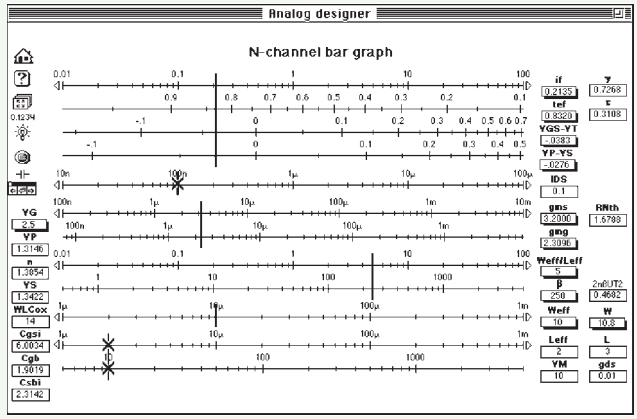

Fig. 1. The Analog Designer tool illustrating the basics of the design methodology based on the inversion coefficient [61].

factor to include important effects such as velocity saturation and mobility reduction due to the vertical field, allowing for a more accurate design for short-channel devices at high inversion factors. Drain induced barrier lowering (DIBL) is also included in the calculation of the voltage gain, since it often dominates the channel length modulation (CLM) effect at short transistor length and low inversion factors. D. M. Binkley recently published a book on his work making it the first true reference on the original EKV design methodology and the many extensions he developed [60].

III. LOW-POWER CIRCUIT DESIGN

The EKV MOS transistor model and the related design methodology has been taught for many years and has been used by many designers for the design of low-power circuits. Many circuits that were developped by E. Vittoz, F. Krummenacher, our Ph.D. students and myself, have in one way or another used and improved the methodology.

I started to use the EKV design methodology immediately after my Ph.D., when, together with F. Krummenacher (the "K" of EKV) we founded Smart Silicon Systems in 1989. We were working together with Erik Heijne and other teams at CERN developing several CMOS strip and pixel detector front-end read-out chips[3] [62]-[65]. After I joined the Electronics Labs at EPFL in 1992, apart from the modeling work mentioned above, my other Ph.D. students were working on low-power and low-voltage CMOS design and were intensively using the EKV design methodology.

With the purpose of having ever decreasing supply voltages, the concept of log-domain circuits was first investigated. The log-domain approach uses instantaneous companding where the currents, having basically an unlimited dynamic range (DR), are com-

[3] For more details on the history of CMOS read-out chip design for particle physics experiment, please read the article by E. Heijne in this issue.

pressed logarithmically when transformed into voltages and expanded exponentially when converted back to currents. The voltage swings are hence strongly reduced making them almost independent of the supply voltage, which can be reduced to the minimum required for a proper operation of the circuit. This principle is illustrated by the simple integrator shown in Fig. 2(a), where the companded voltage across the linear capacitor C is expanded when transformed to the output current i_{out} using the nonlinear function *f(v)*, which for log-domain circuit is simply an exponential function.

It can be shown that, in order to have a linear transfer function from the input current i_{in} to the output current i_{out}, the current on the capacitor C has to be inversely proportional to the derivative of the expanding function *f(v)*. This can obviously easily be implemented using the exponential I-V characteristic of bipolar transistor since the derivative remains an exponential function which can be matched to the output expander. It leads to the simple translinear integrator shown in Fig. 2(b). The principle was successfully implemented in several BiCMOS filters by G. van Ruymbeke and M. Punzenberger [66]-[69]. The basic integrator used in [68] is presented in Fig. 2(c). The same concept can also use the exponential characteristic of the MOS transistor in weak inversion, which was explored by D. Python in his Ph.D. thesis [70]. The basic CMOS log-domain integrator used in [70] is shown in Fig. 2(d).

Other innovative circuits taking advantage of the MOS transistor operating in weak inversion were developed by R. Fied for the purpose of low-power analog signal processing. The goal was to emulate the behavior of large electric power distribution networks in order to determine their stability [71]. The main advantages of using an analog VLSI circuit are the much shorter computation time and lower complexity compared to the classical simulation methods based on numerical calculations [71]. The limited accuracy achieved by the analog simulation can be circumvented by using the solution found by the circuit as initial conditions for the numerical simulation, greatly speeding up the convergence.

All the circuits mentioned above were operating at a rather low frequency. Following the exploration done by other research groups in the US and in Europe in the 90's to investigate the potential of CMOS for RF, we also started to work on RF CMOS design but focused on low-power and low-voltage circuits for low data rate and short distance wireless communication targeting applications such as wireless sensor networks. The goal was to study the feasibility of designing a complete RF CMOS transceiver operating in the ISM 433 MHz band and running at 1-mA from a 1-V supply voltage. A.-S. Porret, T. Melly and D. Python designed such a complete transceiver. It

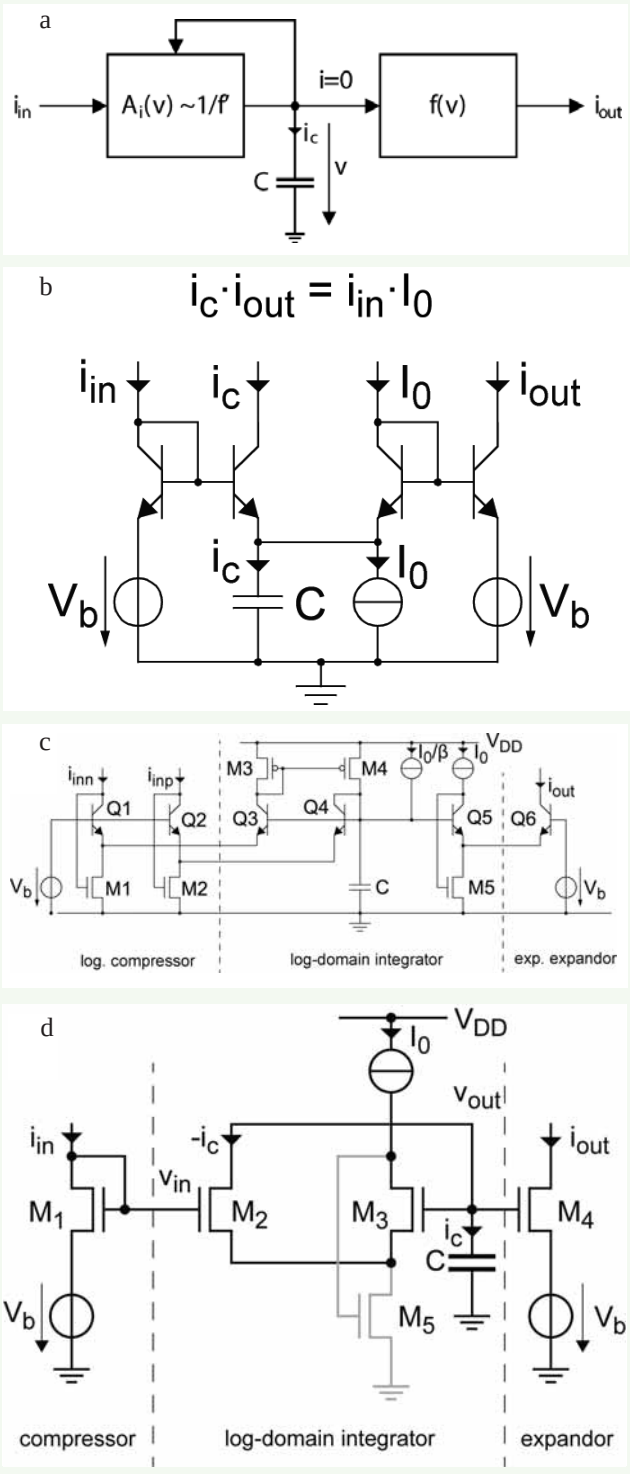

Fig. 2. Log-domain integrators: a) principle of instantaneous companding integrator b) implementation principle in bipolar [69], c) implementation principle in BiCMOS [68], d) implementation principle in CMOS (weak inversion) [70].

was running at 1-V, despite the 0.75-V threshold voltages of the 0.5 µm process, and consumed around 1-mA in receive mode, demonstrating the feasibility of implementing low-power radio in CMOS [72], [73]. It also showed that the EKV design methodology could

be extended to the design of low-power and low-voltage RF-CMOS circuits. This work was then continued at the CSEM, migrating the original design to a 0.18 µm standard digital process and including all the functions required by a wireless sensor node (sensor interface, ADC, µC, embedded low-leakage SRAM, power management, etc) on a complex system-on-chip (SoC) [74]. This set the basis for new RF-CMOS activity at CSEM that started in 2001 and focuses on the design of ultra low-power radios for wireless sensor networks [75]. This constitutes a very good example illustrating the technology transfer mission of CSEM: Ideas are first explored in the academic environment (for example at EPFL) and if successful they are transferred to CSEM for further improvement and consolidation before being proposed to industry as a technology platform that can be customized and industrialized for a particular application. More recently, this activity has been combined at CSEM with the development high-Q resonators such as bulk acoustic wave (BAW) resonators and temperature-compensated low-frequency MEMS resonators for the implementation of an ultra low-power MEMS-based radio [76]-[79].

IV. CONCLUSION

From its beginning, the EKV MOS transistor model really enabled the design and optimization of new low-power and low-voltage analog and RF circuits where most transistors were operating in the weak and moderate inversion regions. Together with the development of the EKV compact model, a design methodology for low-power circuits based on the inversion factor was formulated. This powerful concept allows the optimum operating point to be chosen and the transistor to be sized accordingly. The availability of a MOS transistor model and the related design methodology that is valid in all modes of operation becomes even more crucial today. Indeed, with the aggressive downscaling of CMOS technologies, the operating points of analog and even RF circuits transistors are more and more shifted from the traditional strong inversion region towards the moderate and eventually the weak inversion regions.

ACKNOWLEDGMENT

First I would like to thank Prof. Eric Vittoz who taught me the art and science of low-power CMOS analog IC design based on a deep understanding of the operation and correct modeling of the MOS transistor. I would also like to thank all my Ph.D. students who pushed the limit of low-power IC design always a bit further.

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About the Author

Christian C. Enz (M'84) received the M.S. and Ph.D. degrees in electrical engineering from the Swiss Federal Institute of Technology, Lausanne (EPFL) in 1984 and 1989 respectively.

From 1984 to 1989 he was research assistant at the EPFL, working in the field of micropower analog CMOS integrated circuits (IC) design. In 1989 he was one of the founders of Smart Silicon Systems S.A. (S3), where he developed several low-noise and low-power ICs, mainly for high energy physics applications. From 1992 to 1997, he was an Assistant Professor at EPFL, working in the field of low-power analog CMOS and BiCMOS IC design and device modeling. From 1997 to 1999, he was Principal Senior Engineer at Conexant (formerly Rockwell Semiconductor Systems), Newport Beach, CA, where he was responsible for the modeling and characterization of MOS transistors for the design of RF CMOS circuits. In 1999, he joined the Swiss Center for Electronics and Microtechnology (CSEM) where he launched and lead the RF and Analog IC design group. In 2000, he was promoted Vice President, heading the Microelectronics Department.

He is also lecturing and supervising undergraduate and graduate students in the field of analog and RF IC design at EPFL, where he is Professor since 1999. His technical interests and expertise are in the field of very low-power analog and RF IC design and semiconductor device modeling, with a particular focus on noise. He is the author and co-author of more than 140 scientific papers and has contributed to numerous conference presentations and advanced engineering courses.

Together with E. Vittoz and F. Krummenacher he is one of the developer of the EKV MOS transistor model and the author of the book "Charge-Based MOS Transistor Modeling - The EKV Model for Low-Power and RF IC Design" (Wiley, 2006).

He is member of several technical program committees, including International Solid-State Circuits Conference (ISSCC) and European Solid-State Circuits Conference (ESSCIRC). He has served as a vice-chair for the 2000 International Symposium on Low Power Electronics and Design (ISLPED), exhibit chair for the 2000 International Symposium on Circuits and Systems (ISCAS) and is chair of the technical program committee for the 2006 European Solid-State Circuits Conference (ESSCIRC).

Since 2001, he has been the chair of the IEEE Solid-State Chapter of West Switzerland.

Watch Microelectronics: Pioneer in Portable Consumer Electronics

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Abstract

The quartz watch as pioneering media for new technologies is highlighted with examples both from the past and the present. Technical orientations and resulting areas of expertise for EM Microelectronic, the semiconductor manufacturer of the Swatch Group have been shaped by constraints and requirements genuine to the watch-making industry. The article describes typical "watch microelectronics" skills and solutions and how they diffused into other portable consumer electronics applications.

Index Terms

Electronic watches, watch making, low power, low voltage, integrated circuits, microcontroller.

I. Introduction

With the 'renaissance' of the mechanical watch, 'complications', 'grand complications' and spinning tourbillons are again enjoying unequaled prestige. Skills, handicraft and know-how of – especially Swiss – watchmakers still contribute to the emotional appeal of modern mechanical timepieces. But computer-controlled equipment, high-tech industrial manufacturing and automated assembly techniques have also facilitated the return of mechanical watch. Prior to 1970, Swiss time pieces made of small gears and high precision springs set the world standard in timing. Confident in the tradition of their craft and dominant position on the worldwide watch market, Swiss watchmakers could hardly imagine that a paradigm shift in the way to set the time base of watches would almost annihilate the entire industry. They could even less imagine that micro and nanotechnologies would once open new perspectives also to the mechanical watch.

A. Creation of a Joint Research Lab

In 1962 already, in a premonitory effort to build up and establish microelectronics know-how in Switzerland, Swiss watchmakers founded the *Centre électronique horloger* (CEH) in Neuchâtel, a joint research laboratory dedicated to microelectronics in horological applications. No later than 1967, engineers and researchers from the CEH came up with first quartz wrist watch prototypes working with an integrated circuit. The step from research prototypes to industrial products however, confronted the watchmakers with unknown problems and challenges and the industry leaders at first failed to recognize the relevance of this new technology. Trapped by their mindset and traditional approach of doing things, they were unable to anticipate a coexistence of quartz and mechanical watches. By that time, Swiss watches represented about 44% of the world market; fifteen years later this share had dropped to 13% and was at the edge of disappearing.

With the creation of the CEH, the Swiss watch-making industry did not prevent the quartz crisis leading to a general economic down-turn and low point between the 1970's and 1980's, but it had laid the cornerstone of its own redemption. Since then, major technical developments followed without interruption. Partnerships with academia were established and research institutions constantly adapted to respond to the watch-making industry's needs. Research efforts and results gave rise to numerous initiatives, leading watch component manufacturing companies to invest into microelectronic production infrastructures, which allowed them to expand into markets well beyond the sole electronic watch market. Portable electronics today quite often uses technologies which can be ascribed to insights from the work of Prof. Eric Vittoz and his team at the CEH and which those companies translated into products.

B. Watchmakers Invest in Microelectronics

In 1983, following the advice of Mr. N. G. Hayek, the two largest Swiss watch-making groups (SSIH and ASUAG) merged into a single entity, the *Société suisse de microélectronique et d'horlogerie* (SMH) better known today as *The Swatch Group Ltd*. In this context, it is of course impossible to overlook the Swatch watch itself, which became instrumental for the revival of the Swiss watch industry through its novel approach of production and marketing techniques.

Power consumption has always been the critical issue for electronic watches. Therefore, Ebauches SA – which belonged to ASUAG – created a new unit entirely dedicated to the development and production of CMOS integrated circuits for watches. Ebauches SA bought a CMOS technology license from Hughes Aircraft Company Inc. and in 1975, the new unit delivered its first Al-Gate CMOS circuit.

This production unit has since become a full-fledged semiconductor company under the name of *EM Microelectronic-Marin SA*. As a member of the Swatch Group Electronic Systems companies, the company today still is the first semiconductor provider of the Swiss watch-making industry. Meanwhile, reaching out into other low power, low voltage

applications, EM's non-watch business share represents more than 90% today.

It is probably not exaggerated to consider EM Microelectronic and various other companies and research institutions dedicated to micro and nanotechnologies in the wider Neuchâtel area as an offspring of the quartz crisis. Together they constitute an industrial eco-system strongly rooted in and still serving the watch-making industry, even if they have clearly outgrown their native industrial environment.

C. Industrial Cross-fertilization

When writing about microelectronics and microcontrollers in watch applications here, we do it as a global semiconductor manufacturer with origins and strong ties in the watch-making industry. Our aim will be to show how the watch – electronic and mechanical alike – constitutes a permanent innovation factor for the broader micro and nano-technological industry and vice-versa. Watches have played a pioneer role to bring a set of key technologies to industrial maturity and to consumer awareness. There is a constant interaction and cross-fertilization between the watch-making industry and the overall micro and nano-technological industry (fig. 1). Ideas, technologies and solutions generated on one side bring about new ideas, technologies and solutions on the other side. Moreover, in the whole process, the very specific skills and know-how genuine to the watch-making industry is permanently being refined, honed and optimized through the interaction itself.

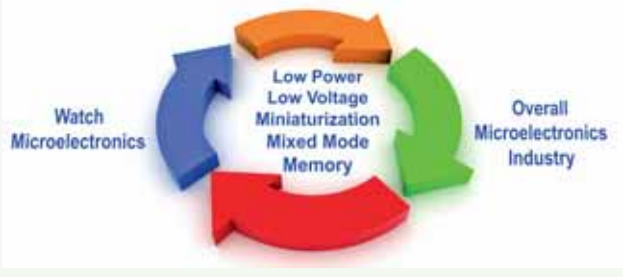

Fig. 1: Industrial interaction diagram

II. Areas of Expertise Specific to Watch-Making

EM Microelectronic has been founded originally to design and produce integrated circuits for the watch industry. Many of its technical orientations and resulting areas of expertise have therefore been pre-determined by constraints and requirements genuine to the watch-making industry.

A. Early Low-Power Efforts

Very low power consumption is certainly the first and foremost area of expertise a semiconductor manufacturer serving the watch industry had to develop. In the early 1970's it appeared that CMOS technology would be a more promising path to low-power devices than bipolar still used by *Faselec*, the Swiss semiconductor manufacturer who produced watch circuits by that time. Through its decision to start an independent CMOS production facility in Neuchâtel, Ebauches SA created the necessary conditions for the emergence of an industrial-scale low power, low voltage expertise.

The two components that account for the power budget in an analog electronic watch are the electric motor and the control electronics, or in other words, the integrated circuit. If the motor takes the lion's share of the consumed power (~80%), the integrated circuit couldn't be neglected and has been trimmed to the absolute minimum power consumption. Funny situation sometimes arise when circuits based on watch-making know-how arrive into other industrial applications: a customer testing one of our oscillator circuits called and claimed that the circuit was working very well, but he couldn't measure any current consumption. We then had to ask him to switch his ampere-meter from the mA scale to the nA scale.

A simple watch circuit consists of an oscillator, a divider chain and a motor driver. Since its creation, EM continuously improved the oscillator block, which accounts for the largest part of the circuit's current consumption. Figure 2 illustrates the evolution of the current consumption in such a simple watch circuit from the company's beginning till today.

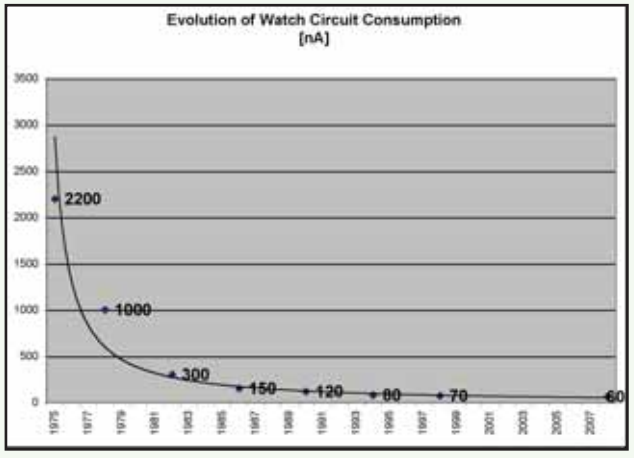

Fig. 2: Evolution of watch circuit current consumption

B. Voltages Well Below 1.0V

Low-voltage is another area of expertise. Electronic watches are traditionally battery operated devices; even if today alternatives based on various energy harvesting techniques (kinetic or solar energy) do exist, the majority of electronic watches is still battery-operated. Small size silver-oxide primary batteries such as produced by Renata AG – a Swiss battery manufacturer – provide a lifetime of more than three years to most analog quartz watch movements. Their form factor and size allow for the smallest and

thinnest watch caliber sizes. Typical voltage of this battery technology is 1.5V, but watch IC's are specified to guaranty stable oscillator and microcontroller operations down to a supply voltage of 1.1V. By today's standards, this is not an outstanding performance anymore, but EM Microelectronic had reached this voltage level already in 1975 for watch ASICs and in 1992 for watch microcontrollers. This low-voltage know-how was essential to help the company to further push back the limits. Today's low-power, low-voltage microcontrollers (e.g., produced for health care and body-care electronic devices) are able to operate down to 0.85V. Low-voltage know-how proved also to be critical for the development of the first RFID circuits in 1989.

In 2002, EM Microelectronic pushed the low-voltage limits even further down with the development of a fully depleted Silicon-on-Insulator (FD SoI) 1µm process allowing operating voltages below 0.5V. Prototype watches built with these circuits highlighted new limits that may be achieved with appropriate design techniques.

C. Mixed-mode Circuits

Watch integrated circuits are used to control devices, such as motors and they often process the input from devices or sensors they are controlling. To interface those devices, the circuit (simple ASIC and microcontroller alike) needs analog to digital converting capability, meaning that every watch circuit is also a mixed-mode analog and digital circuit. Mixed-mode semiconductor processes usually do not reach the ultimate feature size used to produce purely digital devices. However, they require an accurate control of passive components' (i.e., resistors, capacitors, diodes) design parameters, as well as over the characteristics of parasitic bipolar transistors.

D. Miniaturization, a Collaborative Effort

Because of the confinement level of the different watch parts, miniaturization is another crucial area of expertise in watch-making. Feature size on the IC itself is however not the primary issue here because even for the more complex watches, relative IC complexity remains limited. The challenge lies more in the assembly and packaging technologies. Very thin watches might require wafer thinning techniques, leading EM Microelectronic to develop a back-lapping capability to produce ICs down to 100-150µm in production volumes. Such capability is again an advantage for the production of chips delivered for very thin RFID labels.

Space saving connection technologies, such as flip chip assembly, have also been developed. Although bumping techniques were known from the labs, EM Microelectronic was one of the first companies worldwide to industrialize bumping processes, even licensing such technology to semiconductor giant Intel in 1993.

Especially in the area of assembly and packaging techniques, solutions were often the result of a collaborative effort between several electronic systems companies within the Swatch Group. The field-proven System-in-Package solution to produce Real-Time Clocks for the cell phone industry has been applied to watch applications, demonstrating once more the technological cross-fertilization of companies working simultaneously for the watch industry and the electronics industry in general. EM Microelectronic and sister company *Micro Crystal* – Swiss producer of quartz crystals – have collaborated with ETA SA Manufacture horlogère Suisse – one of the world's largest manufacturers of watches and movements - to develop and integrate a crystal oscillator and a watch IC into a single smallest possible SMD ceramic package, thus reducing the electronics of the watch to just one component. The component is factory pre-calibrated and programmable by the watchmaker, depending on its final use.

E. Non-Volatile Memory

Early activities on non-volatile memory at EM Microelectronic reaches back to 1979 with development of the world's first completely TTL-compatible, single 5V supply, nonvolatile RAM utilizing a three-layer polysilicon process and a low-current floating-gate tunneling approach [1]. Memory development has later been refocused to technologies allowing lower voltages.

The introduction of the revolutionary Swatch manufacturing process in 1983 also brought unforeseen challenges. The Swatch assembly model had been inspired by the "Delirium Tremens" concept developed by engineers at Ebauches SA in 1979 and allowing one year later to achieve a gold watch less than 2 mm thick. They had used the back of the case as the bottom plate for the movement. Engineers at sister-company ETA took over this idea for the Swatch plastic watch. Synthetic materials were chosen for the watch cases as well as a new ultra-sonic welding process to seal the case.

In horology, *precision* of a timepiece has to do with frequency stability of a time piece independently of environmental conditions (temperature, position of the watch, etc). *Accuracy* has to do with having the frequency set to the proper value. Before regulating a watch, it must be adjusted for sufficient precision that allows it to be regulated to the desired accuracy. Mechanical watches are regulated by tuning the balance wheel, hair spring and escapement. In a quartz watch, precision is intrinsic to the technology of the tuning fork crystal. To achieve the desired accuracy in first quartz watch models, the quartz crystals needed to be matched with the proper capacitor in order to reach an operating frequency of exactly 32.768kHz.

With the Swatch assembly concept, engineers observed that the ultra-sound welding process detuned the crystal, but then, the watch was already sealed and its parts couldn't be directly accessed anymore. The only way left to access the electronic circuitry of the watch after the assembly process was through the battery contact plates. EM's engineers decided to replace the capacitor matching or trimming principles with a digital tuning of the frequency divider chain by means of non-volatile memory. For this purpose, EM Microelectronic developed its own EEPROM cells accessible over a dedicated 2-wire programming protocol and they delivered the first non-volatile memory based CMOS watch ICs in 1984 to ETA. IC design engineers, supported by the process team designed the EEPROM cells which could be realized with only one additional mask in EM Microelectronic's HCMOS process. The availability of this very economic memory technology gave the company a significant advantage in a number of non-watch applications. It was essential already in early RFID products and especially also in a number of sensor interface circuits, which always needed trimming or calibration functions. Compared to other external processes, EM Microelectronic has since been able to keep the number of additional masks for memory (EEPROM or Flash) in its own semiconductor processes at the lowest levels.

F. Resilience

Finally, robustness is also an issue in electronic watches. The developed assembly and packaging techniques have to withstand a very tough acceleration test: the homologation process of an electronic watch model includes a 5000G shock test to which, the watch has to resist without damage. An integrated circuit may well resist mechanically such a test, but the designers didn't imagine that the shock would induce a voltage peak into the piezo-electric buzzer used in some models. The first circuits were destroyed and the subsequent versions would include the needed over-voltage protection.

III. From Microprocessor Prototypes to Microcontroller Products

A. Watch Microcontroller & Interface Functions

The electronic watch seems to be the first portable, battery operated electronic mass market product in history. On June 1, 2006, Swatch celebrated the 333 millionth Swatch, a time piece which has been produced in several thousand models, with different functions. Through its novel approach of watch production and marketing, Swatch signaled that functionality and time-telling were no longer the primary selling points in a watch. Swatch was not so much marketing time-telling as it was fun and fashion.

Functional diversity however remains a must to meet diversity in customers' preferences, a point which is not easy to conciliate with cost optimization requirements of high volume industrial watch production. Watch components (i.e., also semiconductor components) should therefore be as generic (reusable) as possible, while remaining as cost-effective as possible: there is always a compromise or balance to be found. *Reusability* across different models limits development costs and increases flexibility in an environment characterized by a high innovation pace in functionality and design. *Cost effectiveness* in semiconductor is essentially limiting chip size and using cost-effective production process. The quest for the right optimum especially affects watch microcontrollers used in more complex or functionally rich models. In theory, it would be ideal to have one generic microcontroller chip applicable to every watch model; in reality however watchmakers are working with microcontroller families built around a few dedicated microprocessor cores.

A *microcontroller* is generally considered as a digital device. A *watch microcontroller* however is a mixed-mode device with a digital microprocessor core, memories and a set of mainly analog interfaces. The most common interfaces are motor drivers with adaptive control; there are up to 6 motor drivers on microcontrollers for purely analog chronograph watches. Other interfaces include LCD drivers for digital displays, LED drivers for backlight, sensor interfaces (touch, shock, acceleration, temperature, etc), vibrating alarm and buzzer drivers, I^2C or SPI interfaces, button and crown rotation detection and more.

B. Technology Transfer and Diffusion

Almost all watch microcontrollers developed by EM Microelectronic for Swatch Group products are based on microprocessor cores designed by the Swiss Center for Electronics and Microtechnology (CSEM). CSEM was founded in 1984 out of the CEH and other research labs and represents the continuation of the original research initiatives of the Swiss watch-making industry. As will be shown further down in this article, the microprocessor example epitomizes the cultural proximity and actual technology transfer process between research institutes of the Neuchâtel area (e.g., CSEM, Institute of Microtechnology of the University of Neuchâtel) and the Swiss watch-making industry. But it also underlines the key role of an industrial semiconductor manufacturer in transforming research and lab results into products ready for mass-production. The microprocessor core has to be optimized, design libraries need to be developed, memory technologies have to be added, digital and analog interfaces need to be defined. Finally, a microcontroller remains useless without software development tools (high level programming language, com-

piler, linker, debugger, in-circuit emulator).

The article's examples show how technologies, originally developed for watch applications are brought to industrial maturity; it further underline how these technologies are then "diffused" into other, mostly portable electronic applications.

IV. From RFID in a Watch to RFID Everywhere

RFID ICs are field powered devices whose reading distance depends on the voltage at which the device can start to operate (typically 1.0V). Low-power, low-voltage microelectronics know-how developed for watch-making applications was a cornerstone for the development of an entire RFID business. Transponders for pigeon races developed in 1989 has been EM's first RFID application. The same technology has then been integrated rapidly into Swatch watches used for access control applications, giving EM another incentive to invest in RFID. The Swatch thus became the first mass market media to bring RFID to the public. Today more than 700 ski resorts in 25 countries worldwide can be accessed with Swatch's Snowpass (fig. 3). Swatch Access technology is also in use in several other sports, such as soccer plays.

These early applications have been developed in a low-frequency, 125kHz technology. EM Microelectronic has since developed product families in all relevant RFID standard frequencies (125kHz, 13,56MHz, UHF and 2.45GHz) and all major application domains (i.e., access control, animal identification, logistics and automotive). Together with Swatch, the group's semiconductor company has further pioneered innovative public transport solutions [2]. The company belongs now to the top three RFID circuit manufacturers worldwide. Low-voltage and EEPROM technology developed for watches, as well as an RFID-in-a-watch project were the foundation out of which a whole new business segment could be developed.

V. From Multifunctional Watches to Flexible Display Technologies

A. Multitasking 8-bit Watch Microcontroller

In 1991, EM Microelectronic took a license of the 8-bit multitasking PUNCH-microprocessor core developed by the CSEM on behalf of several Swiss watch-making companies. The PUNCH architecture has been designed in an effort to create a generic building block for more sophisticated quartz watches. EM Microelectronic's first microcontroller based on this core integrated motor drivers for analog watches and LCD drivers for combined analog/digital watches. Tissot's Two-Timer, a multifunction analog/digital wristwatch – launched in 1986 – able to display two time zones and a single crown to control all functions was the first commercial wristwatch to feature a PUNCH microcontroller.

A further PUNCH-version was used in the *Swatch Beat* (fig. 4). This first multifunctional entirely digital Swatch watch was introduced in 1999, one year after

Fig. 3: RFID technology developed originally for Swatch Access applied to car immobilizer and remote keyless entry systems

Fig. 4: From multifunctional watch (Swatch Beat) to flexible plastic LCD displays

the launch of the *Internet Time*, a new decimal time concept. Instead of dividing the virtual and real day into 24 hours and 60 minutes per hour, Swatch's Internet Time system divided the day into 1000 “beats”. One of the goals of the system was to simplify the way people in different time zones communicated about time, mostly by eliminating time zones altogether. Internet Time was also based on a new Meridian (as opposed to the Greenwich Meridian) going through Swatch’s office in Biel, Switzerland and is called the BMT Meridian. So in addition to the standard time format, the digital Swatch would also display beats prefixed with an @ sign.

B. Need for Enhanced Display Technologies

Microcontrollers were first designed into watches with analog and digital displays. Microcontrollers opened new possibilities but also new needs especially on the display side.

Higher end brands such as Omega and Rado have also created models with mixed-mode displays or specialty displays (e.g., full-dial LCD display with a hole in the middle for the watch hands). Displays available on the market didn't always meet the esthetical standards (i.e., contrast, color) or physical requirements (i.e., viewing angle, shape) of the watchmakers. In 1986, EM Microelectronic installed an LCD production infrastructure and started production of LCD displays simultaneously for the watch industry and for other industrial segments (e.g., avionics). Initially producing display in TN technology, the activity has since been diversified. Besides watch applications, the company’s displays are widely used today in white goods, portable electronic devices, computer peripherals etc. In its latest move, still aiming at miniaturization and increased design flexibility for watches, EM Microelectronic and Asulab, the Swatch Group’s corporate R&D lab, have co-developed a flexible plastic LCD display technology (fig. 4).

VI. From Minimal Complexity Watch Microcontrollers to Body Care Devices

A. 4-bit Microcontroller Gives the Tone

For some watch applications, an 8-bit microcontroller was over-dimensioned, both from the point of view of product cost and capability. In 1992, EM Microelectronic asked the CSEM whether it would be feasible to realize a 4-bit low-power microprocessor architecture with no more than 1mm^2 footprint in a 2µm analog low power technology (called ALP-2). The task was given as diploma work to a student who came up with the µPUS (acronym for *microprocesseur ultra-simple*) architecture and the result caught the interest of ETA who was looking for a solution for Swatch's Musicall (fig. 5), a wristwatch featuring an alarm function and playing a 7 tone melody. Japanese micro-

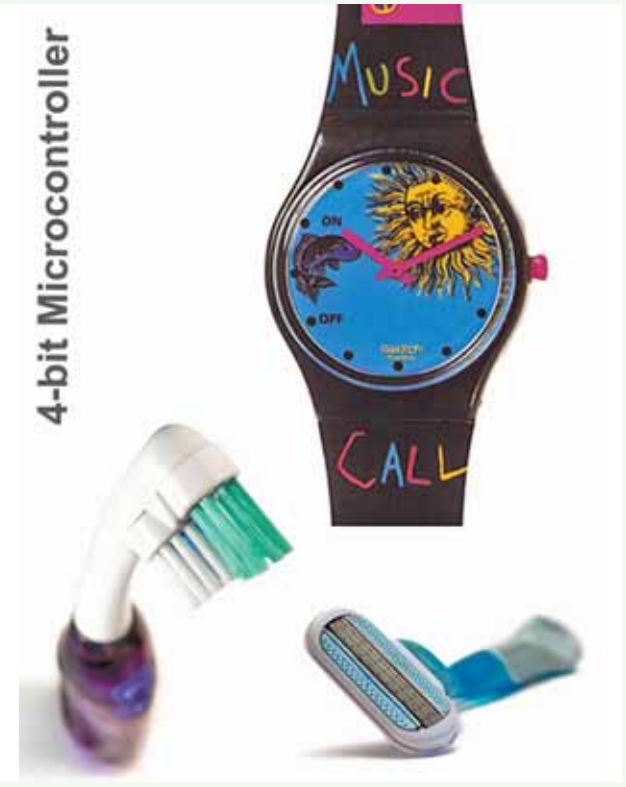

Fig. 5: 4-bit µPUS Microcontroller in Swatch Musicall and electronic body care devices

controller alternatives were able to output only two frequencies. EM Microelectronic built the microcontroller and the first Musicall watch was launched in 1993 by Nicolas G. Hayek and French electronic music composer and performer Jean-Michel Jarre in the Palais de I’Unesco in Paris.

Several versions of µPUS-based microcontrollers have been realized subsequently for different multifunctional watches. Today this microcontroller family is still at the heart of most analog quartz chronograph watches made by Swatch and ETA's analog quartz chronograph calibers.

B. Low Voltage in Body Care Devices

Expanding from watches into other portable, battery-operated applications, EM Microelectronic introduced its first sub-1.0V microcontroller in 2004. The EM6682 is a 4-bit microcontroller with a voltage operating range of 5.5 down to 0.9V. Sub-1Volt operation in this circuit was achieved without artificial means; the entire internal circuitry is running down to the lowest voltage. Taking into account the discharge characteristics of a 1.5V AA battery, a microcontroller operating down to 0.9 volt will be able to extend the battery life by 50%, compared to a 1.2V circuit (fig. 6). The key point with such a technology is not only the increased battery life-time, but also the fact that devices can be operated with a single cell, instead of two, which allows increased miniaturization and

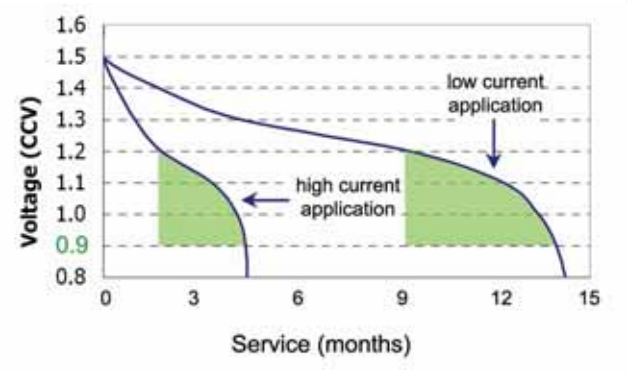

Fig. 6: Constant power discharge curves of a standard AA alkaline cell

design freedom, as well as lower manufacturing and usage cost.

Cost optimized ASIC versions of EM's 4-bit microcontroller can be found today in electric toothbrushes (fig. 5). Another application example of this minimal complexity and lowest voltage microcontroller is a shaver model with a vibrating motor in the handle, which optimizes the shaving quality. In this application, the microcontroller is used to control the motor and maximize the life-time of the single cell, 1.5V AAA battery.

VII. Tactile Technology: T-Touch

The availability of a dedicated watch microcontroller in the Swatch Group fueled the creativity of the development teams in the Swatch Group and allowed a number of pilot projects to investigate the integration of various technologies in watches.

Asulab, the R&D company of the Swatch Group, was at the forefront of such efforts and presented several such watch prototypes [3] always with the constraints of retaining the specific characteristics of watch-making products such as size, precision, water-resistance or resilience. Ergonomic characteristics and intuitive use of the product were of primary importance. One of the key technologies tested and improved in such projects is certainly the tactile sapphire glass, brought to fame by Tissot's T-Touch (fig. 7 & 8).

The watch combines compass, thermometer, barometer, altimeter in a regular steel case analog/digital watch. The tactile glass can be activated with the right center crown and all the watch functions can then be controlled by simply touching one of the seven sensitive areas on the glass (fig 7).

This watch ideally illustrates the need for a multitasking capable microcontroller able to manage the different functions and peripherals, based on a primary battery without sufficient life-time. Originally, the T-Touch microcontroller has been designed around the PUNCH core by Asulab's engineers, who also developed and integrated the capacitive touch

Fig. 7: Tactile areas on the Tissot T-Touch

interface, LCD drivers, bidirectional motor drivers, sensor interfaces (a mechanical compass coupled with a Hall sensor detects the north and the direction is displayed with the watch hands.

The T-Touch has generated by-products in two areas outside of the watch-making industry. The first one is of course the *tactile technology* itself, which has since been applied to display modules, ready to be integrated into either in white goods, consumer electronic devices and computer peripherals.

The second important area is *MEMS interface* know-how for accelerometers (fig. 8), angular rate

Fig. 8: Sensor interfaces in Tissot T-Touch and game controller with 3D acceleration sensors

sensors, pressure sensors, featuring atto Farad detection level (10^{-18}F) and full self-test capability including the MEMS part and interface. Sensor interface technology was used also in the Swatch Touch family; hitting the glass with the tip of the finger would set off some function such as light up the dial, stop an alarm of play a small game.

VIII. From SIM-Cards to Flash-based RISC Microcontrollers

A. Flash Memory and Time-to-Market

In 1997, EM Microelectronic was looking for semiconductor projects to be realized in more advanced silicon processes than the ones it had in-house. Smartcards seemed to be a promising application, both because of the level of integration required and because of the fast evolution pace in this market. An initial SIM card market analysis revealed that the major market share relied on ROM-memory chip versions, implying a new chip for every application evolution. Considering the decreasing time-to-market of such products, EM Microelectronic took the approach of developing SIM-Card (fig. 9) circuits with Flash program memory. Such technology represented a significant competitive advantage and helped the company to reach a leading position in the worldwide SIM-Card IC market.

If watch-making was the cause for EM Microelectronic to develop its EEPROM technology, giving the company an advantage for non-watch applications, we can say that the smartcard industry gave the company the impulse to introduce Flash memory technology, which now in turn paves the way for other innovations in watch-making.

From the microcontroller point of view, multifunctional quartz watches followed a path similar to many other mass-market microelectronics applications. Originally the products were based on ASIC circuits, implying a new IC for every new product or even product version. With the µPUS and PUNCH cores and a set of interface building blocks, the watch makers introduced a more modular approach; but these circuits were all ROM-based versions, meaning that every software change required a new metal mask, i.e., a new chip. If original watch ASICs were considered non-programmable devices, ROM-based microcontrollers were qualified as fab-programmable (i.e., programmable by the wafer foundry) devices. The next natural evolution step was then to offer field-programmable devices to the watchmakers (i.e., ETA).

B. RISC Microcontroller Architecture in a Watch

In 1998, EM Microelectronic initiated the development of its latest watch microcontroller generation based on CSEM's CoolRISC 8-bit core with, besides the required typical watch interface building blocks, the addition of Flash memory. The original SIM card Flash memory could not simply be transferred to a watch circuit. Programming voltage and power consumption common to cell phone applications were much too high for a wristwatch. The technology had to be adapted; current Flash memory for watch applications operates at a programming voltage of 1.8V.

The CoolRISC microcontroller family is now in use in Tissot's technical watch family (latest T-Touch, Silent-T models, Navigator 3000 (fig. 10)). Swatch also uses it in the Swatch Fun Scuba (fig. 9) and Swatch Fun Boarder models. The Fun Scuba is the first Swatch with an automatic depth-meter which is automatically activated when the watch is one meter below the water surface. The hour hand displays depth down to a maximum of 40 meter. The minute hand shows the total dive time. Information about a dive can be stored and viewed/replayed by the diver at any time. Once out of the water, the watch automatically switches back to display the time, just like any other watch. The Fun Boarder is a variation on the same theme: instead of a depth-meter, it features an altimeter; the minutes hand shows the height up to 995m, while the hours hand shows the height per 1,000m.

Fig. 9: Flash memory developed for SIM-cards now used in watch applications (Swatch Fun Scuba)

C. Non-Watch System-on-Chip Applications

As always, when a given watch technology has a potential for non-watch application or vice-versa, EM Microelectronic would try to take advantage of it. The company has reused the CoolRISC core for embedded industrial sub-1Volt microcontroller versions.

The EM6819 features 0.9V operation without external components, 17kB Flash memory freely shareable between program and data memory. The Flash memory is readable and writeable within the whole circuit supply voltage range. The EM6819 is also the first 8-bit, Flash-based microcontroller worldwide able to work on a single battery cell down to 0.9Volt, without external components (coil and capacitor).

From the design of a microprocessor core combined with a library of different interface building blocks it is a short distance to reach a System-on-Chip design approach. Sometimes it is a mere definition of terms depending on the complexity level of the said building blocks. Anyway, drawing from the know-how developed in the various application domains, EM's engineers started to combine and integrate various functions for battery-operated consumer electronic devices.

EM Microelectronic has a long lasting presence in computer mice applications. As mice became wireless and battery operated, EM's specific low-power, low-voltage know how became increasingly critical for the computer peripheral manufacturers. The latest delivered circuits are single-chip optical motion calculators for wireless mice, which combine the 8-bit RISC microprocessor core, RAM, ROM, full sensor and light source control, a 27MHz transmitter for the wireless function, single battery DC-DC converter, optical sensor with image processor for either LED or laser light. Over the years, cumulating simple and most complex chips, EM Microelectronic has delivered well over 1 billion ICs to computer mice manufacturers (fig 10).

Fig. 10: 8-bit RISC microcontroller in a Tissot Navigator 3000 and in a System-on-Chip optical motion calculator for wireless computer mice

Several other technologies originally developed for the watch-making industry help EM Microelectronic to provide ever more sophisticated solutions to the automotive industry. Adapting its early RFID circuits, the company entered into automotive applications with immobilizers for car keys (fig. 3), a request of insurance companies to car manufacturers following a surge in car theft in the 1990's.

Today, car makers tend to integrate (fig. 10) the remote control function, remote keyless entry function and immobilizer into single chips. Current circuits integrate a RISC microcontroller, a UHF transceiver, advanced cryptography with side channel attack countermeasures, Flash memory and an RFID function in one chip able to be operated in battery or field powered mode.

IX. From the Pager Watch to Bluetooth ULP

A. Swatch The Beep

The very first microcontroller developed by EM Microelectronic was in 1991 for Swatch "The Beep", the first analog wristwatch with an integrated pager function (fig. 11).

The 4-bit Seiko microcontroller chosen by ETA to control the application couldn't handle incoming messages fast enough in early models, so EM Microelectronic was given the task do develop an ASIC to speed up message handling and buffering. EM's designers based their ASIC on specifically designed 8-bit microprocessor architecture with a dedicated instruction set. But the already booming cell phone market soon made this masterpiece of a highly integrated system solution obsolete.

B. Watches and Communication Technologies

Swatch The Beep was an early example of a recurring issue in wristwatches: communication technologies. Almost all relevant communication technologies have been prototyped so far in wristwatches by the Swatch Group, but not every effort ended up in a commercial products. Asulab has developed Swatch Talk GSM, an agenda watch with RF link to a PC, another Cell phone watch, a GPS watch to mention only some [3].

Starting in 2004, ETA developed watches based on Microsoft's Spot technology a type of advanced pager function based on the usage of an FM sub-carrier fre-

Fig. 11: Early watch with telecom application (Swath The Beep) and ultra-low power RF circuits for portable electronic devices

quency. These watches integrated a 32-bit dedicated ARM-Core platform. One of these models, the High-T, has been built for Tissot. The model featured a graphical user interface (GUI) based on a dot-matrix LCD display and tactile glass technology integrated in a steel case. Network and services availability being available only in the US, these models remained confined to this market.

C. Ultra Low Power (ULP) Bluetooth

Most communicating wristwatches realized so far with either a longer communication range or higher data rate capability could only be realized with rechargeable batteries. Acknowledging the need for demanding communication technologies at very low power, be it for watches or other applications, EM Microelectronic is currently working on a joint development project with partners from the industry and academic research to build a very low-power RF front end chip, compatible with the currently standardized ULP Bluetooth channels.

X. Conclusion

History tells that watch-making has been and still remains an extremely favorable, creative and innovative context for micro and nano-technologies. The wristwatch is acting as an extremely prolific catalyst in the technological quest for the better, smaller, more efficient and even more beautiful. Watch-making not only generates new technologies and whole industries, but often also acts as an early adopter. Numerous new technologies have been pioneered in watch applications; because wristwatches are a mass-market product, they are also the ideal platform to bring technological improvements to public awareness.

Tactile technology increasingly becomes pervasive especially in portable electronic devices (music players, cell phones, etc). Tissot had introduced its T-Touch already in the year 2000.

Electronic wristwatches have brought a long-term and steady contribution to the availability of low-power, low-voltage technologies and they have thereby significantly contributed to the feasibility of a wealth of other portable electronic applications.

The cross-fertilization described earlier in this article is however not limited to the *electronic* watch industry. Today, wristwatches have advanced to an abundance of choices from very cost effective entry-level quartz watches to the very high-end bejeweled mechanical masterpieces. It is no secret that currently mechanical watches are again high in the trend. Technological improvements and innovations continue to happen also in the mechanical segment.

Nivarox – a company of the Swatch Group specialized in the manufacturing of time-regulating components for mechanical wristwatches – prepares to install a production facility for silicon watch parts. Silicon is insensitive to magnetic fields and opens the way to new and more complex shapes. Moreover, silicon is lighter and harder than steel, needs no lubrication and is resistant to corrosion and wear. Production readiness of such parts originates on results of a joint MEMS project run by Swiss research institutes and Swiss watch-makers.

This latest example further underlines how a very traditional handicraft (mechanical watch-making) can take advantage of the most advanced technologies to improve the precision of its masterpieces, thereby developing and improving a unique know-how which will not fail to show fall-outs again outside of the watch-making industry. But such an example also proves the inevitable and essential role of Switzerland's industrial network, which remains at very forefront of watch-making technology.

Acknowledgement

To all engineers of the Swatch Group who over the years have contributed to bring research results to industrial maturity.

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About the Authors

Mougahed Darwish holds a doctorate in Physics from the Swiss Federal Institute of Technology in Lausanne (EPFL), Switzerland. He has been member of the Extended Group Management Board of the Swatch Group since 2005 and is responsible for EM Microelectronic, Micro Crystal, Renata, Microcomponent, Michel Präzisionstechnik, Sokymat Automotive, Oscilloquartz and Lasag. Dr. Darwish has been with the Group since 1979, starting as Project Manager for the Xicor-Ebauches joint venture. Previously, he had been active in research and development for the Centre électronique horloger (CEH) (today Centre Suisse de l'électronique et de microtechnique SA, CSEM). From 1985 to 2006, he ran EM Microelectronic as a CEO, where he is now a member and delegate of the board. Dr. Darwish is also member of the Swiss Academy of Technical Sciences.

Marc G. R. Degrauwe was born in Brussels, Belgium on August 16th, 1957. He received the engineering degree in electronics and the Ph.D. degree in applied sciences from the Katholieke Universiteit Leuwen (KUL) Leuven, Belgium, in 1980 and 1983, respectively.

During the summer of 1980 he was on leave at the Centre électronique horloger (CEH), Neuchâtel, Switzerland. From autumn 1980 to 1983 he was associated with KUL where he worked on the design of micropower amplifiers and sampled date filters. In July 1983 he returned to CEH. In 1984 when CEH was reorganized into the CSEM, he became Head of the Circuits Department, reporting to Dr. E. Vittoz. Later on, he became responsible for the Microsystems activity, the IC design, mask shop and tribological measurement equipment.

Dr. Degrauwe also lectured on analog circuit design from 1985 till 2006 at the University of Neuchâtel, Switzerland. He authored or co-authored more than 10 papers on low power in the JSSC Journal and the ISSCC Conference. He was also secretary of the European program committee of ISSCC. Dr. Degrauwe received the 1987 ESSCIRC Conference Best Paper Award for a paper on crystal oscillators he co-authored.

In 1999, he joined EM Microelectronic where he became COO in 2006 and CEO in 2007.

Thomas E. Gyger was born in Switzerland, in 1961. He received the engineer degree engineer in electronics from the University of Applied Sciences of Western Switzerland (HES-SO) in Saint-Imier in 1984.

Between 1984 and 1999, he worked as software project manager for various companies of Ascom, a international telecom solutions group, including 4 years at the corporate R&D labs. He is working for EM Microelectronic since 2000 as project manager for electronic systems and RFID projects with a focus on data security. He took over the function of Communication Manager in 2007. Part of his time at EM was devoted to project management for Swatch Group Research & Development, working on several watch projects with advanced technologies. Th. Gyger is also member of the Swiss Informatics Society.

Günther Meusburger was born in Austria 1945. He received the Academic Degree from Technische Universität, Vienna, Austria.

From 1973 to 1978 he was with Siemens Research Laboratories, Munich, Germany where he was involved in the design of DRAMs. In 1978 he joined Eurosil GmbH, Munich where he was responsible for the Design department for CMOS Low power, low voltage IC's. In 1984 he moved as Design Manager to EM Microelectronic in Marin, Switzerland, a company of the Swatch Group developing and producing also CMOS Low Power and Low Voltage IC's. Since 1994, G. Meusburger is business unit leader and responsible for the development of Watch IC's for the Swiss watch industry.

Jean-Claude Robert graduated in electronics from Swiss Federal Institute of Technology in Zürich (ETHZ), Switzerland, in 1971.

He joined the Technical Direction of Ebauches SA in Neuchâtel where he was in charge of developing integrated circuits for watches with LED, LCD and electrochromic displays. Since 1986 he has been responsible for the electronic development at ETA SA Manufacture Horlogère Suisse in Grenchen. He is currently Project Manager in the Advanced Research group at ETA and works in the field of new technologies and devices for the future watches.

J.-C. Robert has been Member from 1986 to 1998 and President from 1993 to 1995 of the Scientific Board of the Centre électronique horloger (CEH, french acronym for Watchmakers Electronic Center). He is also member of IEEE.

It's about Time: A Brief Chronology of Chronometry

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Prologue

The lobby clock's label boasted, in HP's characteristically understated way, that a cesium standard controlled the displayed time. While waiting for his host to greet him, Max Forrer reflexively checked his wristwatch, and noted a three-second disagreement. Although most people in 1968 would have dismissed the difference as trivial (if, indeed, they had noticed one at all), the discrepancy bothered the new director of the Centre Electronique Horloger (CEH). Since CEH's founding in 1962, engineers had toiled in secret at the Centre's labs in Neuchâtel, Switzerland to develop the world's first quartz-controlled wristwatch. They had succeeded brilliantly: In December of 1967, ten "Beta 2" prototypes had swept the top ten spots in the annual Concours held at the Observatoire de Neuchâtel, smashing all previous records by exhibiting drifts of only a few hundred milliseconds per day. Given the magnitude and consistency of that triumph, Forrer could not accept that his wristwatch was off by three seconds. Of logical necessity, then, the lobby clock had to be wrong, cesium notwithstanding. Once his host appeared, Forrer shared his reasoning, and a subsequent investigation revealed that the lobby clock was indeed off by about two seconds [1]. Word spread quickly among HP engineers that a *wristwatch* had caught an error in their atomic-controlled clock. The times – and certainly timepieces – they were "a-changin."

The Age of Continuous Time

Rejoice at simple things; and be but vexed by sin and evil slightly.

Know the tides through which we move.

– Archilochos, c. 650BCE

The path to Forrer's moment of rejoicing was anything but linear and predictable. Simple things – natural, continuous processes – such as the regular motions of the sun, moon and stars, had marked the tides through which we move for most of human existence. Sundials had been used since at least 3500 BCE, when obelisks appeared for this purpose in Egypt [2]. The 3300-year-old Luxor Obelisk is a beautiful example of how far the ancients were able to develop this technology (Fig. 1). Standing 23 meters tall, the 200,000-kilogram pink-granite monolith still tells time as accurately as it did when it was built.

Portable sundials appeared about two millennia later, contemporaneously with the first timekeepers based on an artificial (but still continuous) process: the flow of water. The oldest surviving example dates to the reign of Amenhotep III, over a century after the first written description. Consisting of a leaky bowl with graduations on the inner surface, sloping sides helped compensate for a varying drain speed as the bowl emptied. This early clock represents the first in a line that would see considerable refinement in the hands of the Greeks, who called them *clepsydras* ("water thieves," because of the outflow of water), starting around 325 BCE. Water clocks reached their evolutionary peak with a succession of Chinese water towers (200 CE to 1300 CE), the last of which operated bells and other mechanical indicators [2].

Figure 1 – The Luxor Obelisk at the Place de la Concorde in Paris, where it was moved from Egypt in 1829 (photo credit: David Monniaux)

A Little Relaxation is Good

The rather long periods (e.g., a day or a lunar month) of the natural processes accessible to the ancients made it difficult to mark time accurately in fine increments. Besides possessing periodicities that aren't directly traceable to any fundamental time constants, water clocks also suffer from the temperature- and impurity-sensitive characteristics of water, to say nothing of freezing. Partial solutions devised over the centuries include sundials surrounded by an array of marker stones to facilitate resolving shorter intervals, as well as the substitution of mercury for water in at

least one Chinese clock (around the year 976 CE) [3]. These improvements, useful (if occasionally toxic) though they were, represented only incremental modifications of technologies that had served well enough not to have stimulated more radical changes for five millennia.

After countless centuries of relative stasis, revolutionary (both figuratively and literally) technologies abruptly appeared in Europe, starting around the 13th century CE. Evidently, something had suddenly made people feel that there was a problem to be solved. Historian David Landes offers a provocative (and much-debated) hypothesis to explain why Europe was the center of these activities, instead of other regions with far better-established horological traditions. He argues that it was the growth of a professional class, with its need to charge for services on a finer-grain basis than by the lunar month, and the Catholic Church, with its almost arbitrary schedule of prayer and other liturgical activities, that together created a time-granularity problem [4].

The first examples of new clocks designed to solve this problem appeared in the late-13th to early-14th century. Richard of Wallingford's *Tractatus Horologii Astronomici* (c. 1330) provides the earliest known description of a weight-driven clock that employs an *escapement* [5], and Giovanni de Dondi's *Il Tractatus Astrarii* (c.1370) contains the first drawing of an escapement (Fig. 2) [6].

The invention of the escapement is what marks this era as wholly distinct from what preceded it. The subtle and profound action of the escapement transfers the burden of timekeeping away from continuous processes, with their inconveniently large and often fixed time constants, to artificial processes possessing much shorter and freely chosen time constants. The importance of that seemingly minor shift can hardly be overstated.

Figure 2 – Early mechanism, from Giovanni de Dondi's *Il Tractatus Astrarii*. It is the oldest extant drawing of a device using a *verge-and-foliot* escapement. Although what is shown is actually part of an orrery, it can function as a clock essentially without modification. (Wikipedia: de Dondi.)

The dominant form of escapement for about 400 years was the *verge-and-foliot* mechanism (see Fig. 3).

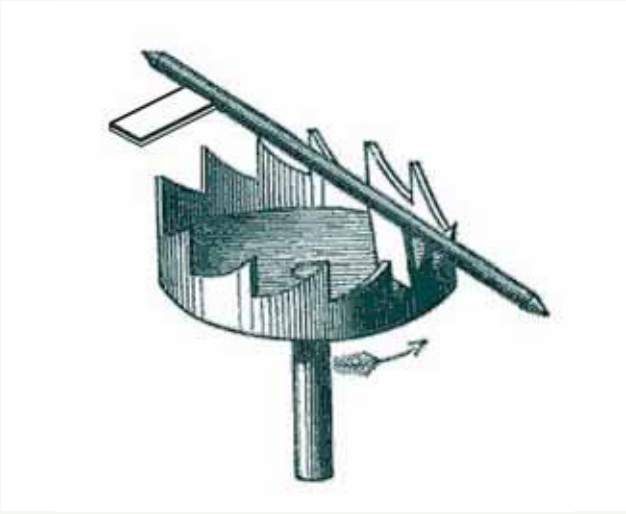

Figure 3 – Detail of an early escapement, showing the crown wheel, and the verge with palettes (*pallets* in English). Foliot not shown. (Wikipedia: Escapements.)

Through a gearing mechanism (not shown), force from hanging weights ultimately applies a constant torque to the axle of the crown wheel, causing it to turn in the direction indicated in the figure. The saw-toothed wheel in turn drives the verge discontinuously by alternately hitting one of two palettes. As shown, the palettes are typically disposed in quadrature around the rod. A saw-tooth hits one palette, causing the verge to rotate until the other palette encounters a saw-tooth on the opposite side of the crown wheel. That encounter briefly stops the verge and crown wheel altogether (indeed, it actually induces a small retrograde motion in both), until the continued application of torque on the crown wheel's axle eventually forces a restart. In this way, the continuous pull of weights produces a periodic intermittent rotation of the verge and, coincidentally, produces the now-familiar "tick-tock" sound we take for granted.

The periodicity of that motion is a function of the applied torque, as well as of the inertia of the verge. The typical method of adjusting the clock's speed is to alter the verge's inertia by using a propeller-like bar called the *foliot*. In this arrangement, the verge then acts as an axle for the foliot, and additional, movable weights attached to the ends of the foliot bar provide a means for changing the inertial moment, and thus the speed of the clock. The somewhat unusual

motion of the foliot may have given the bar its name (*folle* is French for crazy).

An electrical analog of this type of clock is an RC relaxation oscillator. A constant force on the main weights (a battery) accelerates (charges up) a mass (capacitor) up to some limit, which mass then gives up its all of its kinetic energy prior to the cycle beginning anew. As with electrical relaxation oscillators, the verge-and-foliot escapement permits oscillation over a wide range of frequencies, and thus enables the subdivision of time into almost arbitrarily fine intervals. And as with RC oscillators, the stability of a verge-type clock is somewhat less than ideal. Nevertheless, the escapement permitted the construction of clocks with "good enough" performance for a great many tasks. Measurements on the oldest working clock in Europe, at the Salisbury Cathedral in England, give us a rough idea about the typical accuracy one could expect. The Salisbury clock, built in 1386, drifts a large fraction of an hour per day. With care, one could perhaps expect to lose or gain half an hour per day [7]. By today's standards, of course, that level of error is considered unacceptable, but in the 14th century, it was unheard-of precision. Indeed, as late as the 15th century, soldiers were still using roosters as portable alarm clocks [4], conveying some idea of what performance level was tolerable. As a bonus, severely off-spec roosters could always be eaten.

As with many other clocks of this period, the Salisbury has no face. Instead, a bell chimes every hour, a function that is reflected in etymology: The very word *clock* comes from the Latin *clocca* (bell); other cognates include *glocke* (German), *klocke* (Dutch), and *cloche* (French), highlighting the universality of this early use of clocks. Prior to the mid-14th century, derivatives of the Latin term *horologium* had applied to all timekeeping devices. The development of the vastly superior escapement-controlled clocks required a new word to distinguish this invention from the sundials, water and sand clocks, and graduated slow-burning candles that had previously represented the state of the art.

Replacement of the suspended weights by a spring drive enabled much more compact shapes, bringing the wristwatch a step closer to reality. Peter Henlein of Nuremberg gets credit for building the first spring-driven clocks in the period 1500-1510, and is thus the father of the portable clock, and the grandfather of the wristwatch. Although the torque applied to the foliot diminished as the spring unwound, the revolutionary portability itself made the spring drive attractive despite the systematic drift. Later developments, such as the invention of the *fusée* – a cone-shaped coupler that provides a continually varying gear ratio as the spring unwinds – helped to reduce the variation in foliot torque until still better compensation methods came along [4].

Huygens' Resounding Success

The verge-and-foliot arrangement, though revolutionary, suffers from several important deficiencies that one may readily identify from a circuit analogy. The verge's palettes are in contact with the crown wheel's teeth a large fraction of the time, ensuring substantial frictional losses. Perhaps worse, the verge-and-foliot's oscillation frequency is a function of several variables that are hard to maintain constant, and so it is inevitable that accuracy suffers.

From circuit theory, we know that many of these problems can be mitigated through the introduction of a resonator – every circuit designer knows that an LC oscillator is generally much better than an RC relaxation oscillator. The introduction of a resonator into clocks began with observations by Galileo. By 1602, he had deduced important facts about a free pendulum's motion. In a letter that year to his patron, Guidobaldo del Monte, Galileo described experiments that revealed an independence of oscillation period on the mass of the pendulum. Within his limits of measurement precision, he concluded that the period is similarly independent of amplitude, and only a function of length [8].

The Dutch astronomer Christiaan Huygens later performed a careful theoretical analysis, and realized that Galileo was somewhat in error: In truth, amplitude does matter. However, this same analysis revealed the result now taught in every elementary physics class: For "small enough" angular displacements, the period of oscillation is indeed a function only of length. From there, it is a short intellectual step to exploit the near-isochrony of the pendulum to enable better clocks. Huygens himself took that next step, allegedly inventing the pendulum clock on Christmas Day, 1656 by proposing the replacement of the aperiodic weighted foliot with the resonant pendulum. Not being an instrument-maker himself, he had the clock built in 1657 by someone who was: Salomon Coster, whose clock now resides at the Boerhaave National Museum of the History of Science, in Leiden. Clocks of that type are capable of errors measured in minutes per day, representing an order-of-magnitude improvement over the older verge-and-foliot clocks. Huygens described these developments the following year, in his much-celebrated *Horologium Oscillatorium* [9]. In short order, clocks all over Europe were being upgraded by replacing foliots with pendulums.

The superiority of the pendulum highlighted deficiencies in the rest of the clock mechanism by contrast. The largest remaining error source was the very large swings forced on the pendulum by the legacy verge escapement. The amplitudes were somewhat in excess of the 90-degree spacing of the palettes, and thus well outside the "small-swing" regime that corresponds to near isochrony. Conscious realization that

this problem limited further improvements stimulated the development of better escapements. The first of these was by Robert Hooke, who developed the *anchor escapement* the same year that Coster built Huygens' clock [10]. It was the first important innovation in escapements in the 300-year history of the technology. By reducing swings by an order of magnitude, stability was improved by about an order of magnitude as well. Errors were now denominated in tens of seconds per day. A mathematical analysis of the escapement would finally be carried out by Astronomer Royal George Biddell Airy in 1830 [11]. Interest in how escapements function remains high, with modern treatments continuing to appear in the literature [12].

The length-dependent periodicity of the pendulum clock produces a sensitivity to the temperature coefficient of expansion of the materials used. George Graham of England introduced the idea of using a combination of metals to reduce the overall temperature coefficient, and by 1721 had improved accuracy yet another order of magnitude. Errors were now of the order of a second per day [13]. Not long after, a carpenter named John Harrison began to elaborate on Graham's compensation ideas, and supplemented those with compensation also for motion. By 1761, the self-taught horologist bettered Graham by achieving errors of 250ms a day, and in a shipboard installation, no less. Miraculously, Harrison was eventually able to shrink the mechanism to pocketwatch dimensions (Fig. 4). By famously solving "the longitude problem" Harrison revolutionized the art of navigation [13].

Figure 4 – Harrison's final chronometer, the H5 (Wikipedia: John Harrison).

For the next 150 or so years, further improvements were aimed at reducing frictional losses to their absolute minimum values through a combination of lubrication and the use of better materials. Escapements underwent a continuing evolution to reduce the duration and surface area of metal-metal contact. Eventually, damping by air became a limiting factor, and so the best clocks were operated in a vacuum. Finally, the tiny energy required to operate an indicator came to dominate the remaining loss, and so William Shortt devised in 1921 a master-slave arrangement of two weakly-coupled pendulums. The slave shouldered the burden of driving an indicator, while the master pendulum suffered only its own infinitesimal frictional losses and a tiny coupling energy as dissipation. The slave pendulum acted as a phase-locked buffer between the master oscillator and the load. Shortt's free-pendulum clock was so precise and stable that it enabled the discovery of the earth's own rotational instability [4]. After more than 600 years of steady development, artifice had finally bested nature.

Piezoelectricity

Shortt had pushed the art of mechanical engineering beyond all reasonable expectations. Any additional major improvements would have to come from elsewhere. Additionally, a growing demand for accurate personal timepieces would force continued innovation in still different areas as well. Fortunately, a decades-old discovery by Pierre Curie and his brother Jacques in 1880 would shortly develop into a technology that would advance horology on several fronts.

During a study of pyroelectricity (in which heating induces electrostatic polarization in certain crystalline solids), the brothers Curie had found that mechanical stress would also induce polarization in these crystals; they had discovered *piezoelectricity*. Among the piezoelectric materials they identified was quartz [14].

Not long after the Curies announced their discovery, their colleague at the Sorbonne, Gabriel Lippmann, argued on thermodynamic grounds that the converse effect should exist [15]. The Curies soon verified that applying a voltage across the crystal did indeed cause mechanical deformation. Lippmann would remain important to the Curies, becoming Marie Sklodowska's thesis advisor a decade hence.

Piezoelectricity remained the object of purely scientific study for almost 40 more years. That changed with the outbreak of the First World War in 1914. The need to detect enemy submarines led Paul Langevin, a former student of Pierre Curie, to devise a sonar system using quartz ultrasonic transducers [16]. The war ended before the invention could be put into service, but the utility of piezoelectric technology was now firmly established.

Langevin was not alone in pursuing the development of sonar. In the United States, Walter G. Cady had developed a sonar system that used piezoelectric crystals made of Rochelle salt. As had happened to Langevin, the Armistice was signed before Cady's system could be used. The experience nevertheless stimulated a fascination with piezoelectricity, and Cady continued his research at Wesleyan University after the war. In the years immediately following the war, he discovered resonant phenomena in piezoelectric crystals, filing a patent for the resonator in 1920 [17].

He was the first to generate the now-familiar electrical model for a crystal, in which a series-RLC circuit is shunted by a capacitance. In short order, Cady developed an oscillator based on insights facilitated by this model (Fig. 5) [18].

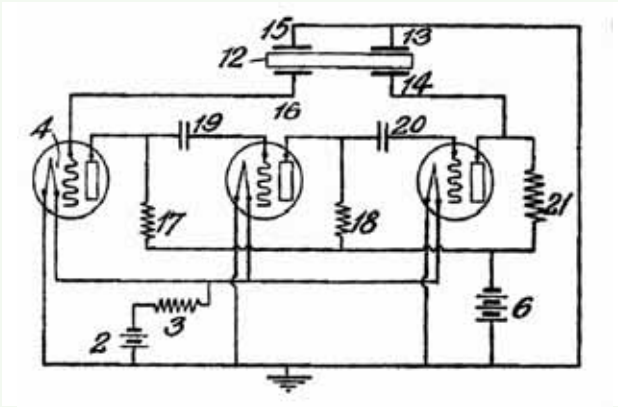

Figure 5 – Two-port crystal oscillator (from Cady's patent application [18]).

Cady's work caught the eye of George Washington Pierce, an acquaintance who was teaching at Harvard. Cady graciously demonstrated his two-port oscillator to Pierce, who then devised a simpler oscillator that required only one vacuum tube and a one-port crystal resonator. The Pierce oscillator has been a standard circuit block ever since (Fig. 6) [19].

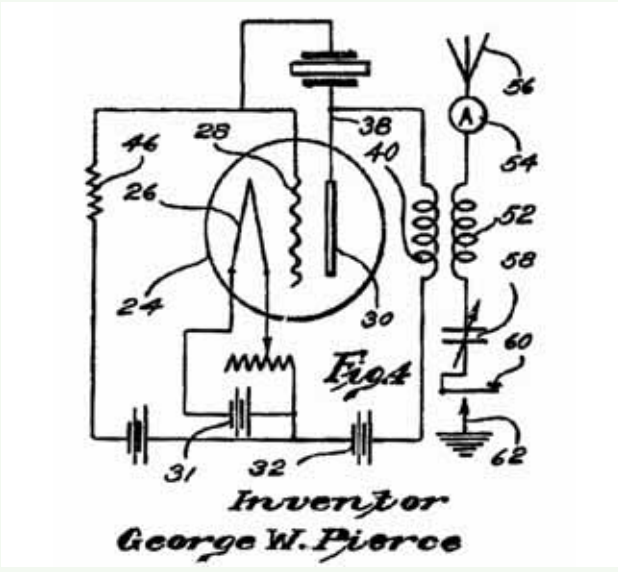

Figure 6 – First published schematic of a Pierce oscillator (from Pierce's patent [19]).

Both Cady and Pierce were motivated by the need for frequency-stable oscillators in the nascent radio art. Standard LC oscillators were hard-pressed to maintain frequency within a 1% tolerance band. Quartz-controlled oscillators are at least a hundred times more stable, an attribute equally valuable for transmitters and clocks.

"It Doesn't Tick – It Hums!"

Aside from renewing interest in piezoelectric technology, the First World War produced a generation of soldiers who relied on wristwatches instead of the less-practical pocket watches that had previously been in fashion. Consumer demand for wristwatches grew steadily in the postwar years, and watch manufacturers responded to the growing interest. By the end of the Second World War, wristwatches were a commonplace item.

The invention of the transistor made it inevitable that watches and clocks would eventually benefit somehow. The first company to put an electronic watch into production was Bulova, an American company with facilities in Switzerland. Swiss employee Max Hetzel received permission in 1952 to begin research on his ideas for what would be called the Accutron – a wristwatch based on an electromagnetic *tuning fork* as the resonant element. Oscillation would be maintained by placing the tuning fork in the feedback loop of a single-transistor circuit. In early 1953, Raytheon delivered a few CK722 germanium alloy transistors, and Hetzel started work in earnest. Within a year he had a working prototype with a 5cm fork oscillating at 200Hz. His Swiss colleagues were not terribly impressed, and Hetzel eventually moved to Bulova's New York headquarters to continue work on the project [20]. Working closely with fellow employee William Bennett, the fork was shrunk to fit within a typical wristwatch, with a resulting resonance at 360Hz. Each Accutron coil was wound with 8000 turns of 15μm-diameter insulated copper wire, conveying some idea of the manufacturing challenges that they had to overcome. An exploded view of a second-generation Accutron is shown in Fig. 7.

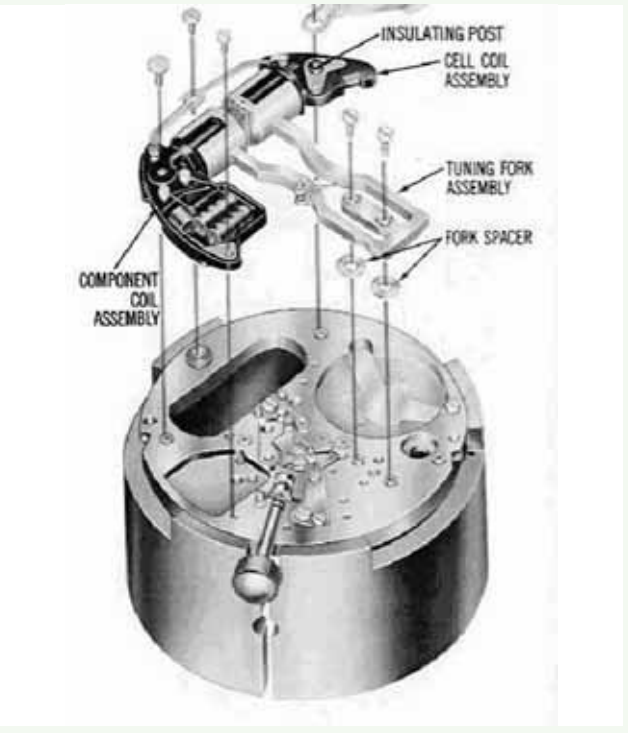

Figure 7 – Exploded view of Accutron model 218 [21].

The first Accutrons were offered for sale in November of 1960, just in time for the Christmas shopping season. The 360Hz vibration of the tuning fork was quite audible, and Bulova chose to highlight this characteristic as a feature: "It doesn't tick – it hums!" Jim Williams of Linear Technology notes that "if you left an Accutron on a glass coffee table in a quiet room, the hum would drive you nuts."

"It Doesn't Hum – It Squeals!"

The accolades that Bulova enjoyed for having developed the Accutron, as well as their steadfast refusal to license Hetzel's patents [22], contributed to the formation of CEH in response. It also spurred the Japanese into action as well. Seiko's head of R&D, Nakamura Tsuneya, started a secret project in reaction to the Accutron's announcement [23]. Rejecting the electromagnetic tuning fork resonator (which was patented by Bulova in any case), Seiko chose instead an 8192Hz quartz crystal as the resonator, just as CEH had. Because Seiko lacked an IC capability at that time, the circuitry in the "Astron" was fully discrete, consisting of 76 transistors, 29 capacitors, 83 resistors and a smattering of other components. This collection of components was painstakingly hand-assembled.

Prototype Astrons competed with CEH's Beta prototypes at the 1967 Concours. Although CEH swept the top 10 spots. Seiko won two of the next three places, so it was a complete sweep for quartz technology. The triumph was so complete, in fact, that the Concours was suspended in mid-1968, then cancelled forever; quartz and electronics had taken the charm out of the contest [4].

Manufacturing Astrons must have been a nightmare; the difficulties undoubtedly explain why only 200 of the watches were ever offered for sale. The high initial price of $1250 – roughly that of a compact car at the time – also strongly suggests that the Astron was more of a marketing experiment than an earnest attempt at production. Seiko did get to enjoy some bragging rights, however, for their introduction of the Astron on 25 December 1969 made Seiko the first company in the world to offer a quartz electronic watch for sale on the open market. Watches based on CEH's Beta21 (for "Beta2, version 1") module went on sale the following April. Unlike the Astron, the Beta21 module was intended for high-volume production, thanks to the IC technology developed by Eric Vittoz and his CEH colleagues [24].

Once the "IC genie in the bottle" had been released, there was no turning back. Swiss-born Jean Hoerni, who had invented the planar process at Fairchild, left to found Intersil in 1967 with the partial backing of Swiss companies. Two years later he returned to his homeland to ask for $75,000 to make CMOS ICs for the watch industry. Rebuffed, he flew onward to Japan, where he met with Hattori Shoji, the chairman of Seiko, who signed an agreement with Intersil on the spot [23]. Thanks to the growing IC industry, a few short years would be enough to turn electronic watches into a throw-away commodity.

Up to 1970 or so, these new electronic watches still had traditional analog displays. The Hamilton Watch Company took out ads in the spring of 1970, announcing the Pulsar all-digital LED watch, largely as a market research exercise. The reaction was wildly enthusiastic, but engineering difficulties forced them to delay taking orders until March of 1972. They set the initial price at $2100, knowing that Roger Moore would be sporting a Pulsar in the upcoming James Bond film, *Live and Let Die*. The Pulsar finally began shipping in 1973.

The same year that Hamilton started taking orders, Motorola began offering CMOS-based watch electronics to all comers for $15, and the watch business went into a frenzy. Intel, worried that they might miss one of the Next Big Things, bought a company called Microma Universal in 1972 to get into the watch business. The disastrous result motivated Intel to sell off the Microma division at a considerable loss only five years later [25].

As the cost of the electronics plummeted, the resonator remained a sore spot because of its lack of scaling. The 8192Hz resonators were somewhat bulky, constraining case size, and were also somewhat expensive. A breakthrough in resonator design was announced in 1973, when Juergen Staudte of

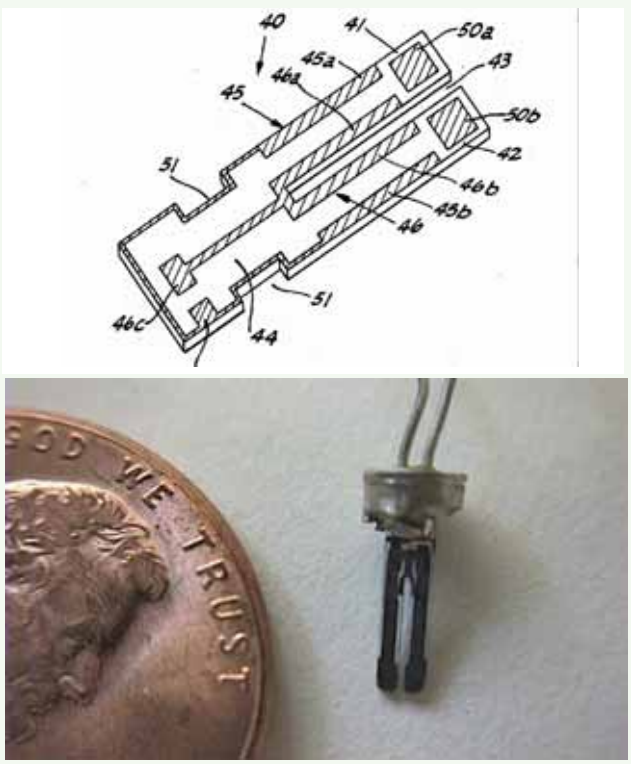

Figure 8 – Quartz tuning fork resonator of Juergen Staudte [26][27]; typical unit shown on bottom with cover removed (photo credit: Erhard Schreck)

Statek described his quartz resonator [26]. By creating an electrostatic version of a tuning fork, Staudte was able to shrink dimensions dramatically (Fig. 8). Additionally Staudte introduced photolithographic batch-processing techniques to quartz resonator manufacture, including laser trimming, allowing the same economies of scale enjoyed by the IC business. Statek even offered a transparent glass package option that allowed laser trimming on packaged resonators. Thanks to Staudte's brilliance, a compact, inexpensive, but accurate resonator could oscillate at 32.768kHz. This frequency has since become the standard frequency for clocks, including those found inside desktop and laptop computers.

The compounding effect of all of these advances was a boon to consumers, for now anyone could afford a watch whose accuracy was undreamt of only a few years earlier. By the time of Intel's sale of Microma, LED watches were selling for under $10, and LCD watches would soon follow suit.

"What's Next?"

Even the most inexpensive wristwatches available today are so precise that the need for even better stability no longer drives their evolution. Other factors, such as esthetics, generally matter more to consumers now. The electronics revolution has continued unabated over the four decades since the Beta21 was introduced, so the ability to integrate ever more functions per unit volume explains why many watches are becoming multipurpose information appliances. Wristwatches that are also PDAs, infrared remote controls, pagers, radios, TVs, walkie-talkies and MP3 players have all appeared on the market at one time or another. The primary constraint on adding even more features is the power consumed by all of these functions. The low-power tradition that Eric Vittoz established will only strengthen as engineers struggle with the constrained power budgets of a wristwatch form factor.

And for those consumers who *are* obsessed with accurate time, the ability to communicate with GPS satellites can endow a watch today with traceability to an atomic standard. One can only hope that it would maintain a better accuracy than that lobby clock Max Forrer's wristwatch bested in 1968.

Acknowledgements

The author is grateful to Byron Blanchard for calling attention to Airy's analysis of the escapement; to Jim Williams of Linear Technology for relating his experiences with the Accutron; and to our polymath editor, Mary Lanzerotti, for her literary and technical inspirations.

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About the Author

Thomas H. Lee received the S.B., S.M. and Sc.D. degrees in electrical engineering, all from the Massachusetts Institute of Technology in 1983, 1985, and 1990, respectively.

He joined Analog Devices in 1990 where he was primarily engaged in the design of high-speed clock recovery devices. In 1992, he joined Rambus Inc. in Mountain View, CA where he developed high-speed analog circuitry for 500 megabyte/s CMOS DRAMs.

He has also contributed to the development of PLLs in the StrongARM, Alpha and AMD K6/K7/K8 microprocessors. Since 1994, he has been a Professor of Electrical Engineering at Stanford University where his research focus has been on gigahertz-speed wireline and wireless integrated circuits built in conventional silicon technologies, particularly CMOS.

He has twice received the "Best Paper" award at the ISSCC, co-authored a "Best Student Paper" at ISSCC, was awarded the Best Paper prize at CICC, and is a Packard Foundation Fellowship recipient.

He is an IEEE Distinguished Lecturer of the Solid-State Circuits Society. He holds 43 U.S. patents and authored "The Design of CMOS Radio-Frequency Integrated Circuits" (now in its second edition), and "Planar Microwave Engineering", both with Cambridge University Press. He is a co-author of four additional books on RF circuit design. He is a founder of Matrix Semiconductor (now part of Sandisk) and ZeroG Wireless.

History of the Development of Swiss Watch Microprocessors

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Abstract

The history of watch microprocessors is very interesting; on one hand microprocessors today are very well-known and widely used in most personal computers, PDA and self-phones, and on the other hand, microprocessors for electronic watches are very different from those used in personal computers. So the history of the evolution of watch microprocessors has been very different compared to the history of general purpose microprocessors. In addition, this history of watch microprocessors is a very "Swiss" or "Neuchâtel" story, a completely unknown story, and consequently an interesting piece for contributing to the history of sciences and techniques.

Index Terms

Microprocessors, electronic watches, integrated circuits, CMOS, history of sciences and techniques.

I. Introduction

The first microprocessor, called 4004, has been designed and fabricated by Intel in 1971 [1-4]. But some time was necessary to see this new component go through Atlantic Ocean, also perhaps because Intel has not fully understood what they have invented! In 1974, microprocessors became a hot topic in Europe, resulting in many conferences and seminars. It is not sure that speakers have really understood what they were speaking about, and it was difficult to find in their talks the simple and final truth, i.e. a microprocessor was a very simple computer on a single chip! It was nevertheless sure that non scientific people did not understand a bit of microprocessors; to announce a Workshop at EPFL, Switzerland, about this topic, newspapers have written: "the arrival of micro-compressors"! During such conferences, people asked us frequently if microprocessors could be useful for electronic watches. The answer was always: "no, for what purpose?" It was true that at the time, electronic watch circuits were simply a quartz oscillator and a divider chain to produce a 1 Hz signal driving a step motor. A microprocessor was not required for such a task. The second reason was typically Swiss: a very big tradition of secrecy in the Swiss watch industry.

First Work about Watch Microprocessors

In 1975, at Neuchâtel, we were already thinking that a microprocessor could be very useful for a watch. A very small project was initiated at CEH (Centre Electronique Horloger) to discover what a microprocessor was [5] and to evaluate if we could design such a component. In 1978, a working group called « Processor Group » is started with people from CEH (C. Piguet, J-F. Perotto), University of Neuchâtel (J-J. Monbaron, N. Péguiron), EPFL (E. Sanchez, A. Stauffer) and from some Swiss watch companies (J-P. Wattenhofer, Asulab). The goal of this Processor Group was to propose many different watch microprocessor architectures, aiming at very low power, and to compare them. This work produced many original ideas and microprocessor architectures, as it is reported in many publications [6-12]. The proposed microprocessors are very different form the conventional architectures due to the requirements in terms of power consumption. First, the proposed architectures are very simple, and with less hardware, one can save some power. By the way, we were very surprised to see that conventional 8-bit Intel microprocessors have to execute many instructions even for very simple tasks, such a +1 in seconds register, +1 in minutes register in case of overflow, +1 in hours register and so on. Such a task required hundreds of executed instructions, with a large penalty in power consumption. Our conclusion was that such microprocessors were too complicated for a watch microprocessor.

We were influenced by the work of Prof. Daniel Mange at EPFL on Binary Decision Machines (BDM) [13-15]. Such a machine has basically only two different instructions, i.e. an **if** or a test instruction and a **do** instruction. The test instruction allows testing an input through the test multiplexer located at the bottom of Fig. 1. If the input value is "1," the binary machine will execute a branch (or a jump), otherwise the next instruction will be executed. The other **do** instruction allows executing an operation, i.e. to send a control word to an execution unit not shown in Fig. 1. The instructions or the program are memorized in a memory, which is generally a Read Only Memory (ROM). The Program Counter (PC) is incremented through a +1 incrementer (Fig. 1). The stack allows implementing subroutines by memorizing the return address on top of this stack. The binary decision machines are in fact a "bridge" between Boolean logic and very simple microprocessors. In our case, they were very interesting for their performances in low power consumption due to their simplicity. Instead of having hundreds of instructions executed for simple tasks, we will have only tens of instructions.

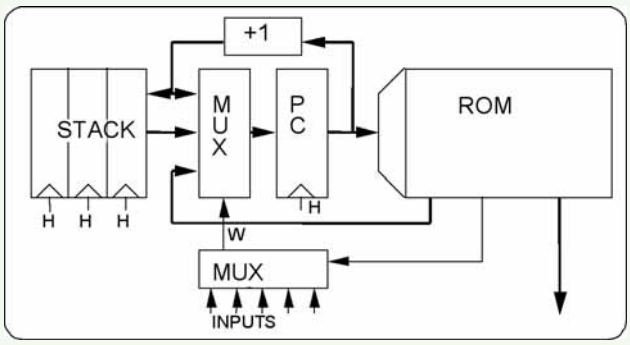

Fig. 1. Binary Decision Machine (BDM)

So we designed our first watch microprocessors along the principles of binary decision machines. A very nice characteristic of these first watch microprocessors designed in 1979 and 1980 [6-12] was an instruction format as a single long word, unlike conventional microprocessors of that time that present multi-bytes instructions. This multi-bytes format was due to the memory organization in bytes.

The single word instruction format has been by the way rediscovered in 1981 for RISC machines (Berkeley and Stanford) that also take the opposite tack of existing complex CISC machines and result in simpler microprocessors. Alternative to complexity was obviously simplicity; single word instruction format, less instructions, instructions executed in one clock cycle, load/store architectures, hardware control unit. This single word instruction format was indeed the format used for the first big computers at the end of World War II. So for these watch microprocessors, we have rediscovered single word instruction format and therefore RISC machines before the RISC revolution coming from Berkeley and Stanford.

Analysis has shown that the number of clock cycles for watch software embedded in our watch microprocessors was about 100 clocks. For an Intel 8048 microprocessor, it was about 2'000 clock cycles for the same watch program. These watch microprocessor architectures have been presented in [12]. Four of these architectures have been designed by four members of the "Processor Group," and they are compared in the paper. These four architectures have 12 to 18-bit single word instructions and instruction sets containing 6 to 20 different instructions (they were really RISC or Reduced Instruction Set Computers). Some of these architectures perform the incrementation (+1) in software and therefore does not require a hardware incrementer. The main characteristic of these architectures is the very small number of executed instructions for executing a watch program, from 28 (one clock per instruction) to 252 (several clocks per instruction). As consumed energy is proportional to the number of executed clocks, the most energy efficient architecture we have presented in [12] was about 70 times more efficient than the Intel 8048. Most of our architectures could be implemented with about 20'000 transistors. But we have to say that 20'000 transistors in a 6 micron technology used at that time was about 50 mm^2 of silicon area, a very big chip.

The First Watch Microprocessors

After these more or less theoretical results, our future was to face reality. The CEH, as leader of this "Processor Group," was asked by several watch customers to develop electronic watch circuits comprising watch microprocessors. Several circuit developments were started more or less successfully. The first problem we have to face was the development time. Suddenly, processor–based watch circuits reach 20'000 transistors including embedded memories, while previous processor-less circuits were around 2'000 transistors. So the development time was largely under-estimated, not so much for the circuit architecture and detailed transistor circuits, but for the design of the layout that was still designed fully manually. So 50 mm^2 of layout was really a huge task. In fact, we hit a complexity barrier with the available CAD tools we have at that time. At debriefing time, we try to estimate and to compute layout productivity, that was a surprising low 5 to 10 transistors per day, but it was the case for any chip in any company at that time. So our problem was only under-estimation of the effort.

A first CEH project, called Silvermoon, was stopped, partially due to big delay and cost increase, but also due to the fact this circuit was designed for a watch with a digital display. And finally, Swiss watch makers preferred to have analog displays even for electronic watches, unlike inexpensive Japanese watches. This story could be compared to the cathedral Sagrada Famila in Barcelona, which is not yet finished, facing also a complexity barrier 125 years ago when it was started. The design of these watch microprocessors were too complex for the CAD tools we have at that time, and we did not search for an adapted design methodology to compensate for these tools weaknesses.

A second project aimed at developing what is the first CEH watch microprocessor, called Combo [16, 17], realized for the Delirium Tremens watch of ETA (Swatch Group). The main architect was J-F. Perotto (CEH). The instructions were 16-bit wide, data 7-bit wide (4 bits for BCD coded units and 3 bits for the tens 0-5). The instruction set was very small and contained only 12 instructions. The ROM memory was storing 800 instructions and data memory (SRAM) 16 words of 7 bits. The processor core was about 2'000 MOS, but the complete circuit including memories and numerous watch peripheral circuits (LCD driver, step motor driver, time base) was about 20'000 transistors (Fig. 2).

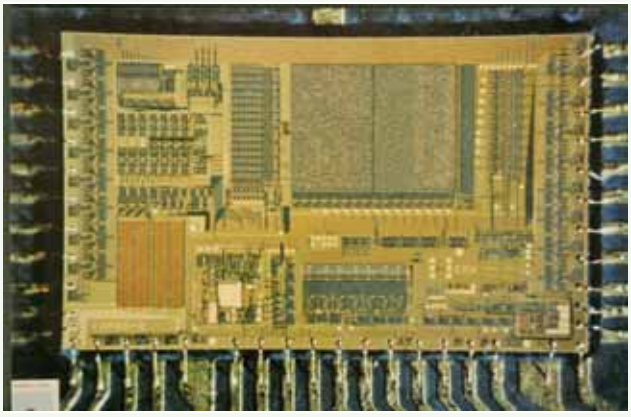

Fig. 2. The first watch microprocessor called Combo in 1982

The CEH microelectronic technology used was a 6 micron CMOS. The circuit was about 40 mm2. Supply voltage was very low at 1.5 Volt and power consumption was already very small to 0.4 µA at 16 kHz.

A second watch microprocessor called Beta 32 was designed by Michael Ansorge and co-workers at CSEM (CSEM was founded in 1984 joining CEH together with other labs). The instruction set of this machine was 20 instructions of 17 bits and data words of 6 bits. The complete circuit was about 24'000 MOS [18]. Subroutines were implemented in software, to remove some hundreds of transistors. The used technology was a CSEM 4 micron technology. So the silicon area was only 20 mm^2 and its power consumption still 0.4 mA at 1.5 Volt. Many other watch microprocessors for various electronic watches were designed in the following years, such as a chronograph for ETA with 35'000 transistors [20], a pager watch circuit [21] and some others with circuits up to 100'000 MOS. A research project was defined at CSEM in 1988 for studying parallelism and multiprocessors in watch circuits, as it is known that larger parallelism allows a supply voltage reduction for a same throughput and consequently a power consumption reduction [22-24].

Competitors [9] at that time were many companies such as AMI, Eurosil, Motorola, Intersil, Hewlett Packard, Intel, Mitsubishi, National, RCA and Sharp. They proposed watch microprocessors with power consumption in the range of 1 to 50 µA at 1.5 Volt, most of them consuming more than 4 or 5 µA, so 10 to 100 times what we have obtained at CEH/CSEM. Electronic and digital watches market has grown significantly from 1975. This market was very profitable during some years but was hit by a deep depression [19]. In January 1976, TI was selling a LED watch with 5 functions for $19.95. For Christmas 1976, a similar watch was $9.95. By 1977, the price of digital watches had fallen from more than 100$ to less than $10 in just two years. Profits evaporated. Once again as with calculators, there were only three real survivors: again, two Japanese competitors, Casio and Seiko, and Texas Instruments [19]. Twenty years later, Intel chairman Gordon Moore still wore his ancient Microna watch (my $30 million watch, he called it) to remind him of that lesson. So Intel leaves this market very rapidly.

The explosive rise and fall of the digital watch market (the same for calculators) was largely due to a brilliant but dangerous strategy of Texas Instruments. TI was a risk-taking, rich company, ready to lower prices of TI electronic watches to kill its competitors. But, ultimately, TI found itself with lines of watches whose prices had been driven so low by the fierce competition that they were not the giant profit generators they had been expected to be. Worse, the market was wide open to those survivors with low labor costs, i.e. the Japanese Seiko and Casio. Those firms soon did to TI what TI had done to its American competitors [19] and TI was forced to leave this market.

The "Punch" Project (1990-1993)

PUNCH is the name of the watch microprocessor designed by CSEM in early nineties with C. Piguet as project leader. Swiss watch makers, shareholders of CSEM, have decided to have a common Swiss watch microprocessor that can be used for every Swiss electronic watch. It is obviously more economical for time to market reason to re-use the same watch microprocessor rather than to re-design a new microprocessor for each new watch. Another strategic reason was to have a Swiss microprocessor instead to buy some Japanese or US microprocessors. Swatch Group (it was called SMH at this time) has decided to be completely independent by not buying Japanese microprocessors for its Swiss watches.

The choice of the Punch architecture was to use a multitask principle shown in Fig. 3 [24-28].

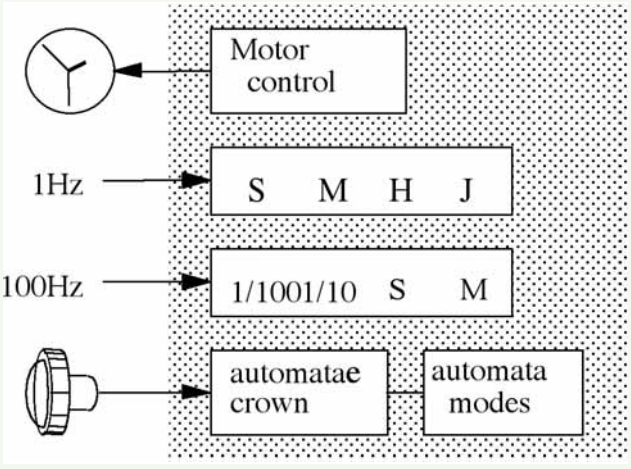

Fig. 3. Multitask Principle

It allows the definition of several independent tasks that will be executed in pseudo parallelism. Fig. 3 describes four independent tasks in a watch program,

i.e. time update every second, chronograph up date every 100 Hz, crown management to select another mode and finally step motor management. The latter could be very long if minutes hands have to move for a 60 minutes range. The originality of the Punch microprocessor consists in the fact that these independent tasks are executed in pseudo parallelism, i.e. by executing sequentially one instruction of each task. This is interesting for reactivity: as soon as a task is started, first instructions of this task are executed, and it is not necessary to wait for the termination of an already running task. In addition, it is possible to define one to four tasks and therefore to define also a conventional monotask microprocessor if "one" task is selected at starting time. The Punch microprocessor presents 103 assembly instructions of 18 bits with 8 bits data. The core itself has 11'000 MOS and the complete watch circuit with embedded memories about 150'000 MOS. Its figure of merit in MIPS/watt (MIPS: millions of instructions executed per second) is 800 MIPS/watt. Fig. 4 shows the test chip of this Punch-based circuit designed mainly by J-F. Perotto and C. Lamothe. It has been used for many Swatch electronic watches such as the Tissot Two Timer (Fig. 5).

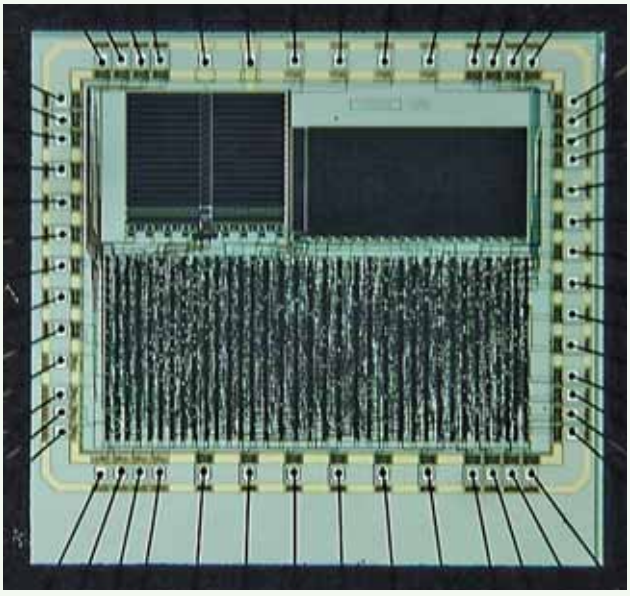

Fig. 4. Test chip of the Punch microprocessor (1993)

The CoolRISC

In 1994-1995, CSEM has developed a new microprocessor called "CoolRISC" [29-32]. The main architects were J-M. Masgonty, C. Arm and S. Durand. The goal was to design a microprocessor with the lowest possible power consumption by using low power techniques such as pipelining, gated clocks, etc… This microprocessor had about 20'000 transistors (Fig. 6) and it consumed about five times less than the Punch. This new development was motivated by the need to lower even more the power consumption and also by the fact that the Punch was proprietary of the Swiss watch makers. This was a limitation to the CSEM freedom to license a low power microprocessor to its customers.

Fig. 5. Two Timer Watch from Tissot with a Punch-based circuit

This microprocessor was really a successful design. Powerful instructions, gated clocks (not to clock blocks that have nothing to do), RISC-like machine, a 3-stage pipeline, one clock per instruction instead of about 15 for old microprocessors, these efficient techniques have been applied to this CoolRISC. These techniques were simple and known, but it was the first time that they were applied to so simple microprocessors. The figure of merit of the CoolRISC is 100'000 MIPS/watt for the core only (about 20'000 transistors) in a 0.18 micron technology. This is about 10 or 15 times better than most of 8-bit microprocessors available on the market.

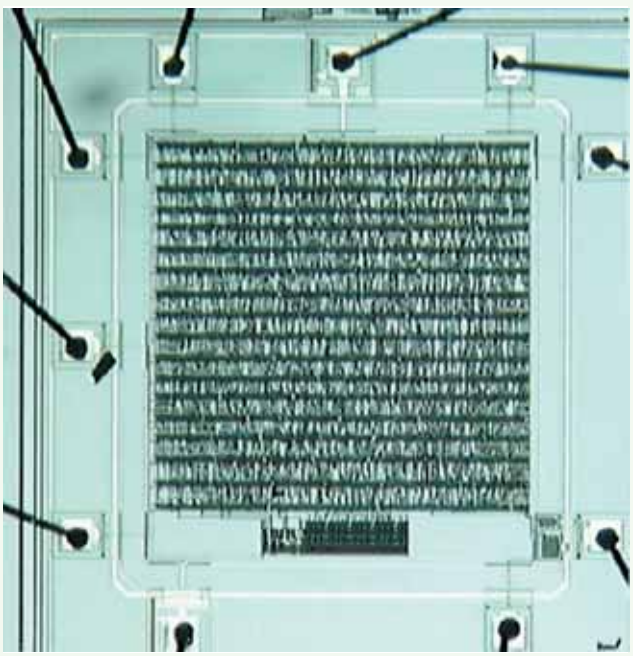

Fig. 6. Test chip of the CoolRISC microprocessor (1995)

Conclusion

Some papers mentioned the huge impact of the watch industry on the development of the microelectronics in Switzerland [33] after the invention in Switzerland too of the first quartz watch [35]. One can say the same thing for the microprocessors in Switzerland, as the first Swiss microprocessor has been developed for watch circuits, as shown in this paper, largely before they have been used for many other different applications also requiring very low power consumption. Nevertheless, new challenges still do exist [34], but the development of low power microprocessors remains and will remain a must for the design of low power circuits used in many portable products like watches but also hearing aids, self-phones, wireless sensor networks and so on. CSEM continues to develop microprocessors, more specialized such as Digital Signal Processors (DSP) like MACGIC [36, 37] or icyflex (DSP + 32-bit microprocessor).

It is also interesting to appreciate the computation power provided worldwide by all the electronic watches. Recently, the following question was asked: what is the largest unused computation power in the world? D. Lando, Lucent Technologies, answered that it was the totality of electronic watches [38]. According Lando, his Lab is seriously thinking how to use this huge unused computation power!!

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About the Author

Christian Piguet (M'03) received the M. S. and Ph. D. degrees in electrical engineering from the Ecole Polytechnique Fédérale de Lausanne, respectively in 1974 and 1981. He joined the Centre Electronique Horloger S.A., Neuchâtel, Switzerland, in 1974. He is now Senior Manager at the CSEM Centre Suisse d'Electronique et de Microtechnique S.A. He is presently involved in the design of low-power low-voltage integrated circuits in CMOS technology, including design methodologies, microprocessor architectures and logic design. He is Professor at the Ecole Polytechnique Fédérale Lausanne (EPFL), Switzerland, lectures in VLSI and microprocessor design at the University of Neuchâtel, Switzerland and in the ALaRI Master at the University of Lugano, Switzerland. He is also a lecturer for many postgraduates courses in low-power design.

Christian Piguet holds about 30 patents in digital design, microprocessors and watch systems. He is author and co-author of more than 200 publications in technical journals and of books and book chapters in low-power digital design. He has served as reviewer for many technical journals. He is member of steering and program committees of numerous conferences and has served as Program Chairman of PATMOS'95, co-chairman at FTFC'99, Chairman of the ACiD'2001, Program Co-Chair of VLSI-SOC 2001 and Program Co-Chair of ISLPED 2002. He has been Low-Power Topic Chair at DATE 2004-2006. He is Special Session Chair at DATE 2007.

Eric Vittoz and the Strong Impact of Weak Inversion Circuits

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By the late 1960s, several people had noticed that the so-called "threshold" of MOS transistors was not a threshold after all, and that drain current continues to flow even when the gate-source voltage is lowered below that threshold value. This "leakage" current was found to be due to diffusion in a weakly inverted channel, and to depend exponentially on the gate voltage [1-3]. Investigations were initiated, to see if the impact of this current can be eliminated or at least limited, particularly in dynamic memories. Eric Vittoz got to thinking instead how this current can be used in analog circuits.

Ten years after Eric first measured devices in this "weak inversion" region, the now classic Vittoz and Fellrath paper [4] came out. In it, we learned what Eric and his colleagues had been up to all this time: They had meticulously characterized devices operating in the weak inversion region, and had developed models for them; they had also developed a variety of circuit building blocks that not only could operate in this region, but actually exploited the exponential characteristics in it. Their killer application was the electronic watch, which stands to reason, given that they were working at CEH, the Centre Electronique Horloger (the research arm of the Swiss watch industry) in Switzerland. The first wristwatch containing weak inversion MOS circuits appeared on the market in 1975. But it was clear from that terrific paper that the techniques described in it did not have to be limited to the electronic watch; in fact, by now they have been used in a score of low-voltage, micropower applications, such as biomedical devices, hearing aids, pagers, sensor interfaces, motion detectors for pointing devices, and a variety of portable instruments. That paper taught the design community how to design with low voltage (1 V, three decades ago!) and low current (nanoamps!). There weren't many analog MOS circuits at the time to compare this feat to, but the few that existed typically operated with supplies from +-5 V to +-15 V, with currents typically in the milliamps.

The proposition to design analog circuits biased in weak inversion was such a drastic departure from the norm, that at the time many doubted that this could be done reliably. In fact, for many years it was not uncommon after a technical presentation discussing circuits operating in weak inversion, for someone in the audience to question whether such operation is reliable, unaware of the fact that the circuits in his/her own wristwatch were operating in weak inversion!

Eric had done important work on micropower circuits before that time, notably on frequency dividers, using both MOS and bipolar transistors. Similarly, he did important work since, in a large variety of circuits and systems, including sensors and bio-inspired circuits. But such work cannot be summarized, or even adequately commented on, in this limited space. So, in this article, I will focus on his innovative work on weak inversion devices and circuit building blocks. Rather than limit this article to praising Eric, I will also take this opportunity to speculate on what it is that makes it possible for a person to be as creative and impactful as Eric has been. And, being an educator, I will not resist the temptation to also comment on what Eric's example may suggest, as to how we should be educating our students.

When you first meet Eric, what strikes you is his energy. If you attend one of his lectures, you better be alert, or you will quickly lose the thread. His enthusiasm shines through, and is contagious. He has persistently published and publicized his results in conferences, journals, workshops, short courses, and tutorial book chapters. This enthusiasm, combined with other qualities, can make sparks fly. This brings us to Eric's other qualities.

Eric is deep. He can take a problem and dissect it until he gets to the root of it. A case in point is his meticulous analysis of the clock feedthrough problem [5, 6]; this work has been very influential in the design of a variety of circuits which use sampling, such as A/D converters and switched-capacitor filters. Closely related to the above quality is Eric's ability to get down to fundamentals, and use them to understand and optimize circuit performance. His work on oscillators is an example of this [7]. But for me personally, the work that had the most impact in this respect was his contributions to the study of fundamental limits of analog circuits [8-11]. His formulas and plots in that work, together with further discussions with him, made it abundantly clear to me why the power-speed tradeoff is fundamentally coupled to dynamic range, and how this tradeoff fares in this respect in comparison to digital. My group at Columbia has benefited from these results – they have been our guide in our search for circuits with dynamic power dissipation, in which the circuits dissipate each time only the power needed for the signal/interference situation at hand [12]. I even ended up co-authoring a detailed chapter with Eric on speed-power-dynamic range tradeoffs (and you can be sure that Eric did most of the work for it!) [11]. Eric's papers also exemplify his ability to maintain a bird's eye view – to distill what is important, and to not lose the forest for the trees [10]. This quality is something that comes, of course, with experience. It is notably absent from most students; giving them to read Eric's papers helps.

Once he has all the pieces figured out, Eric is excellent at combining pieces together to do something useful; in other words, he is creative. This quality is exemplified in his weak inversion work already mentioned. There are numerous other examples in his papers and articles, and I will refer the reader to Eric's own account of them.

Another quality of Eric's is his breadth. The center of his activities has been circuits, but he has not hesitated to delve into device modeling in order to support his circuit activity. This was already evident in the classic 1977 paper [4] mentioned above, which contains an Ebers-Moll-like symmetric model for the MOSFET, and which has evolved into the EKV model for computer-aided design [13] ("V" of course standing for "Vittoz"). To my knowledge, this was the first computationally efficient model that achieved continuous characteristics, as well as continuous derivatives, as one goes from weak, through moderate, to strong inversion; and it achieved this not just for the current, but for all quantities of interest, such as small-signal conductances, charges, capacitances, and noise. The model is notable both for the rather small number of parameters on which it is based, and for its close connection to circuit design. (I hope circuits-oriented students who ask questions like "why do we need to learn semiconductor devices" are reading this.) Another example of Eric's breadth, this one in the other direction, is his work on bio-inspired systems and vision sensors [14].

Finally, Eric is both an industrial researcher and an academic. His teaching and research activities as Professor at EPFL in Lausanne makes this clear, but even when he is not pursuing those activities, there is always a sense of an "academic" curiosity in him; he can value certain research that does not have immediate applications. Of course, the vast majority of his research did find applications, and important ones at that.

It is true that Eric happened to be in the right place (the research arm of the Swiss watch industry) at the right time (when weak inversion currents revealed themselves). He was working at a place where ideas could thrive, where the management allowed people to think and explore new directions without being constantly limited by scheduled deliverables. I have never been to CEH, but from Eric's descriptions I gather that the spirit there must have been somewhat like that at Bell Laboratories, which I was fortunate enough to experience first-hand in the late seventies during my association with them. Although of course the scale and scope of the two operations was very different, the results that came out of them have something in common: they speak volumes as to what can happen if capable individuals are allowed to do their thing, under a management that understands what research is all about. It is very difficult, if not impossible, to find such a place today. Companies rely to a large extent on universities to do the research. But if you look at what type of work they encourage and fund, it is very often too constrained and not far-reaching enough. Many of us in this field decry this, and consider its negative effects obvious; apparently, they are not obvious to all. I hope we will be proven wrong.

Coming back to Eric Vittoz – he did, indeed, find himself in the right place at the right time. But, as Louis Pasteur has noted, "chance favors the prepared mind". Indeed, Eric's mind was already prepared, and I do not mean just by biology. I believe a key to explaining his career and achievements is his having been fortunate enough to tinker as a child. In our field tinkering develops intuition, motivates further exposure, and gives tinkerers unique satisfaction, confirming that electronics is ideal for them. I am sure that Eric and many others of our generation, who were lucky enough to have tinkered as children, will support me in this claim. Sadly, today it is rare to find students who have tinkered[1].

We are fortunate to have Eric Vittoz in our midst, a researcher with a sharp and prepared mind, willing to go against odds and consider new possibilities with enthusiasm; a prolific author, eager to share his important results with the rest of the community. His contributions, rather than wearing out, are becoming even more influential with the passage of time, as low voltage and low power become increasingly important in the age of mobile devices.

A note of thanks: I would like to thank Eric for his contributions to two books for which I served as co-editor; for the pleasure of collaborating with him, albeit on only one book chapter; and for our many discussions and arguments – he still hasn't convinced me that it's better to use the substrate as a potential reference rather than the source in circuit design, but such continuing debates are part of the fun of knowing him.

[1] I have described in the February 2008 issue of this Newsletter what we are doing at Columbia to turn things around in this respect. Essentially, what we are trying to do is to make students tinker, in the hopes that we can make a few more Erics!

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About the Author

Yannis Tsividis received the B.S. degree from the University of Minnesota, Minneapolis in 1972, and the M.S. and Ph.D. degrees from the University of California, Berkeley, in 1973 and 1976, respectively. He is Charles Batchelor Memorial Professor at Columbia University in New York. His research has been in analog and mixed-signal MOS integrated circuits at the device, circuit, system, and computer simulation level, starting with the first fully-integrated MOS operational amplifier in 1975. A Fellow of the IEEE, he has received the 1984 Baker Prize Award for the best IEEE publication and the 2007 IEEE Gustav Robert Kirchhoff Award, and was co-recipient of the 2003 ISSCC L. Winner Outstanding Paper Award. He received Columbia's Presidential Award for Outstanding Teaching in 2003, and the IEEE Undergraduate Teaching Award in 2005.

continued from page 6

streams. Smaller companies do not typically have this option available to them and as such tend to keep tight focus. There is another less obvious reason for this…whatever is funded is likely to be much more important to a small company. Their attention span is necessarily limited by their market(s). Failure to provide a useful result (either positive or otherwise) can be catastrophic at both ends of the spectrum but is much more apparent at the small end.

Do You Speak IP?

Mention IP in different circles and one gets varied responses, from glazed expressions of disinterest to the wringing of hands and talk of IPO. No matter what your opinion, intellectual property is the lifeblood of collaboration and research. Nevertheless, this can be the biggest source of angst in any negotiation. IP discussions can run aground for a whole variety of reasons including (but certainly not limited to) sole right to use versus open access, single versus multiple use licences, royalty based agreements based upon volume sales, one-off costs and inferred rights transfer, indemnification issues and post sales support, to name but a few.

I am not, nor ever likely to be, a lawyer. I do, however, have experience in IP discussion. I could wax lyrical for several pages on the perils and pitfalls of IP negotiation from a non legalistic perspective. However, my advice to all interested parties is simple…be realistic! It is common for IP generators to over-value their product. On the other hand, it is equally common that IP is undervalued by the intended recipient. In a symbiotic relationship, it is important to provide incentives to all parties such that they can see a clear strategic or monetary advantage. Any agreement needs to reflect the ultimate goal of building success. It is of little use having a cast iron IP agreement if it takes millions in lawyers' fees and the target market is missed. Sometimes it is worth taking a step back to figure out the high level stakes.

Of equal importance to core IP development is post sales support. IP by its very nature is transient and needs to be refreshed and supported to maintain viability. Anyone underestimating the resources that this may absorb does so at their own risk. Some of today's most successful IP trading companies have large support groups to help end customers get the most from their product. Realistically, one should not expect academic bodies to engage deeply in this area. There is more to be gained by the commercial partner adding their value in this field. They usually know their markets very well and are usually the best people for the job.

About the Author

Tony Harker graduated from Northumbria University (formerly known as Newcastle Upon Tyne Polytechnic) with a degree in Physical Electronics in 1983. Tony has held product engineering, design engineering, design centre management, project management and director level roles at a senior level with a number of multinational IC companies.

In addition to representing IEEE SSCS as Associate Editor for Europe and Africa, Tony currently runs Scotland's Institute for System Level Integration (iSLI). This was set up in 1998 by four of Scotland's leading universities in order to enhance the industry/academic interface. In his time at ISLI, Tony has enhanced the commercial face of the organisation, increasing its international profile and its interaction with the design community.


Advances in Ultra-Low-Voltage Design

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Executive Summary

In the near future, a number of systems will be powered using energy scavenging technologies, enabling exciting new applications such as medical monitoring, toxic gas sensors and next-generation portable video gadgets. This will require electronic circuits to operate with utmost energy efficiency. The idea of exploiting weak-inversion operation for low power circuits was pioneered by Dr. Eric Vittoz in the 1960's, and has led to many recent advances in sub-threshold circuit design.

While exploring aggressive V_{DD} scaling for energy reduction, researchers discovered that the V_{DD} which minimizes energy consumption of a digital circuit often lies in the sub-threshold region. However, ultra-low-voltage design must overcome two key challenges: increased sensitivity to process variation and the reduced ratio of on to off currents in sub-threshold. In scaled technologies, exponential effects of local variation necessitate statistical design approaches and new circuits to aid low-voltage operation. In SRAMs, for example, an 8-transistor cell can significantly improve cell stability, while peripheral assist circuits enable reliable reading and writing. Furthermore, redundancy has proven to be a powerful technique for managing variation in ultra-low-voltage systems.

Powering sub-threshold systems requires energy delivery circuits that can efficiently convert a battery supply to low voltages at µW load power levels. Moreover, since the optimal V_{DD} of a circuit changes with workload and other conditions, the ability to track the optimum is crucial to maximize energy savings. A digital tracking loop can non-invasively sense the energy per clock cycle consumed by a load circuit, and then direct an embedded DC-DC converter to supply the optimal V_{DD} for minimizing energy. For micro-power systems, switched capacitor DC-DC converters can be completely integrated on-chip to efficiently provide variable supply voltages at a wide range of load power levels.

A survey of demonstration systems illustrates the significant advances made in recent years related to sub-threshold design. A few examples, among many, include an 18mV Fast Fourier Transform (FFT) processor, a high throughput motion estimation accelerator, a 0.2V flash ADC, and a microcontroller with integrated SRAM and DC-DC converter (Fig. 1). Sub-threshold SRAMs have explored a wide range of bit-cell and peripheral circuit designs. These works have addressed important issues, such as device variability, through new circuits and system architectures. To transition these concepts to products, it will be critical to develop design techniques and CAD tools to encapsulate variation-aware methodology for ultra-low-voltage design.

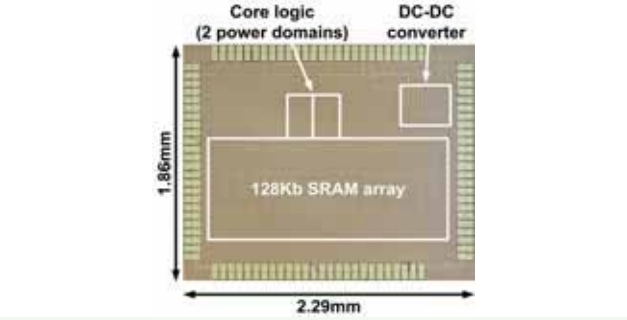

Figure 1: Die micrograph of 65nm sub-threshold microcontroller.

This Executive Summary is a preview of full coverage coming in the fall SSCS News.

Gigasensors for an Attoscope

Erik H.M. Heijne, CERN, erik.heijne@cern.ch

Executive Summary

When elementary particles cross silicon, they leave a small signal which can be used to trace them. Sophisticated silicon trackers with close to 10^9 sensor cells of 40 -100 µm dimensions are now installed in the experiments at CERN, the accelerator laboratory in Geneva, Switzerland. These systems take snapshots at 40 MHz rate, and allow to record every 25 ns the coordinates of hundreds of particles, that emerge from violent interactions between colliding beams. The purpose is to study the properties of matter in the TeV energy range, where energetic quanta interact on the 'atto' (10^{-18} m) length-scale.

The gigasensor system has to operate at high speed and in a small volume, with signal processing, temporary data storage and logic operations all integrated in chips that are a part of the detectors. It has been essential to employ low-power CMOS circuits, and these, moreover, have to withstand the ionizing radiation inherent to this application.

Around 1987, Eric Vittoz studied the basic parameters for the development of the 'pixel' particle tracking detectors, in collaboration with our team at CERN. His collaborators Christian Enz and François Krummenacher then designed the very first prototype implementation with a low noise input amplifier in each pixel, operating at low power. Subsequently, Krummenacher also implemented a clever scheme for coping with the dark current of the sensor cell, which allows DC connections at very high density: typically > 10^4 per cm^2 .

The evolution of these particle imagers now results in matrices of 256x256 pixels with >1000 transistors per pixel, as illustrated in the Fig. 1.

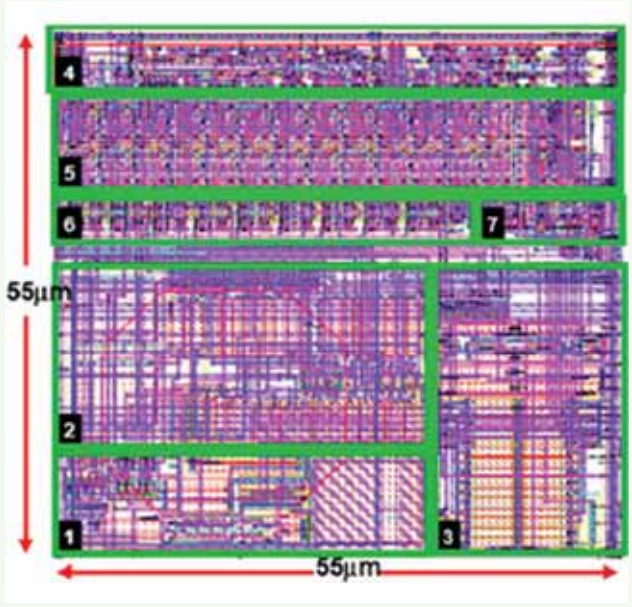

Fig. 1 Layout for the Medipix3 chip of a 55µm pixel cell in a 130 nm CMOS technology by Campbell and his team at CERN. Preamplifier, shaper and comparators, resp. 1, 2 and 3 form the analog part, while 4-7 are the control logic, counters, configuration and arbitration circuits. This pixel has more than 1080 transistors.

Such pixels can process single quanta and are designed to have connections with their neighboring cells, which allows analog and logic operations at ns time-scale for distributed events, where a single incoming X-ray quantum touches several cells simultaneously.

This Executive Summary is a preview of full coverage coming in the fall SSCS News.

1528 PROCEEDINGS OF THE IEEE, VOL. 57, NO. 9, SEPTEMBER 1969

Complementary-MOS Low-Power Low-Voltage Integrated Binary Counter

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Abstract—An integrated complementary MOS-transistor binary counter stage, particularly suited to low-power low-voltage applications, has been realized in monolithic form. The topology of the circuit allows one to group together all p-channel MOSTs and all n-channel MOSTs within two distinct surface areas. This feature results in an appreciable reduction of the surface necessary for a given circuit function. Dynamic current consumption is about 10 nA per kHz at a supply voltage of 1.35 volts. The complementary type of substrate is obtained by etching and epitaxially refilling wells in the original substrate material. Technological problems which had to be solved in order to achieve low-power low-voltage operation in complementary integrated MOS circuits will be discussed.

I. Introduction

FOR A PARTICULAR application we need a chain of more than ten binary counter stages in integrated form. While power consumption should be held at a minimum, an upper limit of the input frequency of a few hundred kilohertz is sufficient. Logic circuitry making use of complementary MOS transistors is ideally suited to this application because the power consumed is essentially proportional to the energy required to recharge the capacities of the circuit [1], [2]. This dynamic power consumption P is given by the relation $P=fCV^2$, where f is the frequency of the input signal, C is an equivalent capacity (sum of the different capacities modified by suitable weighing factors), and V is the supply voltage.

It is thus desirable to use a supply voltage as low as is consistent with reliable operation. A choice of 1.35 volts has been made also in view of using readily available mercury cells. We thus face the technological problem of fabricating complementary MOS transistors having threshold voltages[1] below the chosen supply voltage. In fact, in order to assure acceptable dynamic performance, threshold voltages around 0.8 volt are required for both p- and n-channel devices. In order to limit the static power consumption, the drain currents in the off-state of these enhancement mode devices have to be as low as possible.

Using MOS transistors with small dimensions, compatible with standard photolithographic techniques, reduces the equivalent capacity C. At the same time, chip surface is minimized and higher yields may be obtained. The realization of complementary MOS transistors in monolithic form is greatly facilitated if the topology of the circuit renders possible grouping the MOSTs of either type within two distinct surface areas. Such a circuit is described briefly in the following section.

Manuscript received January 14, 1969; revised February 21, 1969.

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[1] This threshold voltage is defined by the intercept of the extrapolated straight line portion of the $I_D^{1/2}=f(V_D \equiv V_G)$ curve with the abscissa. The customary definition of the threshold voltage, based on 10 μA drain current is not too useful when we are dealing with nanowatt circuits, as these circuits may be operated below this "threshold current."

II. Description of the Circuit

One stage of a binary counter represents a sequential logic circuit which can be decomposed into a combinational circuit and some elements of memory [3].

In order to reduce the number of MOSTs we have chosen to realize the memory functions with the help of commutation delays. By applying classical methods of synthesis of sequential circuits [3] the equations of the combinational circuit may be obtained.

$$A = \overline{DI + C\bar{I}} \tag{1}$$

$$B = \overline{DI + A\bar{I}} \tag{2}$$

where

$$C = \bar{A} \tag{3}$$

$$D = \bar{B} \tag{4}$$

and I and $\bar{I}$ are the logical input signal and its complement, respectively.

A, B, C, and D are logic variables, changing state once for each cycle of the input signal I. Equations (1) and (2) can in principle be realized by a transmission gate [4]. However, to make possible assembling all transistors of one type in one given substrate area we decided to use AND–NOR gates of the type shown in Fig. 1. One stage of the binary counter consists of two of those gates and two inverters [corresponding to (3) and (4)].

After combining certain MOSTs we arrive at the circuit shown in Fig. 2. The circuit consists of 8 pairs of complementary MOSTs. The uncritical delay functions are assumed by the commutation times of the variables A and B.

III. Fabrication Sequence and Associated Technological Problems

A. Substrate Preparation

Starting with a n-type substrate having a donor concentration of $5 \times 10^{14} \cdot \mathrm{cm}^{-3}$ one has to convert certain selected areas of the substrate into the opposite type of conduction. In order to assure low threshold voltage operation of the n-channel devices, the acceptor concentration N_A of these p-type regions has to be around $9 \times 10^{14} \cdot \mathrm{cm}^{-3}$, corresponding to a specific resistivity of 15 ohm · cm. Some of the pos-

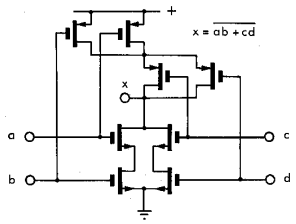

Fig. 1. Complementary MOS transistor AND–NOR gate.

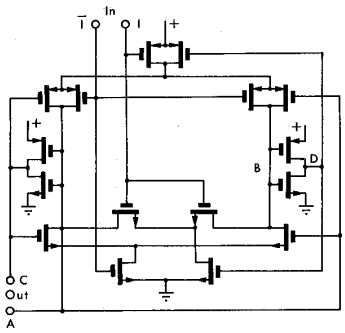

Fig. 2. One-stage binary counter consisting of 8 pairs of complementary MOS transistors.

sible approaches to this problem are:

1) low surface concentration diffusion
2) deep diffusion followed by well-controlled removal of surface layer
3) outdiffusion from buried p-type layer into epitaxially grown n-type layer
4) etching of wells, followed by epitaxial refill-deposition and polishing operation.

We will limit the discussion in this paper to this last technique, since the bulk of our work so far has been concerned with this approach.

From previous work on p-channel devices [5] it is known that starting material of (100) orientation is best in order to obtain low-threshold voltage operation. This is due to the lower positive oxide charge for a (100) surface, compared to that observed for a (111) surface. Lower positive oxide charge results in a n-channel device meeting the important requirement of being in the off-state at zero gate voltage.

The starting material [n-type, 10 ± 1 ohm·cm, (100) orientation] is submitted to the following process steps.

1) Wafers are polished to a thickness of 230 ± 5 μm (alkali containing polishing substances are excluded from all polishing operations).
2) A 1.2 μm oxide is grown on the surface.
3) A first mask is used to form four oxide windows.
4) Using a wet etch (Iodine B), four wells about 30 μm deep are etched into the silicon. This stage of the sequence is schematically illustrated in Fig. 3(a). These deep wells will be used as alignment marks for the masking steps to follow later since the epitaxially refilled wells will no longer be visible after the final polishing operation.
5) The oxide is stripped and a new oxide is grown.
6) A second masking step results in a repetitive pattern of oxide windows. The four etched wells coincide with four windows belonging to this pattern.
7) The oxide windows are now used to etch a repetitive pattern of wells, using a gaseous HCl–H_2 etch in a vertical epitaxial reactor. An etch rate of 3 μm/min is used to etch wells which are 25-μm deep. For this depth, a value of 1.3 was observed for the ratio of lateral attack to perpendicular attack. Fig. 3(b) represents this stage of the sequence.
8) The masking oxide is removed.
9) Epitaxial deposition is performed at 1210°C by the hydrogen reduction of $SiHCl_3$. Diborane gas is used to obtain a p-type film with a resistivity of 15 ± 2 ohm·cm. Fig. 3(c) shows this stage of the sequence.
10) The wafers undergo a second mechanical polishing operation to a level approximately 5 μm below the original surface [as indicated by the dashed line in Fig. 4(a)]. A final HCl etch removing 1 to 2 μm of silicon provides a surface essentially free of polishing surface damage. This final stage of substrate preparation is shown in Fig. 3(d). Due to their greater

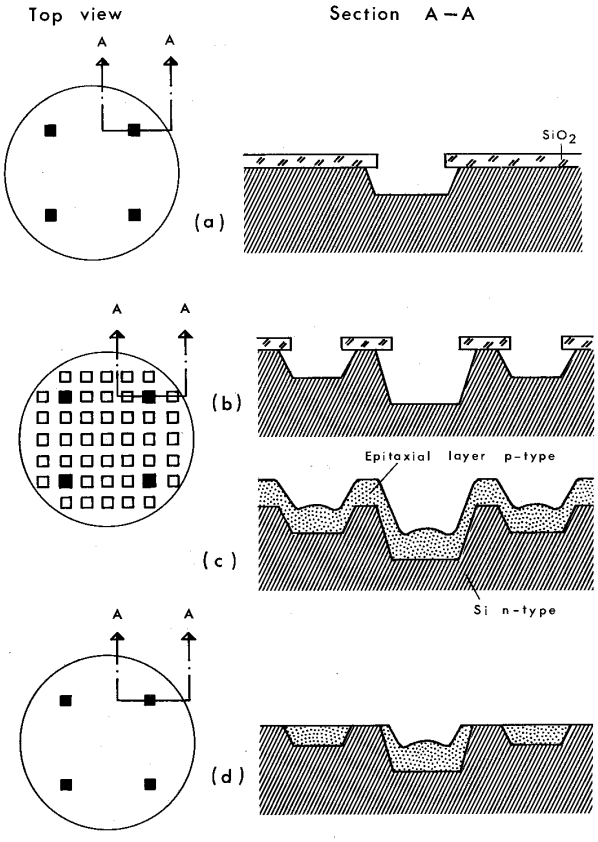

Fig. 3. Schematic drawing indicating the key steps of the substrate preparation sequence.

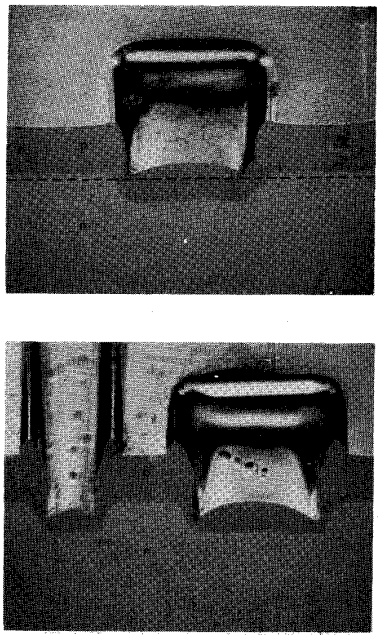

Fig. 4. (a) Cross-sectional view of well after epitaxial deposition of 35-μm-thick p-type layer. Angle lap was at 30°. (b) Faceted structure is due to misalignment within the (100) plane of the mask used to etch the wells.

depth, the four deep wells are still visible. They will serve as alignment marks for the masking steps to follow. The substrate consisting of n-type and p-type regions is now ready for the diffusion and metalization processes to be described in Section II-B.

Before leaving the subject of substrate preparation, a few remarks concerning the etching of the wells and the quality of the epitaxial p-type islands are in order: etch rates lower than about 1 μm/min tend to result in convex-shaped well-bottom surfaces, and replacing the carrier gas hydrogen by helium during the etch phase allows one to use an oxide mask only 0.5 μm thick as compared with the 1.2 μm required in the case of hydrogen.

About 11 500 etch pits/cm^2 have been counted on the starting material after a Sirtl etch. After some 30 μm of silicon had been removed by an HCl–H_2 etch, a Sirtl etch revealed no etch pits over the entire surface of the wafer. The efficacy of the three etches was monitored on (111) surfaces. It is known that it is difficult to reveal dislocations on a (100) surface. It seems therefore very risky to draw any conclusions regarding dislocation densities from the observed etch pit densities. After epitaxial deposition and polishing we find from 10^4 to 10^5 etch pits/cm^2. Their density on the n-type surface is fairly uniform. As far as the p-type islands are concerned, we find that about 80 percent of the etch pits are located within a distance of 20 μm from the edge. The maximum stacking fault density is 10 cm^{-2}.

The room temperature leakage current density of the islands, measured at 1.5 volts was found to vary between 0.5 and 1.5 μA·cm^{-2}. The same order of magnitude values have also been found in the case of a diffused well with an acceptor surface concentration of 10^{15} cm^{-3}.

B. Diffusion and Metalization Processes

A 0.8-μm-thick oxide is used to produce the diffusion windows for the source and drain regions of the p-channel devices. After boron predeposition, the boron glass is removed, followed by drive-in and reoxidation.

A second masking step produces the diffusion windows for the source and drain regions of the n-channel devices. After phosphorous diffusion and subsequent reoxidation, all oxide is removed from the gate areas and the contact windows.

The gate oxide is now grown at 1150°C in a RF-heated double-wall quartz oxidation furnace. The oxidation is done in dry oxygen and its duration is 45 min. It is followed by 30 min of annealing in dry helium, also at 1150°C.

This *in situ* high-temperature annealing step reduces the density of surface states to a level of 1 to 2×10^{10} (eV)$^{-1}$·cm^{-2} [6]. Previous work in our laboratory showed that this clean oxidation-annealing operation resulted in devices showing threshold voltage shifts from 0.01 to 0.04 volts after a positive bias-temperature stress characterized by the following parameters: $T=200$°C, $E_{ox}=1.5\times10^6$ V·cm^{-1}, and $t=24$ h. On devices with their gate oxide grown in a conventional resistance heated furnace equipped with an alumina and a quartz tube, threshold voltage shifts ranging from 0.1 to 0.5 volt have been observed after an identical bias-temperature stress. This range may be appreciably larger, depending on the sodium contamination level of the furnace.

The contact windows are reopened in a fourth masking step.

The evaporation of a Mo-Au sandwich over the entire wafer is done in a conventional vacuum system. 0.25 μm of Mo is evaporated by an electron gun system and 0.4 μm of Au from a resistance heated tungsten boat.

The dependence of the threshold voltages for both p-channel and n-channel devices on the kind of gate metal used is illustrated in Fig. 5. Measured values of threshold voltages at 10 μA drain current on some five hundred transistors differing in their gate width, and in the case of the n-channel device also in substrate resistivity, were normalized according to the gate width and resistivities used in the circuit.[2] The values thus obtained are shown in Fig. 5. It is

[2] Normalization with respect to gate width is straightforward. The substrate resistivity dependent shift for the n-channel device was obtained from measurements of threshold voltages of a large number of devices fabricated on (5±1) ohm·cm and (10±1) ohm·cm substrates, respectively. For (100) substrates, Mo-Au contacts, a gate width of 50 μm, and a channel length of 8 μm, the following ranges of threshold voltages (measured at $I_D=10$ μA) have been obtained: 1.60 to 1.64 volts for 5 ohm·cm and 1.15 to 1.26 volts for 10 ohm·cm. A linear extrapolation of this voltage shift corresponding to a resistivity of 15±2 ohm·cm may result in an error of the same magnitude as the error due to the epitaxial layer resistivity variation (15±2 ohm·cm). Constant electron and hole mobilities, respectively, have been assumed in carrying out this normalization. The justification of this procedure is borne out by the fact that the threshold voltages shown in Fig. 7 fall within the ranges of threshold voltages for the Mo-Au sandwich shown in Fig. 5.

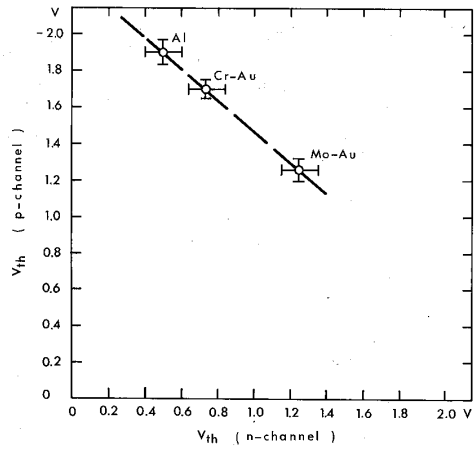

Fig. 5. Dependence of threshold voltages for both p-channel and n-channel devices on the kind of metal used.

not implied that the line connecting the experimental points represents a functional relationship. It merely indicates trends observed consistently.

The Au-Mo-Si (SiO_2)-system satisfies all the essential requirements: acceptable threshold voltages for both p- and n-channel devices, good adherence to SiO_2, and a metallurgically sound bond between gold pads and gold bonding wire. Contact resistance problems occasionally encountered with this system are of no importance at the low current levels used in our case. The metallurgical aspects of the Au-Mo-Si system have been treated in detail by Cunningham [7].

A final masking step defines the interconnection pattern and is followed by metal etching operations.

A 4-hour low-temperature (350°C) annealing process in nitrogen completes the wafer processing sequence. This thermal treatment leads to a reduction of the positive oxide charge by 1 to $2 \times 10^{11} \cdot cm^{-2}$. By alternating simulated[3] molybdenum evaporations from an electron gun operating at 4 kV with 350°C annealing in nitrogen we have been able to show that this positive oxide charge is in fact due to the X-ray exposure during electron gun operation.

This completes the actual wafer processing. Dicing and mounting are conventional.

We have omitted all cleaning operations in the fabrication outline given above. It should be clear, however, that cleanliness in device fabrication has a profound influence on device performance and stability. Our requirements concerning cleanliness are rather extreme, as we do not utilize any passivation process like the deposition of a phosphorous glass onto the gate oxide.

IV. Discussion

Fig. 6 shows a photomicrograph of one binary counter stage. The epitaxially deposited p-type region, a square with 250 μm sidelength, is delineated by the dashed line. Also indicated are two test transistors. Fig. 7 shows the usual square root dependence of the drain current on gate and drain voltage (gate connected with drain) for these transistors. Except for some minor differences concerning the amount of lateral diffusion, the dimensions of both devices are identical and are shown in Fig. 8.

[3] In order to avoid redeposition of molybdenum on the finished wafers, these were protected by mica sheets some 200 Å thick.

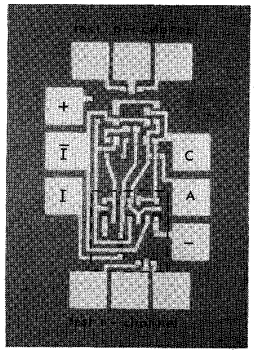

Fig. 6. Photomicrograph of one stage of a binary counter.

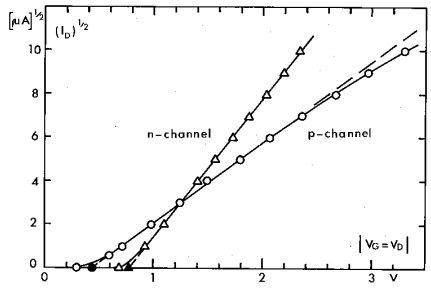

Fig. 7. Square root of drain current as a function of drain and gate voltage (drain and gate are connected, so that $V_G = V_D$).

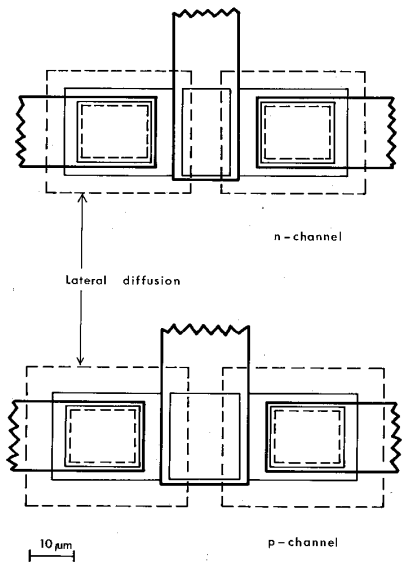

Fig. 8. Top view (to scale) of p-channel and n-channel device used in the circuit.

The dynamic current drain of this circuit is roughly 10 nA/kHz at 1.35 volts supply voltage, corresponding to an equivalent capacity of the order of 7 pF. The observed static consumption of 10 to 30 nA at room temperature is due to leakage currents of the drain diodes, residual off-state channel currents and leakage current of the reverse biased diode formed by the two substrate regions.

Any number of these circuits may be cascaded by connecting the A and C outputs of one stage to the inputs I and $\bar{I}$, respectively, of the following stage. The maximum input frequency of such a chain is of the order of 200 kHz at 1.35 volts supply voltage.

This circuit is not yet optimized and it seems therefore possible to push the upper frequency limit somewhat higher. Parasitic capacities may be further reduced by minimizing the amount of lateral diffusion as well as by reducing capacities associated with the interconnections. An improvement of the transconductance to input capacity ratio may be achieved by reducing the actual channel length of 7 μm to half this value. However, as this type of circuit is especially attractive at low frequencies, it is even more important to reduce the static power consumption by at least one order of magnitude.

Acknowledgment

The authors wish to express their gratitude to Dr. K. Hübner for his valuable suggestions. R. Taubenest and his co-workers were responsible for the difficult task of substrate preparation. It is a pleasure to thank D. Doviane and P. Brander for their expert assistance in fabricating the circuits.

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Summer course on Switched Capacitor Circuits, June 9-12, 1981
ESAT, Katholieke Universiteit Leuven, Heverlee, Belgium

MICROWATT SWITCHED CAPACITOR CIRCUIT DESIGN

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A la mémoire de mon ami Jean Fellrath

1. INTRODUCTION

Energy must be saved in battery-operated instruments. This is mandatory in electronic watches where the average power available is only a few microwatts. Micropower operation is required or desirable in various other portable instruments such as paging receivers, hearing aids, implanted biomedical devices, and devices for environment and security control [1].

Switched capacitor circuits have not yet been effectively used in watch circuits, but they start appearing in DC handling circuitry (controlled voltage generation, battery voltage checking). Furthermore, SC filters are considered for word recognition systems to be incorporated in watches.

Micropower filters are required to enhance pulses delivered by the heart in pacemakers and will be needed in future portable devices to process analog signal delivered by sensors. A dynamic range of 60 to 80 dB is acceptable in such applications, but the current drain must be kept below 1 to 10 µA with a single supply voltage V_{cc} lower than 3 V.

CMOS is ideally suited for micropower, and Si-gate has some advantages over Al-gate, mainly because of its self-alignment properties.

Analog subcircuits, including SC circuits, must be compatible with standard technologies that are optimized for digital applications.

After a brief review of the behaviour of MOS devices at very low current, this paper will discuss the CMOS implementation of the three basic components of SC circuits (switches, matched capacitors, amplifiers) in the context of low power and low voltage. Some emphasis will be put on the realization of amplifiers and on the trade off between low power, settling time and noise considerations. Large parts of this discussion are derived from reference [2].

United States Patent

[11] **3,619,646**

[72] Inventor **Eric Andre Vittoz**
Hauterive, Switzerland

[21] Appl. No. **875,680**
[22] Filed **Nov. 12, 1969**
[45] Patented **Nov. 9, 1971**
[73] Assignee **Centre Electronique Horloger SA**
Neuchatel, Switzerland
[32] Priority **Nov. 11, 1968**
[33] **Switzerland**
[31] **16,822/68**

[54] FREQUENCY DIVIDER CIRCUIT

8 Claims, 9 Drawing Figs.

[52] **U.S. Cl.** **307/225,** 307/205, 307/303
[51] **Int. Cl.** **H03k 21/00**
[50] **Field of Search** 307/220, 205, 225, 251, 279, 303, 304, 246; 328/39; 340/173

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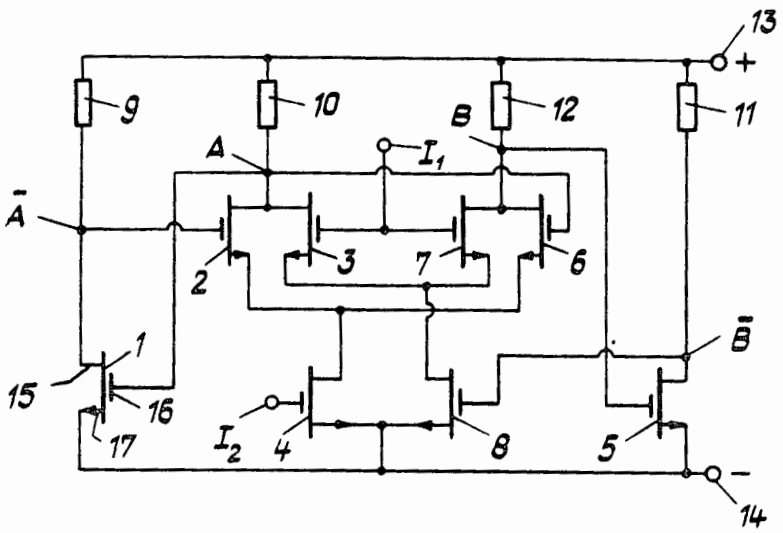
Primary Examiner—Stanley T. Krawczewicz
Attorney—Stevens, Davis, Miller & Mosher

ABSTRACT: A frequency divider circuit including at least one logical structure complying with the Boole Relations:

$A=\overline{BI_1+AI_2}$ and $B=\overline{BI_1+AI_2}$

in which I_1 and I_2 are two complementary input quantities and A and B two output quantities.

The logical structure comprises three pairs of field effect transistors, such as MOS-transistors having isolated gates. A cascade of binary frequency divider circuits can be made as an integrated circuit.



FREQUENCY DIVIDER CIRCUIT

BACKGROUND OF THE INVENTION

Frequency division is generally obtained by multivibrators which, in order to function correctly, must be fed with input pulses offering certain qualifications, as for example a maximum growth time. From that fact, the operation of these circuits depends on the behavior of these input signals.

Efforts have been made to remedy this disadvantage by using, in the frequency divider circuit, logical circuits. These circuits are, however, complex.

OBJECT OF THE INVENTION

It is an object of this invention to simplify the known frequency divider circuits, and to provide such circuits which are reliable and can easily be made in the form of integrated circuits presenting a cascade of binary frequency divider circuits.

DEFINITION OF THE INVENTION

According to the present invention, a frequency divider circuit comprises at least one logical structure complying with the Boole relations:

$A=\overline{\overline{B}\,I_1+\overline{A}\,I_2}$ and $B=\overline{\overline{B}\,I_1+\overline{A}\,I_2}$

in which I_1 and I_2 are two complementary input quantities and A and B two output quantities.

Said logical structure comprises three pairs of field-effect transistors, each of them having a source, a drain and a gate, two outputs connected each to the drains of the two transistors of a first, respectively of a second pair, the sources of one transistor of the first and one transistor of the second pair being connected to the drain of a transistor of the third pair and the sources of the two other transistors of this first and second pair being connected to the drain of the other transistor of the third pair, or the four sources of the transistors of the two first pairs being connected together to the two drains of the transistors of the third pair, the two sources of the transistors of the third pair being connected together to one of the terminals of a tension source.

DESCRIPTION OF PREFERRED EMBODIMENTS

In the annexed drawing, the mathematical basis of the circuit and some preferred embodiments are shown.

FIGS. 1 to 4 are diagrams explaining the mathematical basis on which the circuit is built.

FIG. 5 shows an embodiment having MOST (i.e., a field-effect transistor having an isolated gate, also called IGFET) of the same type only.

FIG. 6 shows a variant of the embodiment according to FIG. 5.

FIG. 7 shows a variant of the embodiment according to FIG. 6 which is derived from this latter by replacing load resistors by MOST.

FIG. 8 shows an embodiment with complementary MOST and two logical circuits.

A structure complying with the system of logical equations:

$A=\overline{\overline{B}\,I_1\overline{A}\,I_2}$

$B=\overline{\overline{B}\,I_1\overline{A}\,I_2}$

permits to divide by two the frequency of the input signals I_1 and I_2.

Assuming that $I_2=\overline{I}_1$, we obtain the transition diagram of FIG. 1.

The arrows indicate the various implications. One can verify that the quantities implicating a given transition do not change their state during this transition.

The variation frequency of each of the quantities A and B is half of I_1 and I_2, as is shown more clearly on FIG. 2.

In reality, the showing of FIG. 1 is incomplete, because one has to take into account the transition times of I_1 and I_2, so short can they be. As I_1 and I_2 are practically obtained by inversion of one another, it can be seen that the transitions of one of these two quantities are slightly delayed compared to those of the other. By assuming that I_2 is obtained by the inversion of I_1, we obtain the transition diagram of FIG. 3.

The transition surrounded by a dotted line is forbidden, because it occurs on a quantity implicating the following state; therefore, it must not arise before I_2 has taken the value 1, by introducing a delay element. The transient states are represented on FIG. 3 by ET.

FIG. 4, which corresponds to FIG. 2, shows the logical values taken by the various signals, in course of time. R represents the delay, TI the forbidden transition.

In the case where I_1 is delayed compared to I_2, it can be seen that two transitions are forbidden, one from A, the other from B.

FIG. 5 shows a first embodiment of a circuit with eight N-type MOST 1 to 8 working in enrichment mode, and four load resistors 9–12. Each MOST includes, as indicated for MOST 1 only, a drain 15, a gate 16 and a source 17. The drains of MOST 1 and 5 respectively are connected to load resistors 9 and 11 respectively, and to the gates of MOST 2 and 8 respectively. The drains of MOST 2 and 3, and 6 and 7 respectively are connected together to load resistors 10 and 12 respectively, and to the gates of MOST 1 and 5 respectively. The drains of MOST 4 and 8 are connected to the sources of MOST 2 and 6; and 3 and 7 respectively. Sources of MOST 1, 4, 5 and 8 are connected to the negative terminal of a voltage source (not shown), those of MOST 2 and 6 to the drain of MOST 4, and those of MOST 3 and 7 to the drain of MOST 8. The control signals I_1 and I_2 respectively are fed to the gates of MOST 3 and 7, and MOST 4 respectively. The signals A, B, $\overline{A}$, $\overline{B}$ appear at the terminals of the load resistors 10, 12, 9 and 11 respectively, opposite to those connected to the positive terminal 13 of the voltage source.

The circuit of FIG. 6 comprises the same elements as that of FIG. 5, but the sources of MOST 2, 3, 6 and 7 are all connected to the drains of MOST 4 and 8, themselves connected together, instead of the sources of MOST 2 and 6 being connected to the drain of MOST 4 and the sources of MOST 3 and 7 to the drain of MOST 8. As a result, the circuit of FIG. 6 is the duality of the one of FIG. 5, the states O and I, as well as the operations AND and OR being permutated.

It complies to the same equations as the circuit of FIG. 5.

Indeed, we have.

$$\overline{A}=\overline{(A+\overline{I}_2)(B+\overline{I}_1)}=\overline{(A+\overline{I}_2)}+\overline{(B+\overline{I}_1)}=\overline{A}I_2+\overline{B}I_1$$

$$\overline{B}=\overline{(A+\overline{I}_2)(B+\overline{I}_1)}=\overline{(A+\overline{I}_2)}+\overline{(B+\overline{I}_1)}=AI_2+BI_1$$

The circuits of FIGS. 5 and 6 comprise fewer elements than the classical logical division circuits. They are not critical: it is sufficient that the delay necessary for good operation exceeds a certain value.

In the two previous circuits, load resistors 9 to 12.

In the two previous circuits, load resistors 9 to 12 can be replaced by MOST. The circuit on FIG. 6 is transformed, for example into that of FIG. 7. The four resistors 9 to 12 are replaced by four MOST 18 to 21, of which all the drains are connected to the positive terminal 13 of the voltage source, and of which all the gates are connected to a control terminal 22. By connecting terminal 22 to a source with short positive impulsions, the circuit works in "pulsed power" permitting considerable reduction in the average current consumed. MOST 18 to 21 conduct in fact only during the short impulsions; they are blocked during the intervals between the impulsions, the state of the circuit being then conserved by the "parasitical" capacitances.

As to its manufacture, this circuit has the advantage of comprising MOST only, which facilitates its realization as an integrated circuit.

The circuit of FIG. 8 is realized with complementary MOST. It permits reduction in current to that necessary for loading the parasitical capacitances during the transitions. The consumption is then proportional to the working frequency. The circuit complies with the same equations as the above-mentioned ones.

United States Patent [19]

Hammer et al.

[11] **3,895,486**

[45] **July 22, 1975**

[54] **TIMEKEEPER**

[75] Inventors: **Walter Hammer,** Boudry, NE; **Eric Andre Vittoz,** Cernier, NE; **Jean Hermann,** Neuchatel, NE; **Hubert Choffat,** Saint-Blaise, NE, all of Switzerland

[73] Assignee: **Centre Electronique Horloger S.A.,** Neuchatel, Switzerland

[22] Filed: **Mar. 21, 1972**

[21] Appl. No.: **236,774**

[30] **Foreign Application Priority Data**

Oct. 15, 1971 Switzerland 15117/71

[52] **U.S. Cl.** ..... **58/23 R;** 58/85.5

[51] **Int. Cl.** **G04b 27/00**

[58] **Field of Search** ..... 307/225; 328/48, 120; 58/23 R, 23 A, 23 AC, 24, 39.5, 33, 85.5, 26, 23 BA, 50 R, 152 H, 153, 57; 310/8.1

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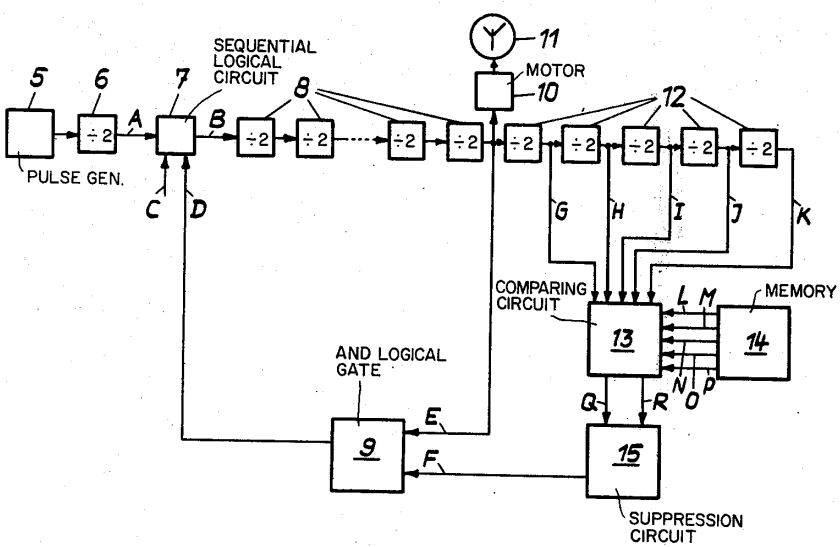
Primary Examiner—Stephen J. Tomsky
Assistant Examiner—U. Weldon
Attorney, Agent, or Firm—Stevens, Davis, Miller & Mosher

[57] **ABSTRACT**

A timekeeper comprises a quartz crystal resonator having a stable frequency but with a relatively large tolerance, and a frequency divider with an adjustable divison ratio. Said divider has auxiliary electrical inputs the logical state of which determines the division ratio, and a memory, for example an electrically alterable electronic memory, supplies stored data to determine the logical state of the auxiliary inputs and hence the division ratio. The memory may comprise volatile and permanent parts, the permanent part intermittently regenerating data stored in the volatile part.

21 Claims, 28 Drawing Figures



TIMEKEEPER

The invention relates to timekeepers of the type comprising a resonator and a frequency divider with an adjustable division ratio.

In timekeepers comprising a time base and a frequency divider, the required output frequency of pulses from the frequency divider is generally obtained by providing both that the time base, usually formed by a quartz-crystal-controlled pulse generator or a diapason (tuning fork), has an exactly determined frequency, and that the frequency divider has an exactly determined division ratio.

This necessitates a careful adjustment of the time base which, for example in the case of a quartz crystal resonator, is carried out with the following steps:

1. Rough adjustment, in which the relative divergence $\Delta f/f$ between the natural frequency of the quartz resonator and its nominal value passes from about 10^{-2} to 10^{-4};

2. Fine adjustment, in which $\Delta f/f$ passes from 10^{-4} to several units $\times 10^{-5}$; and

3. Final adjustment and compensation for ageing, in which $\Delta f/f$ passes from several units $\times 10^{-5}$ to less than 10^{-6}.

These steps each require delicate and costly operations, especially difficult to carry out for miniature quartz crystals intended for portable timekeepers such as those for wrist watches. In effect, for energy consumption reasons, miniature quartz crystals must oscillate at low frequencies, typically comprised between 8 and 64 KHz. Such resonators are formed by bars oscillating in flexion and their small dimensions, in particular the reduced thickness, require an extremely great precision in cutting the crystal. The rough adjustment takes place by filling the ends of the bars, in very difficult working conditions. The required frequency precision of 10^{-5} for encapsulated quartz resonators is particularly difficult to achieve, since for wrist watches the resonators must have a shock-resistant suspension, the rigidity tolerances of which have an appreciable influence on the frequency, and a small casing. Both the suspension and the casing may, during the final stages of manufacture, modify the frequency of the quartz resonator by several units $\times 10^{-5}$. This frequency difference can be partly compensated for by providing an adjustment after closing the casing, and by arranging two windows through which a metallic layer can be deposited on the ends of the quartz crystal bar before closing the windows and evacuating the casing; however, this is a complex and costly operation. Lastly, the final adjustment is usually carried out by means of an adjusting capacitor in series with the quartz crystal in the resonator circuit.

This procedure has numerous drawbacks which adversely effect both the precision and the cost of the finished product, for example a wrist watch. The rougn and fine adjustments are detrimental to the frequency stability of the quartz resonator and increase ageing effects. The final adjustment requires use of an adjustable element (capacitor) the stability of which also effects the frequency stability of the resonator, which therefore becomes sensitive to exterior influences such as the temperature, humidity, dust, and so on.

Moreover, the rough and fine adjustment operations being delicate, they must be carried out using complex equipment and taking special precautions, which considerably adds to the cost price of the resonator. The adjusting capacitor is also a fairly expensive component and takes up valuable space.

It has been proposed (W. German published patent application DAS 1, 946, 166, Timex corresponding to U.S. Pat. No. 3,540,207 to Rieler) to do away with the adjusting capacitor by employing a frequency divider whose division ratio is adjustable by means of an inhibition member. One of the described embodiments provides a potentiometer for adjusting the duration of this inhibition, which amounts to replacing one precisely adjustable element by another component subject to the same requirements of maintaining a stable value. Another of the described embodiments provides switches (commutators) which enable modification of the division ratio by inhibition of a number of pulses equal to 2 to the power of any whole positive number (including zero), i.e. 1, 2, 4, 8 . . . pulses. These embodiments thus also replace one delicate electromechanical component by another one subject to the same problems of stability, bulk and cost. Pulses from an integrated circuit, to which the switch is exterior, pass through the switch, which can involve dangers such as errors in operation, excessive consumption, and overloading of the circuit, especially in a humid, corrosive or dusty atmosphere. Moreover, it can easily be shown that this arrangement enables neither a very large correction of the division ratio, nor a fine adjustment of this ratio.

Dividers with adjustable division ratios operating according to other principles are also known and used, in particular in frequency synthetisers. However, most types have characteristics which render them inapplicable to use in wrist watches, either because of difficulties that would be involved in providing them in integrated form, or for diverse other reasons. For example, a known adjustable frequency divider operating by inhibition (W. German Patent Publication No. 1, 299, 023, Lorenz) requires, in addition to a principal frequency divider, an auxiliary counter operating at the same frequency as the principal divider, which doubles the power consumption and requires switches (commutators) which can be arranged in combinations to determine the desired division ratios. The inclusion of such switches would involve problems of availability of space, cost and, especially, would make adjustment of running of a timekeeper rather difficulty, especially for the user or an after-sales service.

The general aim of the invention is to eliminate these drawbacks and to enable the introduction of new possibilities of adjustment of a timekeeper which could not be carried out by the previously known means. A specific aim is to propose a satisfactory solution to the problem of obtaining a precisely adjustable timekeeper comprising a quartz resonator whose frequency is stable but may be comprised within relatively large tolerances.

According to the invention, a timekeeper comprises a resonator, a frequency divider with an adjustable division ratio, said divider having auxiliary electrical inputs the logical state of which determines the division ratio, and a memory connected to said auxiliary inputs, said memory storing coded data which determine the logical state of said auxiliary inputs and therefore the division ratio of the divider.

Several important advantages stem from the arrangement according to the invention.

Clark Nguyen Presents DL Talk on RF-MEMS in Japan

SSCS Distinguished Lecturer Clark T.-C. Nguyen presented a talk entitled "Integrated Micromechanical Circuits for RF Front-Ends" to a crowd of 150 at Nihon Dempa Kogyo (NDK) in Sayama-city, Saitama, Japan on 24 April, 2008.

The one and one-half hour lecture and discussion at the company was part of NDK's annual engineer educational program, said NDK Fellow Takeo Oita, the organizer of this year's Spring 2008 Special Session. "We at NDK have always endeavored to keep up with new technologies, not only quartz crystal but also other materials and technologies representing Si-MEMS," he said. "Since Clark and I have had many discussions about the above areas for many years, I decided to arrange this talk to acquaint our engineers with the latest RF-MEMS technology in the world. I am sure his remarks helped our engineers broaden their horizons."

Abstract:
Recent advances in vibrating RF MEMS technology that yield on-chip resonators with Q's over 10,000 at GHz frequencies and excellent thermal and aging stability have now positioned vibrating micromechanical devices as strong candidates for inclusion into a number of future wireless communication sub-systems, from cellular handsets, to PDA's, to low-power networked sensors, to ultra-sensitive radar and jam-resistant communicators designed for hostile environments. Indeed, early start-ups have already sprouted to take advantage of this technology for timekeeper applications, and the timing of this technology seems well placed for wireless markets, whose requirement for multi-mode reconfigurability fuels a need for on-chip high-Q resonators to prevent the cost of the front-end passives in a typical handset from obviating that of the IC's. But the benefits of vibrating RF MEMS technology go far beyond mere component replacement. In fact, the extent of the performance and economic benefits afforded by vibrating RF MEMS devices grows exponentially as researchers begin to perceive them more as building blocks than as stand-alone devices. In particular, when integrated into micromechanical circuits, in which vibrating mechanical links are connected into larger, more general networks, previously unachievable signal processing functions become possible, such as reconfigurable F channel-selecting filter banks, ultra-stable reconfigurable oscillators, frequency domain computers, and frequency translators. When further integrated together with other micro-scale devices (e.g., transistors, micro-ovens, micro-coolers, atomic cells), system level benefits for portable applications abound, particularly those for which architectural changes allow a designer to trade high Q for lower power consumption and greater robustness, with potentially revolutionary impact. This presentation describes the MEMS technologies and attributes most suitable to enabling such an integrated micromechanical circuit technology.

Prof. Clark T.-C. Nguyen of UC Berkeley spoke on RF-MEMS technology at Nihon Dempa Kogyo (NDK) in Sayama-city, Japan on 24 April, 2008.

Dr. Nguyen, who is a professor at UC Berkeley, gave a shorter version of this talk at the 2008 IEEE VLSI-TSA plenary session in Taiwan at the invitation of VLSI-TSA conference chair, Dr. Clement Wann. Dr. Nguyen presented another DL talk at National Semiconductor in Santa Clara, CA on 8 May.

Further information about NDK may be found at www.ndk.com /en/index.html. More information about the SSCS Distinguished Lecturer Program may be found at //sscs.org/Chapters/dl.htm.

About Clark Nguyen

Prof. Clark T.-C. Nguyen received the B. S., M. S., and Ph.D. degrees from the University of California at Berkeley in 1989, 1991, and 1994, respectively, all in Electrical Engineering and Computer Sciences. In 1995, he joined the faculty of the University of Michigan, Ann Arbor, where he was a Professor in the Department of Electrical Engineering and Computer Science until mid-2006. In 2006, he joined the Department of Electrical Engineering and Computer Sciences at UC Berkeley,

where he is presently a Professor and a Co-Director of the Berkeley Sensor & Actuator Center. His research interests focus upon micro electromechanical systems (MEMS) and include integrated micromechanical signal processors and sensors, merged circuit/micromechanical technologies, RF communication architectures, and integrated circuit design and technology. In 2001, Prof. Nguyen founded Discera, Inc., the first company aimed at commercializing communication products based upon MEMS technology, with an initial focus on the very vibrating micromechanical resonators pioneered by his research in past years. He served as Vice President and Chief Technology Officer (CTO) of Discera until mid-2002, at which point he joined the Defense Advanced Research Projects Agency (DARPA) on an IPA, where he served for three-and-a-half years as the Program Manager for 10 different MEMS-centric programs in the Microsystems Technology Office of DARPA.

Katherine Olstein,
SSCS Administrator,
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Part 2: Narrow Your Questions, Shape Your Answers

Peter and Cheryl Reimold, www.allaboutcommunication.com

In the last column we proposed a quick and easy way to approach a short piece of writing ("The Five-Minute Miracle," January/February 2003 Newsletter). Briefly, you set up a conversation with your reader in which you begin with your main message and then answer your reader's probable questions about that message. Your main message will require only the opening sentence or paragraph (from one to three sentences in all). The bulk of your writing will consist of your answers to the questions you think your readers would have. Now we must see how to make those answers easy to write and useful to read.

Narrow Your Reader's Questions

The first step to easy answers is finding the right questions. The right questions are the ones that tell the readers what they most want and need to know. It is worth spending some time considering what questions are most important, so as not to waste more time answering others that lead you away from the main reasons for your report. For example, suppose you are writing a progress report with the following main message:

Although phase one of the project

was completed two months behind schedule, we now have the data needed to begin phase two.

What do you think your reader's first question would be? The question that immediately pops to mind might be, "Why were you so late finishing phase one?"

That could be a large and difficult question to answer. It could lead you into a litany of explanations, accusations, justifications, apologies, and excuses for the delay that quickly fills up a full page. Is it really the most valuable question? After all, neither you nor your reader will benefit from an annotated list of all the obstacles that came between you and the completion of phase one. If you start with that, you will irritate the reader with all your self-justifying details while giving your report a negative cast by drawing attention to all the things that went wrong before.

Instead of going with the first question that occurs to you, stop to ask yourself what your reader most wants to know. In this case it might be, "When do you expect to complete the project (or, at least, phase two)?" Answering that question first will tell the reader what he or she wants to know right up front. It will give your report a positive, forward-looking approach. Finally, it will leave room for you to explain the reasons for the phase one delay further on, in one or two sentences. Once you have shown that you are on a planned, positive course, the reader will be more accepting of the previous problems that now appear as history.

Structure Your Answers

The best structure for answering your reader's probable questions is this:

Key Point + Backup

It gives the reader the answer immediately and then makes that answer credible by bolstering it with an example, an illustration, or an explanation.

This approach does not come naturally. Our tendency seems to be the reverse: Build up evidence and then present the conclusion. Although this progression makes sense in science and logic, it doesn't work well for business writing. Why not? Well, think of your own expectations as a reader: Do you want to know the answer to your question at the beginning or the end of the section?

To write effectively in business, we must remember to tell the reader the answer first and then explain the reasoning behind it.

In the example, you would begin your answer with a clear statement of when and how you hope to complete the project or its second phase. One or at most two sentences should suffice. Then you would follow with your reasons for this assertion.

Yes, in one sense this method is harder, because it forces you to make clear, committed statements. That's what you look for in the writing you receive, isn't it?

Try it, and, as always, please let us know how it works for you: perccom@aol.com.

Cheryl and Peter Reimold have been teaching communication skills to engineers, scientists, and business people for 20 years. Their firm, PERC Communications (+1 914 725 1024, perccom@aol.com), offers businesses consulting and writing services, as well as customized inhouse courses on writing, presentation skills, and on-the-job communication skills. Visit their Web site at http://www.allaboutcommunication.com.

The article is gratefully reprinted with permission from the authors and the IEEE Professional Communication Society from the May/June 2003 issue, Volume 47, Number 3, pages 10 & 14 of the IEEE PCS Newsletter.

Corrections

Dear Prof. Kernighan,

I enjoyed reading your piece in the IEEE Solid-State Circuits Society News. It is a nice mix of ideas about the technology and the people. It is way too rare for the people to be mentioned, let alone featured as you did.

A minor detail is that the author's name in your last reference should be "Swade" not "Swore."**

Regards, Earl Swartzlander
Professor of Electrical and Computer Engineering
University of Texas at Austin

**Editor's Note: *"Doran Swade is the author of "Charles Babbage and the Quest to Build the First Computer," referenced on page 5 of the SSCS News Vol. 13, No.2.*

ISSCC Student Forum

Both Masters and Ph.D. graduate students network at a special Forum, Saturday evening before ISSCC begins. Tinoosh Mohsenin, a graduate student participant in the 2008 Forum from UC Davis thought, "The ISSCC Student Forum was a great opportunity to present my research and interact with other students and faculty involved in chip design. I had the chance to see early-stage research results, that in many cases were not yet published, by students from universities around the world."

The Forum consists of a succession of 5-minute presentations from graduate students, who have been selected on the basis of a short submission concerning their ongoing research. Selection is based on the potential novelty and coherence of their proposed presentation. The work described is not intended to be complete or final. In February 2008 there were 30 presentations from all regions. This inaugural event attracted more than 100 attendees, primarily graduate students and professors.

Patrick Mercier, a graduate student from MIT felt "the short five minute presentations encouraged students to succinctly present only their key ideas and contributions - a skill that is becoming increasingly important in today's busy world." It provided "an avenue for students to obtain valuable presentation experience and technical feedback." Tomokazu Ishihara of Kobe University agreed: "The concise explanation of research results and the technical feedback made our studies more polished." "I was really motivated and encouraged by the whole experience in the Forum. It was very exciting time for me," he said.

The Chair of the ISSCC 2007 Student Forum, Prof. Anantha Chandrakasan of MIT noted, "ISSCC is driving towards active participation at ISSCC. The student forum provides an excellent opportunity for students to network, get early feedback on their research, and explore collaboration opportunities. "

During breaks and an evening meal, there are a few minutes to approach others one-to-one. Ishihara appreciated the insight and "knowledge gained from aspects of research that the students from foreign countries helped me discover." Mohsenin had the "fortunate benefit of meeting a student researcher that I had previously not known, who is working in a closely-related area."

The ISSCC Student Forum has been organized as short presentations of work-in-progress, and will not be considered as pre-publication for future ISSCC regular-paper submissions or other SSCS Conferences (assuming other conference specific pre-publication rules are followed). "We expect many of the projects presented with early prototype chips to translate to regular paper submissions in future years" commented Chandrakasan.

Participants include the author of the best (local/regional) conference paper from an emerging country. In the Student Forum of ISSCC2008, the author of the best paper from VLSI Design in India was invited. This cooperation with VLSI Design "helps promote ISSCC in terms of awareness, and future paper submission and conference attendance in India," commented Professor C.K. Wang of National Taiwan University.

This Forum is a very useful way to start your week participating at ISSCC and to start your research career. ISSCC 2009 will be February 8 to 12 in San Francisco, the Forum on February 7. Look for the Call for Participation on line later this fall www.isscc.org/ The submission deadline is in early November, about two months after the deadline for submission of conference manuscripts. The Forum "allows students a chance expose themselves and learn about the ISSCC at early stage," C.K. Wang recommended. Students are advised to discuss participation in the Forum with their faculty advisors. Faculty advisors are of course welcome to attend.

In 2009 for the first time, industry representatives will also have an opportunity to observe Forum presentations. In the past, the Forum focused exclusively on student exchange. But the advantages to students of getting feedback from industry are important.

"Overall, I greatly enjoyed my experience at the forum and would highly encourage other students interested in sharing their work at ISSCC to participate," recommends Mercier. Kenneth C. Smith, Professor Emeritus, University of Toronto points out that "idea was for ISSCC to provide a mechanism for the interaction of graduate students from across the globe. We look forward to evidence of its effectiveness at future ISSCC's."

Anne O'Neill
Executive Director, SSCS

Thirty graduate students from around the world met before the ISSCC in February 2008 to exchange brief presentations about their work in progress. Call for Participation in the 2009 Student Forum will be available on www.isscc.org in November.

2007 VLSI-TSA/DAT Best Paper Awards Presented in Hsinchu, April, 2008

Clara Wu and Elodie Ho, VLSI-TSA and VLSI-DAT Symposia Secretariat, vlsitsa@itri.org.tw, vlsidat@itri.org.tw

In opening ceremonies on 21 and 23 April, 2008, the 2008 International Symposia on VLSI Technology, Systems and Applications (VLSI-TSA) and VLSI Design, Automation and Test (VLSI-DAT) presented a Best Student Paper Award for 2007 to Donovan Lee, a graduate student at UC Berkeley, and a Best Presentation Award for 2007 to Prof. Tsung-Hsien Lin of National Taiwan University. SSCS is a cosponsor of both meetings.

Fluid-Gate MOSFET Advances "Lab on Chip" Concepts

"*WetFET – A Novel Fluidic Gate-Dielectric Transistor for Sensor Application*," Donovan Lee, Xin Sun, Emmanuel Quevy, Roger T. Howe, and Tsu-Jae King Liu, Electrical Engineering and Computer Sciences Department, UC Berkeley

Abstract:
The sensitivity of a MOSFET's performance to variations in gate dielectric properties is well known. This sensitivity lends itself perfectly to the MOSFET's utilization as a sensor. Modern biosensors employ gaps with dimensions on the nanometer scale, with their sidewalls functionalized to bind to particular target molecules (such as DNA). Changes in the electrical properties of a nanogap can be detected via resistance or capacitance measurement. Since a modern MOSFET has gate dielectric thickness in nanometer range, it is ideal for adaptation as a nanogap sensor. Furthermore, the use of a MOSFET to sense changes within a nanogap that constitutes a portion of the gate dielectric offers the advantage of signal amplification – a feature unique to transductive sensors (not found in 2-terminal sensors). In this work, we investigate the characteristics of a MOSFET with a hybrid solid/liquid gate-dielectric structure, which can be used for fluidic sensor applications. This "WetFET" device is made using a standard MOSFET fabrication process with additional steps to selectively remove portions of the gate dielectric and to subsequently refill the resultant gaps with liquid. Characteristics of the first prototype WetFET device are presented and analyzed with the aid of device simulations.

In an interview, Mr. Lee said this ground-breaking work "takes advantage of the inherent sensitivity of the standard FET to create a chemical sensor. Since so many chemical and biological systems of interest are dissolved aqueous solutions, the fluidic-gate MOSFET is a very important step toward "lab on a chip" concepts. The device, which is easy to fabricate using CMOS-compatible techniques, is a viable candidate for future system integration," he said.

Mr. Donovan Lee (at left) received the VLSI-TSA Best Student Paper Award for 2007 from Dr. Clement H. Wann, the general chair of 2008 VLSI-TSA.

Mr. Lee, whose childhood goal was to become an inventor, credited mentors in an internship with the US Navy for spurring his interest in engineering. "They taught me that real engineers should be able to fix any problem by asking the right questions," he said. "Electrical engineering and device physics interested me the most because they focus on practical applications of magical phenomena. I found that in EE it was hardest to ask the right questions, and I enjoy the challenge." Mr. Lee plans to become a professor after earning his degree.

The VLSI-TSA Symposium gave its first Best Student Paper Award in 2005 to the paper that was best-written and best-presented by a full time student. Thereafter, the conference committee has presented the Award annually. Winners for 2005 and 2006 were:

2005: Chung-Hsun Lin, Department of EECS, UC Berkeley, for "Compact Modeling of FinFETs Featuring Independent-Gate Operation Mode";

2006: Chia-Pin Lin, Dept. of Electronics Engineering & Inst.of Electronics, National Chiao Tung University, "Impact of Back Gate Bias on Hot-Carrier Effects of n-channel Tri-Gate FinFETs (TGFET)"

2.4-GHz Two-Point Delta-Sigma Modulation Transmitter to Reduce Chip Area & Power Consumption Wins VLSI-DAT Award

The VLSI-DAT Symposium established its Best Presentation Award in 2006 to recognize the best-organized and best-presented conference paper each year by a student or IC professional, based on audience surveys during each session covering technical content, slide quality, presentation and Q&A handling. This year's winner was Prof. Tsung-Hsien Lin of National Taiwan University.

"A 2.4-GHz 18-mW Two-Point Delta-Sigma Modulation Transmitter for IEEE 802.15.4," Prof. Tsung-Hsien Lin, National Taiwan University, Taiwan

Abstract:
The 2.4-GHz two-point modulation transmitter (TX), designed for IEEE 802.15.4 (ZigBee) applications, is based on a delta-sigma fractional-N PLL to reduce chip area and power consumption. In addition, the chosen architecture prevents the transmission data rate from being limited by the PLL bandwidth. To alleviate the non-linearity problems of a conventional fractional-N PLL, linearization techniques are adopted. The TX is designed to operate in the 2.4-GHz ISM band, and is capable of delivering a date rate more than 2 Mbps. Implemented in the TSMC 0.18-µm CMOS process, the TX consumes 18 mW under a 1.4-V supply voltage.

Prof. Tsung-Hsuen Lin (at left) received the VLSI-DAT Best Presentation Award for 2007 from Dr. Jing-Yang Jou, the general chair of 2008 VLSI-DAT.

New 2008 VLSI-DAT Best Student Paper Award

The 2008 VLSI-DAT Technical Program Committee will grant the first-ever Best Student Paper Award in 2009 to the paper that is best-written and presented by a full-time student at this year's meeting. The evaluation will be conducted during the conference. The Best Presentation Award and Best Student Paper Award will both be granted in 2009 at VLSI-DAT.

Now It's Japan's Turn to Host

4th Asian Solid-State Circuits Conference, November 3-5, 2008, Fukuoka, Japan

Koji Kito, A-SSCC 2008 Organizing Committee Chair, Semiconductor Technology Academic Research Center (STARC), kito.koji@starc.or.jp

The fourth Asian Solid-State Circuits Conference will be held on 3 - 5 November in Fukuoka, Japan, at the JAL Resort Sea Hawk Hotel located on the scenic waterfront of downtown Fukuoka. The conference is fully sponsored by the IEEE Solid-State Circuits Society.

Traveling around Asian countries to a different locale each year, A-SSCC provides unique opportunities for semiconductor design experts and technology/business leaders to get together in Asia and to exchange ideas and information.

Between 1997 and 2007, the semiconductor market in Asia grew from US $62 billion to US $173 billion, with a compound annual growth rate (CAGR) of 10.8%. In 2007, approximately 65% of semiconductor products were sold in Asia, and approximately 40% of semiconductor products were sold by companies headquartered in Asia. In 2008, a similar pattern of

growth is expected to continue, supported by the high level of regional research and development activities that is evidenced by the large number of papers submitted from Asia to the A-SSCC:

Year	2005	2006	2007	2008
Country	Taiwan	China	Korea	Japan
Papers submitted	362	332	347	TBA
Papers accepted	136	107	113	TBA
Acceptance Rate	38%	32%	33%	TBA

A comparable number of paper submissions and acceptance rate are expected for 2008. Therefore, the paper quality will be exceptional and the presentations will be very stimulating.

Regular Sessions

Since the TPC consists of a balanced mix of experts from both industry and academia, regular sessions will cover the interests of attendees from various semiconductor product segments, especially in the following eight categories:

- Analog Circuits & Systems
- Data Converters
- Digital Circuits & Systems
- SoC & Signal Processing Systems
- RF
- Wireline & Mixed-Signal Circuits
- Emerging Technologies and Applications
- Memory

Student Design Contest

A student design contest will include accepted papers with system prototypes or measurement results of which operations can be demonstrated on-site. Some of the technical papers selected from the A-SSCC will be printed in a special edition of JSSC after being reviewed, and the best three Student Design Contest papers will be postered at the ISSCC 2009.

Plenary Talks, Panels Discussions, and Tutorials

Date	Schedule
Nov. 3rd	Tutorials
	Student Design Contest
Nov. 4th	Opening & Plenary talks
	Industry program
	Technical Sessions
	Panel Discussions
	Student Design Contest
	Banquet
Nov. 5th	Plenary talks
	Technical Sessions

Details about Plenary Talks, Panel Discussions, and Tutorials are not available at the time of this writing, but will be reported in the SSCS Fall News.

For more detailed information, please visit the following web site: www.a-sscc.org.

We look forward to seeing you in November, and hope that you will enjoy an excellent meeting and warm hospitality at the conference.

About the A-SSCC Industry Program

Spotlighting state-of-the-art technological achievements, emerging product chips, and the speed at which research results are turned to actual products, the A-SSCC Industry Program demonstrates the IC industry dynamics that have resulted in a blossoming semiconductor business in Asia. Industry Program speakers present detailed chip architectures and circuit descriptions for cutting-edge product chips and provide demonstrations and evaluation results to show how customers have improved system performance by using their chips. The A-SSCC Industry Program also provides valuable opportunities for communication that enable audiences to get intuitive business information both through oral presentations and real live demonstrations.

In the first two industry sessions in 2005, Samsung demonstrated NAND Flash memory with the highest density at the time; Renesas Technology presented a low power super SRAM with soft-error immunity. IBM and Toshiba reviewed CELL processor and wireless LAN baseband LSI capable of transmitting high-definition audio; the relationship of these products to digital visual interface and wide band CDR for digital video data was discussed.

In 2006, the Industry Program covered a wide swath of the semiconductor business, including microprocessor, memory, and analog devices. Intel reviewed the dual-core multi-threaded Xeon processor. Sun Microsystems presented UltraSPARC T1. The 2006 Industry Program also included high speed and/or low power devices including Pipeline ADC, GDDR4 SDRAM, and low power FM radio receivers.

In 2007, the two industry sessions featured "Local FC trend & computing" and "Circuits, Storage & High Speed Interface." In addition, the IT-SOC Association of Korea made a presentation on the future of Korea's fabless semiconductor industry. Intel showed the roadmap to the next generation family of processors using the world's first microprocessor in 45nm high-k metal gate process. And Sun Microsystems demonstrated the multi-core SOC (system-on-a-chip). Smart controller for mobile storage, mobile DDR SDRAM with on-chip ECC, and an embedded non-volatile memory were the the technologies presented in a session on storage and high speed interface.

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About Fukuoka

Located in Kyushu Island where many big brands like Toyota, Sony, Toshiba and Canon have their production sites, Fukuoka is the 8th largest city in Japan. Locals refer to Kyushu as "Car Island" or "Silicon Island." Fukuoka has an international airport conveniently connected to Asian countries such as Korea, China, and Taiwan.

Hot Chips 20: Three Days of the Very Best in High-performance Chips and Technologies

At Stanford University, 24-26 August, 2008

Come to the 20th annual Hot Chips conference at Stanford University's Memorial Auditorium on August 24-26, 2008. As always, Hot Chips will bring together designers, architects, and researchers of high-performance chips, software, and systems for presentations and discussions of up-to-the-minute developments.

Tutorials on Scalable Parallel Programming and Solving the "Memory Wall"

Each year, the program starts off with in-depth technical tutorials from leading practitioners. This year it will offer a Sunday morning tutorial on the challenges of solving the "memory wall"- that is, providing sufficient bandwidth and capacity to keep highly integrated multicore processors fed. The second tutorial that afternoon will be a class on NVIDIA's C-language based CUDA programming model for scalable parallel programming.

Keynote Addresses on Autonomous Vehicles and Solar Power

On the first day of the full conference, Professor Sebastian Thrun of Stanford University will speak on "Cars that Drive Themselves." Prof. Thrun led the successful Stanford Racing Team in the 2005 Darpa Grand Challenge and serves as the Director of the Stanford AI Lab, where his research focuses on robotics and artificial intelligence. Autonomous vehicles are not just for the military, but will be your car of the future.

A second keynote on the second day by Dr. Richard Swanson, who is President, Chief Technical Officer, and co-founder of SunPower, will relate the history and technology of this leading solar energy company. Dr. Swanson served as a professor of electrical engineering at Stanford University from 1976 to 1991. He holds a Ph.D. from Stanford University and bachelor and masters degrees in electrical engineering from Ohio State University.

All-Star Panel Retrospective on Successes and Failures of the Past Twenty Years

Monday night's panel in celebration of Hot Chips' 20th anniversary should be a special treat, featuring an all-star lineup of architects, analysts, entrepreneurs, and researchers discussing technology successes and failures over the last 20 years.

Moderated by Nick Tredennick, the panel will include industry analysts Michael Slater, founder of the Microprocessor Report and Microprocessor Forum in his first appearance at Hot Chips, and Nathan Brookwood, the highly quoted and quotable microprocessor pundit from Insight64. For industry and entrepreneurial experience, the panel will include Dave Ditzel, founder of Transmeta and former SPARC architect; John Mashey, early Unix and MIPS pioneer, and former chief scientist at SGI; and Howard Sachs, lead architect of the Clipper processor and now President and CEO of the video processing start-up, Telairity. Academia will be represented by David Patterson, professor of computer science at UC Berkley, RISC pioneer, and highly accomplished computer researcher.

Nine Paper Sessions on State-of-the-Art Technologies

Each of the nine Hot Chips sessions will present state-of-the-art technologies from leading companies and

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HOT CHIPS 20

1] Multi-Core Technologies
- MicroNetwork-Based Coherency: Extending Coherency over Standard Networks
- The Roofline Model: A tool for Auto-tuning Kernels on Multi-core Architectures
- Power-Performance Comparison of POWER5 &POWER6 Microprocessors

2] Video & Media
- spursEngine – Cell Derivative High-Performance Stream Processing for Media Acceleration
- A 167-processor Array for Efficient DSP & Embedded Apps Processing
- PNX5100 System Architecture and Applications: A High-Performance Full HD 120Hz Engine
- AMD media DSP: A Programmable Multicore Video Processor Platform

3] Mobile Media Processing
- A 300-mW Single-Chip NTSC/PAL Television for Mobile Applications
- Voice Processor Based on Human Hearing System
- NVIDIA APX2500: Enabling Stunning Handheld Graphics & HD Video

4] Supercomputing
- PowerXCell 8i: A Cell Broadband Engine Architecture for Supercomputing
- A Specialized ASIC for Molecular Dynamics

5] Networking
- Low Cost 200Mbps Broadband Powerline Communications ChipSet
- The QFP Packet Processing Chip Set

6] PC Chips
- AMD 780G, an x86 Chipset with Advanced Integrated GPU
- Micro-architecture of Godson-3 Multi-Core Processor
- Inside Intel's Next Generation Nehalem Microarchitecture

7] FPGAs
- Virtex-5 FXT, a New Field-Programmable Gate Array Platform
- MAXware: Acceleration in HPC
- New 40nm High Performance FPGA and ASIC Common Platform

8]Visual Computing
- NVIDIA G100: TeraFLOPS Visual Computing
- Larrabee: A Many-Core x86 Architecture for Visual Computing

9]Server Chips
- Tukwila: A Quad-Core Intel(R) Itanium(R) Processor
- SPARC64VII: Fujitsu's Next Generation Quad-Core Processor
- Rock: A 3rd Gen 65nm, 16-Core, 32+ 32 Scout Threads CMT SPARC Processor

Custom Integrated Circuits Conference (CICC) Celebrates 30th Year

More than 400 Expected on 21-24 September in San Jose

- What are the latest trends and innovative circuit techniques for analog and digital ICs?
- Where are the major research universities and industries going with ADCs, PLLs, RF-circuits, high-speed transceivers, and 3D integration?
- How are circuit designers solving the major issues today of power, variation, noise, jitter, GHz performance, system-on-chip integration, and limits to CMOS scaling?

The Custom Integrated Circuits Conference (CICC), sponsored by the IEEE Solid-State Circuits Society and technically co-sponsored by the IEEE Electron Devices Society, will address these questions in 2008, its 30th year, at the DoubleTree Hotel in San Jose, CA, the heart of Silicon Valley. The highlights of the meeting on 21-24 September will be enjoyed by an expected attendance of more than 400 professionals from leading semiconductor companies and universities.

2007 CICC Keynote Address

2007 CICC Poster Session

Dave Bergeron, this year's keynote speaker, will offer a talk entitled "More than Moore: New Directions from Older Nodes." A luncheon presentation on "The Intelligent Car: How Embedded Electronics is Changing the Automobile Business," will be presented by CEO, SVTC Prof. Alberto S. Vincentelli of UC Berkeley, and co-founder of Cadence and Synopsys.

Monday - Wednesday, September 22-24

Of over 160 technical paper presentations, the CICC Technical Program Committee especially recommends:

- A 24GS/s 5-b ADC with Closed-Loop THA in 0.18um SiGe BiCMOS
- An 8.1 mW, 82 dB Delta-Sigma ADC with 1.9 MHz BW and -98 dB THD
- Phase-Locking in Wireline Systems: Present and Future
- A Novel Dual-Band 77GHz/24GHz Frequency-Synthesizer
- MIMO Techniques for High Data Rate Radio Communications
- Linearity and Efficiency Enhancement Strategies for 4G Wireless Power Amplifier Designs
- 3D Heterogeneous Integrated Systems: Liquid Cooling, Power Delivery, and Implementation
- A 512-KB Level-2 Cache Design in 45 nm for sub-2W Low Power IA Processor Silverthorne.

Sunday, September 21

Full-day educational sessions, with three technical tracks and one half-day focused on technical writing and presentation:

- Fundamentals of Analog Design
- High-Speed Serial IO Design
- Coping with Scaling
- Technical Writing and Presentation

Monday & Tuesday, Sept 22 & 23

- Poster Presentation
- Vendor Exhibit
- Circuit/System Demonstration

Additional information including the complete advance program and registration form is available on the CICC website: www.ieee-cicc.org

For specific inquiries about the CICC, please contact the Conference Manager, Melissa Widerkehr, CICC, 19803 Laurel Valley Place, Montgomery Village, MD 220886, Email: cicc@his.com, Tel: (301) 527-0900/101.

Sister Conferences ESSCIRC/ESSDERC Meet on 15-19 September

The 2008 European Forum for Solid-State Circuits is in Edinburgh, Scotland

The increasing level of integration for system-on-chip design made possible by advances in silicon technology requires a deeper interaction among technologists, device physicists and circuit designers. Therefore, this year's ESSCIRC/ESSDERC conferences at the Edinburgh International Conference Centre (EICC) will share plenary keynote presentations and joint technical sessions on topics that bridge both communities, while keeping separate Technical Programs.

Joint ESSCIRC/ESSDERC Plenary Talks

Distinguished invited speakers will discuss issues of interest for the attendees of both conferences:

- R. Chau (Intel Corporation) "Nanotechnology for Future High-Speed and Energy-Efficient CMOS Applications"
- C. van Hoof (IMEC) "Micropower energy Scavenging"
- T. Sakurai (University of Tokyo) "Low leakage digital design and variability"
- V. Subramanian (University of California) "Printed electronics for low-cost electronic systems: technology status and application development"
- M. Thompson (ST Microelectronics) "More than Moore and More Moore in Europe"
- V. Manian (Broadcom) "Technology Interfacing for Fabless Semiconductor Companies"

Attendees registered for either conference are encouraged to attend any of the scheduled parallel sessions.

Joint ESSCIRC/ESSDERC Sessions

Focusing on topics where technology and design issues are closely linked and of shared interest, these sessions are expected to include:

- Sensors and Imagers
- Integration of IC designs with other technologies and materials
- Yield and Reliability related technology developments
- Design for Manufacture.

Plenary Talks at ESSCIRC

Cosponsored by the IEEE Solid-State Circuits Society, ESSCIRC provides an annual European forum for the presentation and discussion of recent advances in solid-state circuits.

Prominent invited speakers will address issues of specific interest to the integrated circuit design community:

- T. Demisen (Medtronic) "Ultralow power for biomed"
- M. Berkhout (NXP) "Audio at low and high power"
- Y. Hagihara (Sony) "SOI design for the CELL processor"

ESSCIRC Papers

Analog Circuits

Analog circuits including small signal amplifiers; variable gain amplifiers; power audio amplifiers; continuous-time & discrete-time filters; comparators; instrumentation and sensor interfaces; voltage references, LDO regulators, DC-DC converters; HV circuits; lighting control.

Data Conversion Circuits and Integrated Systems

Nyquist-rate and oversampled A/D and D/A converters; sample-and-hold-circuits; A/D and D/A converter calibration and error correction circuits.

RF Circuits

RF/IF/baseband circuits including: LNAs; mixers; IF amplifiers; power amplifiers; power detectors; active antennas; modulators; demodulators; VCOs; frequency dividers; frequency synthesizers; PLLs.

Wireless and Wireline Communication Circuits

Receivers/transmitters/transceivers for wireless systems, base stations and hand-sets; advanced modulation systems; TV/radio/satellite receivers; Ultrawideband and data links; wireless sensor networks; RFID.

Sensors, Imagers, MEMS, Bioelectonic Integration

Sensor subsystems and interfaces; accelerometers; temperature sensing; imaging circuits; MEMs subsystems; RF MEMs; bioelctronics systems; implanted electronic ICs, telemetry.

Digital and Memory Circuits

Digital circuit techniques; I/O and interchip communication; reconfigurable digital circuits; clocking; memories; microprocessors.

Digital Signal Processing and Arithmetic
DSPs and DSP kernels, signal processing and arithmetic building blocks.

Nanoelectronics
Digital, analogue and mixed signal circuits using emerging devices such as multi-gate MOSFETs (Double-Gate MOSFETs; FinFETs, Triple-Gate MOSFETs); nanowires/nanotubes and quantum devices.

A Tutorial Day will be organized on Monday 15 September 2008, while a Workshop Day will take place on Friday 19 September 2008.

Tutorials
- CMOS at the bleeding edge
- Nanoelectronics: how far and reliably can we probe essential structural information?
- Integrating CMOS with other Technologies

Workshops
- CMOS variability research in Europe: From Atomic Scale to Circuits and Systems
- Electronic cubes: a More-than-Moore platform for Wireless Sensor Nodes exploiting the 3rd Dimension
- Germanium and III-V MOS technology
- MOS-AK: Towards Nano Compact Modeling
- BIES: Brain-Inspired Electronic Systems
- Si-based Nanodevices for ultimate CMOS and Beyond-CMOS
- Tradeoffs and Optimization in Analog CMOS

More information is available at the conference website: www.esscirc2008.org

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2008 IEEE BIPOLAR/BICMOS Circuits and Technology Conference (BCTM) to Meet in Monterey in October

Collocated for the first time this year with the 2008 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS), the 2008 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM) will be held from Monday, October 13 through Wednesday, October 15, 2008 at the Portola Plaza Hotel in beautiful Monterey, California.

Situated along the coast of California just 115 miles from San Francisco, Monterey is easily accessible from multiple airports. Monterey is the home of the world-class Monterey Bay Aquarium, located on the street immortalized in John Steinbeck's novel Cannery Row, and features renowned events, such as the annual Monterey Jazz Festival. The area has numerous attractions including the Big Sur, Fisherman's Wharf, the Pebble Beach Golf Resort and wonderful restaurants, hotels, galleries, and shops. You are also just a short drive away from some of California's finest wineries.

Everyone interested in the leading edge processes, devices, and circuits used in state-of-the-art telecommunications and power control systems will not want to miss BCTM, which focuses on bipolar and BiCMOS technologies -- particularly SiGe HBT BiCMOS -- that continue to play a key role in these systems.

The conference will start with a one-day short course, followed by two full days of contributed and invited papers, including a special session on Emerging Technologies.

A luncheon with guest speaker, exhibits, and an evening banquet will roll out the program. Booths will feature the latest products of interest to the bipolar community. And papers covering the design, performance, fabrication, testing, modeling, and application of bipolar and BiCMOS integrated circuits, bipolar phenomena, and discrete bipolar devices will be presented. On Tuesday evening, the BCTM Banquet will be held at the Chateau Julien Wine Estate where you will be able to connect with your colleagues and make new acquaintances.

As this year's keynote speaker we are fortunate to have Dr. Gil Amelio, the CEO of Jazz Semiconductor, who will discuss "Technology Convergence Creating New Opportunities for Innovation." This is a great opportunity to meet Dr. Amelio and learn about the latest technologies designed to produce analog-intensive mixed-signal (AIMS) semiconductor

devices including high performance telecommunication systems.

The plenary session will feature six invited talks:

- "Special RF/_Wave Devices in Silicon-on-Glass Technology," Lis Nanver (TU Delft)
- "Silicon Front-End Integration," J. Costa (RFMD)
- "High-Speed A/D & D/A Conversion: A Survey," J.B. Begueret (IMS Bordeaux)
- "Digital Control Power - The Key to Intelligent Energy Efficiency," Manfred Schlenk (Infineon)
- "From Measurement to Intrinsic Device Characteristics: Test Structures and Parasitics Determination," F. Pourchon (ST Microelectronics)
- "Highly-Efficient Wideband Monolithic RF Polar Transmitters Using Envelope-Tracking," D. Lie (Texas Tech University)

The short course will include five renowned experts on "100 Gbps Ethernet and High-Speed Data Converters." Short course invited talks will be:

- "High-speed SiGe BiCMOS technologies for applications beyond 40 Gb/s," Pascal Chevalier (STMicroelectronics)
- "High-speed data converters for 10+Gb/s applications," Peter Schvan (Nortel)
- "System architectures and circuits for 100 Gb/s Ethernet applications," Yves Baeyens, Lucent-Alcatel Bell Labs

We look forward to welcoming you at BCTM 2008.

Find full details and registration information for the conference on the BCTM web page (www.ieee-bctm.org/).

See you in Monterey!

Marise Bafleur
General Chair, 2008 BCTM
LAAS-CNRS, Toulouse FRANCE

2008 IEEE Compound Semiconductor IC Symposium (CSICS) to Collocate with BCTM in October

You are cordially invited to the 2008 IEEE Compound Semiconductor IC Symposium (CSICS) on October 12 – 15th in beautiful Monterey, California. Collocated for the first time in 2008 with the IEEE Bipolar / BiCMOS Circuits and Technology Meeting (BCTM), it is the ideal forum for the latest results in high-speed digital, analog, microwave/millimeter wave, mixed mode, and opto-electronic integrated circuits. Joint functions will include an afternoon session and social functions, and an exhibition permitting cross-fertilization of ideas between the two technical meetings.

For over 30 years, CSICS has been the preeminent international forum for presenting and debating advances in semiconductor circuit and device technology. The scope of the Symposium encompasses devices and circuits in GaAs, SiGe, InP, GaN, and InSb as well as the fields of RF/mm-Wave CMOS and high-speed digital CMOS to provide a truly comprehensive conference.

Due to impressive strides in new materials and devices, greater integration levels, novel circuit implementations, and ever-changing systems partitions, the high-performance wireless and high-speed digital communications markets are thriving. Compound materials are now used in modern silicon CMOS and BiCMOS technologies to enhance their performance. With its HfO_2 gate stack, SiGe source/drain regions for hole mobility enhancement, the use of insulated substrates like SOI and SOS to reduce parasitics, even 45nm CMOS technology has joined the fray of compound semiconductors.

The 2008 CSIC Symposium will offer a full three-day technical program, two short courses, a primer course, and a technology exhibition. The technical program will consist of approximately 60 high quality state-of-the-art technical papers, four panel sessions, two Short Courses on "Phased Arrays (Technology, Systems and Circuits)" and "A Modeling Toolbox for RF Designers," plus an Industry Exhibit. The Symposium will also offer the popular annual introductory level Primer Course on "Basics of Compound Semiconductor ICs." This year, the Symposium will feature approximately 15 invited papers on a wide range of important topics encompassing device engineering to circuit application using advanced compound and other related semiconductor technologies. In addition, the Symposium will continue the tradition of including important "late breaking news" papers.

The CSICS Technology Exhibition will take place in the Monterey Convention Center adjacent to the Portola Plaza Hotel. The close proximity of the Exhibition and the technical sessions will promote a highly integrated experience for our attendees. The Exhibition will also offer our vendors an opportunity to showcase various products and services including specialty semiconductor materials (epitaxy, substrates, high purity gases and related compounds), manufacturing

equipment including photolithography, etch, thin films, ion implantation, wafer surface analysis and metrology equipment and services, test and characterization equipment, simulation and modeling software, and complete foundry services for GaAs and related compound semiconductor technologies. More information on the CSICS Exhibition can be found on our website or by contacting the Exhibition Manager, Sue Kingston, at s.kingston@ieee.org.

Several social events will complement the Symposium, including the Sunday Evening CSICS Opening Reception, the Monday CSICS Exhibition Opening Reception, the CSICS-BCTM Tuesday evening Theme Party, and the CSICS Exhibition Luncheon on Tuesday. The Theme Party will take place at the Chateau Julien Wine Estate, nestled in the Carmel Valley mountains. The theme party will include musical entertainment from a French/Italian opera accordion player and a Paraguayan harpist, wine tasting of world famous Monterey wines, discussions on wine making processes, Bocci ball, tours of the vineyard and estate, and grape stomping. Breakfasts and coffee breaks will also be served on Monday, Tuesday, and Wednesday.

The Portola Hotel in downtown Monterey is 115 miles south of San Francisco and 350 miles north of Los Angeles. Monterey features a dazzling waterfront, a lush urban forest, a rich array of historic and cultural resources, museums, gardens, recreational activities and a wide variety of special events throughout the year. The city's rich history includes Spanish exploration dating back to 1542, and the establishment of the San Carlos Cathedral by Father Junipero Serra in 1770. It was the site of Alta California's capital under Spain and later Mexico, and the place where California statehood began in 1849.

For registration and further information please visit the CSICS website at www.csics.org. Further questions may be addressed to the Symposium Chair: William Peatman, Ph:1-908-668-5000 Ext 5842 Email: wpeatman@anadigics.com

We hope you can attend,

2008 IEEE CSICS Organizing Committee,
Sorin Voinigescu, University of Toronto,
sorinv@eecg.toronto.edu

Hot Chips 20 *continued from page 78*

researchers offering fresh insights on topics ranging from voice processing to supercomputer designs:

The first session on the first day of the main conference will explore the challenges of building high-performance multicore processor systems with presentations on interconnects, software, and optimized power.

The second, media and video, session will look at various approaches to streaming media processing: a modified Cell processor (Toshiba); a many-core processor array (UC Davis); a custom designed engine (NXP Semi); and a programmable multi-core video processor approach (AMD).

For mobile devices, the added factor of battery life and system size constraints must be considered in addition to performance. Presentations will explore different challenges of mobile applications such as mobile television (Telegent); audio processing using complex models of the human hearing system (Audience); and a full SoC applications processor with HD capability for handsets (NVIDIA).

Supercomputing, the topic of the fourth session, is becoming more relevant to mainstream computer designers as costs keep coming down and new commercial markets with high computational needs grow in importance. The two specific approaches to be discussed in this session are: an enhanced version of the Cell processor with improved support for double-precision math; and a very specialized ASIC designed to solve a specific scientific challenge.

The Networking session at the start of the second day will include presentations on a dedicated chipset from Cisco, and a low cost powerline chipset from DS2.

The, fifth, PC Chips, session will cover a diverse group of chips with details about Intel's next generation PC and mainstream server processor (Nehalem); AMD's latest integrated graphics chipset; and a processor developed by the Chinese Academy of Sciences for a computer design.

In the FPGA session, the two perpetual leading competitors, Altera and Xilinx, will face off with their very latest chips and platforms. As fewer companies can rationalize the cost of developing custom chips at the leading-edge semiconductor process, FPGAs are becoming more important. FPGAs can offer leading-edge process chips to designers and researchers.

And speaking of face-offs, the Visual Computing session will host the first ever head-to-head meeting of NVIDIA's latest GPU technology and Intel's Larrabee project. This session should not be missed!

Finally we will wrap up the show with a multicore server processor showdown with Intel's forthcoming Itanium processor (Tukwila) facing two SPARC processors, one from Sun Microsystems ("Rock") and the other from Fujitsu (SPARC64 VII).

Hot Chips is a great conference, with great content, a great community, at a great locale. Come and experience it for yourself.

Don Draper, General Chair,
Hot Chips 20

SSCS-Green Mountain Organizes 17th IEEE North Atlantic Test Workshop

IEEE NATW Special Session on Solid-State Circuits & System Test Held on 14-16 May, 2008

Pascal Nsame, SSCS-GM Chapter Chair, pnsame@us.ibm.com

For the first time this year, the IEEE North Atlantic Test Workshop (NATW) included a special session on solid-state circuits and system test. Sponsored by the SSCS-Green Mountain chapter at the Holiday Inn in Boxborough, Mass. on May 14-16, 2008, the conference served as a forum for discussions on the latest issues relating to high quality, economical, and efficient testing methodologies and designs.

Special SSCS Session Highlights System Resiliency

The special SSCS session discussed both technical and business implications of technological and system resiliency challenges, featuring presentations on three aspects of this crucial problem:

- Advances in Built-in Self-Test for 65nm and 45nm technology nodes
- Adaptive Test
- On-product reliability testing.

The contributions in these papers demonstrated significant technical advances toward addressing system resiliency challenges and covered issues, possibilities, limitations and future needs.

High reliability, fault protection and high resiliency are key requirements for high-performance systems. Embedded processors and embedded memory macros are having an ever increasing impact on system resiliency, not only in servers, high-performance computing, enterprise storage and data centers, but also in gaming and digital multimedia applications.

"Improving Memory BIST Value in a Tough Real Estate Market," by M. Ouellette, M. Ziegerhofer, V. Chickanosky, S. Granato, P. Rachakonda, C. Mirashi, S. Jinagar and K. Gorman (IBM)

A programmable BIST architecture and fuse circuit design that supports at-speed test with reduced test/repair circuit overhead, this paper featured an embedded serial BIST control interface allowing for in-system and diagnostic capabilities.

"Cost-Benefit Analysis for Functional Pattern Test Time Management," by M. Lee, M. Grady, M. Johnson (IBM)

A cost-benefit analysis methodology for test pattern efficiency, identifying actions that could be taken to help keep test escapes and quality impacts to a minimum while allowing adaptive test pattern reduction.

"On-Chip Circuit for Monitoring Degradation Due to NBTI," by K. Stawiasz, K. Jenkins and P-F. Lu (IBM)

A circuit implementation with sufficient accuracy, resolution and power supply noise immunity to enable the characterization of NBTI-induced frequency degradation on product chips under typical product operating voltage and temperature.

More information about the 2008 NATW can be found at: www.ewh.ieee.org/r1/vermont/

SSCS-Green Mountain Chair Pascal Nsame presented certificates of appreciation to Mike Ouellette (left), Matt Grady (center) and Kevin Stawiasz (right) at the special SSCS session of the IEEE North Atlantic Test Workshop (NATW) in May, 2008.

Oregon State University Student Branch Chapter Inaugurated in March

Prof. Tom Lee Presents a History of Radio

Sunwoo Kwon, OSU Chapter Chair, David Gubbins, Chapter Co-Chair, and Pavan Kumar Hanumolu, Advisor, sunnyk, gubbins, and hanumolu@eecs.oregonstate.edu

As its inaugural activity, the Oregon State University (OSU) SSCS Student Branch Chapter hosted a presentation by SSCS distinguished lecturer Thomas H. Lee entitled "A Very Nonlinear History of Radio" on March 14, 2008. Over 100 people, including faculty, attended the informative and entertaining seminar at Covell Hall on the OSU campus.

In his talk, Prof. Lee, of Stanford University, relayed the history of radio from the late 19th century, when people could barely think of "wired communication." He also remarked on contributors to the field who have not frequently been acknowledged and discussed recent and future trends.

The OSU chapter wishes to thank Prof. Lee for his insights, and the School of Electrical Engineering and Computer Science at OSU for its support and help in organizing this seminar.

Prof. P. Hanumolu, Chair of the SSCS Student Branch chapter at Oregon State University (left) introducing Distinguished Lecturer Tom Lee on March 14, 2008.

The OSU SSCS student chapter was founded in 2007 to help students interact and communicate with experts by hosting events featuring SSCS distinguished lecturers and other professionals. Moreover, the chapter wants to encourage electrical engineering students to join the SSCS by demonstrating what we do and what we intend to do through the Engineering Expo at OSU and other local activities. To broaden each member's fields of interest, we plan to invite at least two distinguished lecturers a year and other professionals, too. We have also scheduled replays of each year's ISSCC tutorial slide/CDs.

From left: Prof. P. Chiang, Prof. P. Hanumolu, Prof. K. Mayaram, Prof. T. Lee, Prof. T. Fiez, Prof. U. Moon, and Prof. A. Weisshaar after Dr. Lee's DL talk at Oregon State University in March.

Sansen and Matsuzawa Visit National Taiwan University

Meeting and Seminars in April Organized by SSCS-Taipei Chapter

SSCS President Willy Sansen and AdCom member Akira Matsuzawa presented seminars at National Taiwan University and met with NTU President Prof. Si-Chen on 24 April, 2008.

At the meeting, which was cosponsored by NTU-Mediatek Wireless Laboratory and SSCS-Taipei and included NTU Prof. C. K. Wang, the Society's Region 10 Representative, everyone shared their views on the rapid growth of the IC design and foundry industries in Taiwan. All agreed that the IC design field has recently advanced both in industry and academia due to strong government support, high-quality engineering students and engineers, and good infrastructure. NTU in particular has recently made great contributions to ISSCC and has had a significant number of papers accepted for it. The group concurred that NTU can continue to play an important role in the IEEE Solid-State Circuits Society and its premier conference.

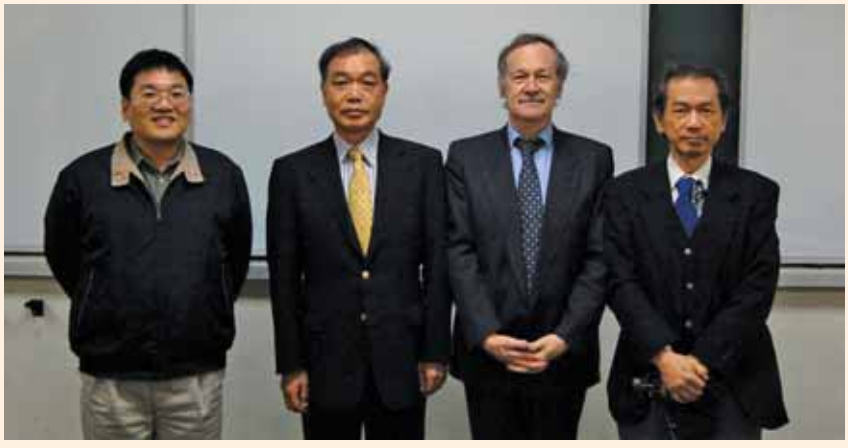
From left: Prof. Akira Matsuzawa, Prof. Si-Chen Lee (NTU President), Prof. Willy Sansen, and Prof. Chorng-Kuang (C.-K.) Wang, after their meeting on 24 April at National Taiwan University, Taipei, Taiwan.

Seminars on the Future of Moore's Law and High Speed ADC's

In a lecture entitled "More Moore or More than Moore," Prof. Willy Sansen of K. U. Leuven termed the continuing advancement of microelectronics technologies which has sustained Moore's Law "More Moore." On the other hand, he termed the emerging trend toward applications requiring the integration of sensor, power-scavenging devices and MEMS structures which are often implemented in conventional but cheaper technologies "More Than Moore." The design considerations and trade-offs for both were discussed and illustrated in his talk.

In a second talk entitled "High speed ADCs: History and Future," Prof. Akira Matsuzawa of the Tokyo Institute of Technology reviewed and summarized the essence of circuit design and the conversion architecture of high speed ADC's. He also showed how IC designers can contribute to the progress of electric systems and products and discussed the technology direction of ADC's, particularly those related to low-voltage nano-scale CMOS technology.

The seminars attracted an audience of about 30 people, most of them NTU faculty and students. Prof. Sansen also attended the 2008 VLSI-DAT (Design, Automation, and Test) Symposium in Hsinchu, Taiwan on April 23-25, 2008, where he delivered a keynote speech entitled "Efficient Analog Signal processing in nm CMOS Technologies."



From left: Prof. Shen-Iuan Liu (SSCS-Taipei Chapter Chair), Prof. Akira Matsuzawa, Prof. Willy Sansen, and Prof. Chorng-Kuang (C.-K.) Wang after seminars by Prof. Sansen and Prof. Matsuzawa at National Taiwan University, Taipei, Taiwan.

C. K. Wang,
National Taiwan University,
ckwang~cc.ee.ntu.edu.tw

Eight Candidates Vie for Five AdCom Positions

Anne O'Neill, Executive Director, SSCS, a.oneill@ieee.org

The SSCS Nominations Committee has announced a slate of eight candidates for five AdCom positions from 2009-2011. Tohru Furuyama, Bruce Gieseke, and Ken O are new candidates; Ali Hajimiri, Paul Hurst, and Ian Young are incumbents. C.K. Wang and Domine Leenaerts currently serve on the AdCom as appointed members.

The AdCom is the governing body of the Solid-State Circuits Society, overseeing conferences, publications, educational activities, chapters, finances, and other areas relevant to the Society's scope. Elected AdCom members serve three-year terms, which are staggered so there are always some experienced and new members.

SSCS members who are eligible to vote will be sent an email in the fall to verify their email address in the IEEE member record. A few days later, an email ballot message to login online will follow with a custom election login included in the email. Members residing in areas where postal ballots would take a long time to reach headquarters in New Jersey are especially urged to use the online system. The Society is interested that its global community participate in Society elections. As a precaution, hard copy ballots are mailed to all eligible voting members in the fall. Voting only once will speed the counting of the return. Please vote using only one method, online or hard copy, not both.

For those interested in petitioning for an additional candidate to be on the ballot, please see the instructions in the sidebar.

The Candidates

Tohru Furuyama (S'83-M'84-SM'05-F'06) received the B.S. degree from the University of Tokyo, Tokyo, Japan, the M.S. degree from Cornell University, Ithaca, NY, and the Ph.D. degree from the University of Tokyo. He is with Toshiba Corp. Dr. Furuyama developed several commodity DRAM's and the first Rambus DRAM and he also led one of the first embedded DRAM projects for graphics application LSI's. From 1994 to 1996, he was the 64Mb DRAM design manager for the Toshiba/IBM/Siemens joint DRAM development project in Burlington, VT. As a general manager of the Center for Semiconductor Research & Development, he has been responsible for various R&D activities, advanced CMOS technologies, NAND flash memories, embedded memories, novel memories, embedded processors (MeP: Toshiba proprietary Media embedded Processor), digital media SoC's and related software since 2002.

Dr. Furuyama is presently the Japan Chapter Chair of the IEEE Solid-State Circuits Society. He served on the Technical Program Committees of ISSCC (IEEE International Solid-State Circuits Conference) and ITC (IEEE International Test Conference). He is the Technical Program Committee Co-Chair of the 2008 A-SSCC (IEEE Asian Solid State Circuits Conference) and will be the TPC Chair of the 2009 A-SSCC. He has been a lecturer at the Tokyo Institute of Technology since 2004. He authored and co-authored more than 40 journal and conference papers and holds over 70 U.S. patents. He is an IEEE Fellow for contributions to high speed dynamic random access memory (DRAM) design and technology.

Bruce Gieseke received the B.S.E.E. degree from the University of Cincinnati, Cincinnati, OH in 1984 and the M.S.E.E. degree from North Carolina State University, Raleigh, NC in 1985.

In 1986, he joined Digital Equipment Corporation, Hudson, MA, where he contributed to Digital's ALPHA microprocessor programs, including the 21264 which he co-managed as a Senior Consulting Engineer.

In 1997, he joined Advanced Micro Devices (AMD), Sunnyvale, CA, contributing to AMD's seventh- and eighth-generation microprocessor designs including the Athlon, Opteron, Sempron, and

Turion microprocessors. He is currently Vice President and Corporate AMD Fellow responsible for next generation microprocessor core development.

In 1999, he joined the Symposium on VLSI Circuits' North American & European Technical Program Committee where he filled several roles. In 2003/2004 he was the Technical Program Co-Chairman/Chairman, and in 2005/2006 the Symposium Co-Chairman/Chairman. Currently, he is a member of the Executive Committee for the conference.

Ali Hajimiri received the B.S. degree in Electronics Engineering from the Sharif University of Technology, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University in 1996 and 1998, respectively.

He was a Design Engineer with Philips Semiconductors, where he worked on a BiCMOS chipset for GSM and cellular units from 1993 to 1994. In 1995, he was with Sun Microsystems, where he worked on the UltraSPARC microprocessor's cache RAM design methodology. During the summer of 1997, he was with Lucent Technologies (Bell Labs), Murray Hill, NJ, where he investigated low-phase-noise integrated oscillators. In 1998, he joined the Faculty of the California Institute of Technology, Pasadena, where he is a Professor of Electrical Engineering and the director of the Microelectronics Laboratory. His research interests are high-speed and RF integrated circuits.

Dr. Hajimiri is the author of The Design of Low Noise Oscillators (Boston, MA: Springer, 1999) and has authored and coauthored more than one hundred refereed journal and conference technical articles. He holds more than two dozen U.S. and European patents. He is a member of the Technical Program Committee of the International Solid-State Circuits Conference (ISSCC). He has also served as an Associate Editor of the IEEE Journal of Solid-State Circuits (JSSC) and of IEEE Transactions on Circuits and Systems (TCAS): Part-II. He has been a member of the Technical Program Committee of the International Conference on Computer Aided Design (ICCAD), Guest Editor of the IEEE Transactions on Microwave Theory and Techniques, and served on the Guest Editorial Board of Transactions of the Institute of Electronics, Information and Communication Engineers of Japan (IEICE).

Dr. Hajimiri was selected to the top 100 innovators (TR100) list in 2004 and is a Fellow of Okawa Foundation. He is a Distinguished Lecturer of both the IEEE Solid-State Circuits and Microwave Societies. He is the recipient of Caltech's Graduate Students Council Teaching and Mentoring award as well as the Associated Students of Caltech Undergraduate Excellence in Teaching Award. He was the Gold Medal winner of the National Physics Competition and the Bronze Medal winner of the 21st International Physics Olympiad, Groningen, Netherlands. He was a co-recipient of the IEEE Journal of Solid-State circuits Best Paper Award of 2004, the International Solid-State Circuits Conference (ISSCC) Jack Kilby Outstanding Paper Award, two times co-recipient of CICC's best paper awards, and a three-times winne of the IBM faculty partnership award as well as the National Science Foundation CAREER award. He is a co-founder of Axiom Microdevices Inc.

Paul J. Hurst (S'76-M'83-SM'94-F'01) received the B.S., M.S., and Ph.D. degrees in electrical engineering from UC Berkeley in 1977, 1979, and 1983, respectively.

From 1983 to 1984, he was with UC Berkeley as a lecturer, teaching integrated-circuit design courses and working on a MOS delta-sigma modulator. In 1984, he joined the telecommunications design group of Silicon Systems Inc., where he was involved in the design of mixed-signal CMOS integrated circuits for voice-band modems.

Since 1986, he has been on the faculty of the Department of Electrical and Computer Engineering at UC Davis, where he is now a Professor.

His research interests are in the area of analog and mixed-signal integrated-circuit design for signal processing and communication applications.

Research projects have included data converters, filters, image processing, and adaptive-equalizer and timing-recovery circuits for data communications. He is a co-author of a college text book on analog integrated-circuit design.

1. Advanced Analog CMOS IC Design

Monday, September 29

E. Vittoz
- MOS: Modes of Operation and Models
- Passive Components and Parasitic Effects
- Layout Techniques for Analog Circuits
- Elementary Building Blocks

Tuesday, September 30

E. Vittoz
- Elementary Building Blocks
- Voltage References

H. Casier
- Technology Effects and Other Limitations for Mixed-Signal ASICs

Wednesday, October 1

W. Sansen
- Analog Functional Blocks

Thursday, October 2

H. Casier
- BICMOS Analog Building Blocks
- Design for EMC

L. Lewyn
- Reliability Issues in Nanoscale Analog CMOS Technologies
- Physical Design Issues in Nanoscale Analog CMOS Technologies

Friday, October 3

G. Temes
- Switched-Capacitor Circuit Design

2. High-Speed Data Converters for Communications

Monday, September 29

M. Pelgrom
- Fundamental Limitations in High-Speed Data Converters
- Flash ADCs

Tuesday, September 30

M. Pelgrom
- System Aspects of ADCs

U.-K. Moon
- Low-Voltage Pipelined ADCs

Wednesday, October 1

I. Galton
- Overview of Pipelined ADCs
- Digital Background Calibration of Circuit Errors in Pipelined ADCs
- Understanding and Using Power Spectral Densities for ADC Simulation, Test, and Debug

L. Lewyn
- Precision Comparator Design for High Speed Data Converters in Nanoscale CMOS Technologies

Thursday, October 2

B. Jewett
- Case Study of a 1.2-GSa/s 15-bit DAC
- Case Study of an 8-bit 20GS/s ADC

R. Sheppard
- Designing with Communications Data Converters in Real RF Systems
- Performance Criteria for Data Converters, Basics and Metrics

Friday, October 3

R. Sheppard
- Test and Trouble Shooting Methods to Determine Performance
- Practical Guidelines for Designing with High-Performance Data Converters

3. Optimized Amplifier Design

Monday, September 29

W. Sansen
- Comparison of MOST and Bipolar-Transistor Model
- Single-Transistor Amplifying Stage
- Dual-Transistor Amplifying Stages
- Noise Performance of Amplifying Stages

Tuesday, September 30

W. Sansen
- Stability of Operational Amplifiers
- Systematic Design of Operational Amplifiers
- Important Opamp Configurations
- Exercise on Amplifier Optimization

Wednesday, October 1

J. Cowles
- Unique Aspects of Design using Bipolar Transistors
- The Current-feedback Amplifier: Benefits and Trade-offs

B. Gilbert
- BJT Wideband Amplifiers: Single-Sided and Differential
- A Survey of High-Performance Variable-Gain Amplifiers

Thursday, October 2

W. Sansen
- Offset and CMRR; Random and Systematic
- Fully-Differential Operational Amplifiers
- Design of Multistage Operational Amplifiers
- Exercise on Fully-Differential Amplifiers

Friday, October 3

W. Sansen
- Rail-to-Rail Amplifiers
- Class –AB Amplifiers
- Optimization of Transimpedance Amplifier

4. H-S Broadband Communications, Signals & Circuits

Monday, September 29

M. Green
- Characteristics of Broadband Signals and Systems
- Fundamentals of Phase-Locked Loops and Clock Recovery Circuits

Tuesday, September 30

M. Green
- CMOS Design Techniques for High-Speed Broadband IC's
- Voltage-Controlled Oscillators, Phase Noise, Random Jitter, and Bit Error Rate

Wednesday, October 1

E. Sackinger
- Broadband Circuits for Optical Fiber Communication

Useful Information

Course Location

World Trade Center, 121 SW Salmon Street, Portland, OR 97204

For additional information contact:

MEAD Microelectronics, Inc., 7100 NW Grandview Drive, Corvallis, OR 97330
Telephone: (541) 758-0828, Fax: (541) 752-1405
Email: valence@mead.ch (technical questions) or
usmead@cmug.com (administrative questions)

For programs, fee and registration information, please visit our web site:

www.mead.ch

Deadline for early registration is August 1, 2008

He is also active as a consultant to industry.

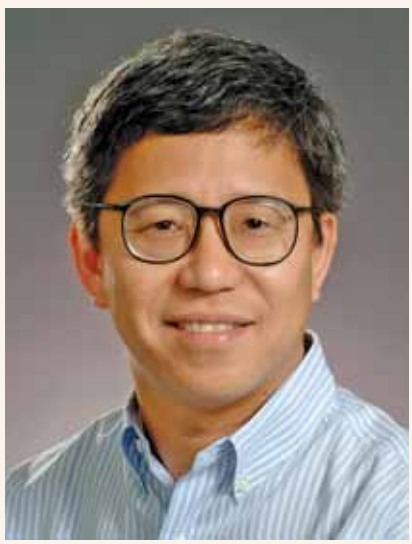
Paul Hurst has served on the program committees of the International Solid-State Circuits Conference and the Symposium on VLSI Circuits. He was guest editor for one issue of the Journal of Solid-State Circuits. He served as associate editor for the Journal of Solid-State Circuits for five years (2001-2006). He was an elected member of the administrative committee of the IEEE Solid-State Circuits Society in 2006-2008. He was elected IEEE Fellow in 2001.

Domine M. W. Leenaerts (M'94-SM'96-F'2005) received the Ph.D. degree in electrical engineering from Eindhoven University of Technology, Eindhoven, the Netherlands, in 1992.

From 1992 to 1999, he was with Eindhoven University of Technology as an Associate Professor with the Micro-electronic Circuit Design group. In 1995, he was a Visiting Scholar in the Department of Electrical Engineering and Computer Science at UC Berkeley. In 1997, he was an Invited Professor at Ecole Polytechnique Federale de Lausanne, Switzerland. From 1999 to 2006 he was a Principal Scientist with Philips Research Laboratories in Eindhoven, where he was involved in RF integrated transceiver design. In 2006, he moved to NXP Semiconductors, Research as Senior Principal Scientist.

He has published over 150 papers in scientific and technical journals and conference proceedings. He holds several US patents and coauthored several books, including Circuit Design for RF Transceivers (Boston, MA: Kluwer, 2001).

Dr. Leenaerts served as IEEE Distinguished Lecturer in 2001-2003 and served as Associate Editor of the IEEE Transactions on Circuits and Systems-Part I (2002-2004) and of the IEEE Journal of Solid-State Circuits since 2007. He currently represents the IEEE Circuits and Systems Society on the IEEE Solid-State Circuits Society Administrative Committee. Dr. Leenaerts also serves on the Technical Program Committee of the European Solid-State Circuits Conference, the IEEE Radio Frequency Integrated Circuits Conference (RFIC), and the IEEE International Solid-State Circuits Conference (ISSCC).



Kenneth O received his S.B, S.M, and Ph.D. degrees in Electrical Engineering and Computer Science from the Massachusetts Institute of Technology, Cambridge, MA in 1984, 1984, and 1989, respectively. From 1989 to 1994, he worked at Analog Devices Inc. developing sub-micron CMOS processes for mixed signal applications and high speed bipolar and BiCMOS processes for RF and mixed signal applications. He is currently a professor at the University of Florida, Gainesville. His research group (Silicon Microwave Integrated Circuits and Systems Research Group) is developing circuits and components required to implement analog and digital systems operating between 1 GHz and 1 THz using silicon IC technologies.

He was the general chair of the 2001 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM) and was the guest editor of a Special Issue on BCTM in the 1996 IEEE Journal of Solid-State Circuits. He served as an associate editor for the IEEE Transactions on Electron Devices from 1999 to 2001. Dr. O has also served as the publication chairman of the 1999 International Electron Device Meeting. Since 2003, he has been the Solid-State Circuits Society liaison to the IEEE RFIC Symposium, as well as a member of the Steering Committee for the RFIC Symposium. He has authored and co-authored approximately 170 journal and conference publications, and holds nine patents. Dr. O received the 1996 NSF Early Career Development Award and the 2003 UF Ph.D./Mentor Award. He also held a UF Research Foundation Professorship from 2004-2007.

Chorng-Kuang (C.K.) Wang was born in Taiwan in 1947. He received

the B.S. degree in electronic engineering from National Chiao Tung University and the M.S. degree in Geophysics from National Central University, Taiwan in 1970 and 1973, respectively. He received the M.S. and Ph.D. degrees in Electrical Engineering and Computer Science from the UC Berkeley in 1979 and 1986, respectively, where he worked on MOS analog integrated circuits using scaled technologies.

Wang has held industrial positions with Itron in Taiwan (1973-1977), National Semiconductor, Rockwell and IBM in California (1979-1991), where he was involved in the development of CMOS memory, data modems and disk-drive integrated circuits. He acted as a consultant to the Computer & Communication Research Lab of the Industrial Technology Research Institute (1991-2000) and an advisor to the Ministry of Education Advisory Office in Taiwan (1997-2001). From 1991 to 1998, he was with the Department of Electrical Engineering, National Central University in Taiwan, where he was a Professor. Thereafter, he has been a professor in the Department of Electrical Engineering of National Taiwan University. His research interests are in the areas of wireless transceiver system and circuit design, high-speed data link circuits, mm-wave CMOS development, and flexible electronics. He has been involved in chairing and launching programs for technical and executive committees of APASIC, A-SSCC and ISSCC. He currently serves as an ex-officio member of the SSCS AdCom, and is a member of the IEEE Donald O. Pederson Award Solid-State Circuits Committee. Prof. Wang was elevated to IEEE Fellow in 2008.

Ian Young is a Senior Fellow and Director of Advanced Circuits and Technology Integration in the Technology and Manufacturing Group at Intel Corporation. He does research and development of mixed-signal circuits for microprocessor, communications and SOC products along with process technology development.

Young joined Intel in 1983. Starting with the development of circuits for a 1Megabit DRAM, he led the design of three generations of SRAM products and manufacturing test vehicles, and developed the original Phase Locked Loop (PLL) based clocking circuit in a microprocessor while working on the 50MHz Intel486™ processor design. He currently directs the development of high speed serial IO circuit technology in the 32nm logic process and researches chip-to-chip optical IO technology.

Born in Melbourne, Australia, he received his bachelor's and master's degrees in Electrical Engineering from the University of Melbourne, Australia, in 1972 and 1975. He received his Ph.D. in Electrical Engineering from UC Berkeley in 1978.

Young was a member of the Symposium on VLSI Circuits Technical Program Committee from 1991 to 1996, serving as the Program Committee Chairman in 1995/1996, and the Symposium Chairman in 1997/1998. He was a member of the ISSCC Technical Program Committee from 1992 to 2005, serving as the Digital Subcommittee Chair from 1997 to 2003, the Technical Program Committee Vice-Chair in 2004 and Chair in 2005. He was Guest Editor for the April 1997, April 1996 and December 1994 issues of the JSSC. He served on the SSCS AdCom from 2006 to 2008.

Young is a Fellow of the IEEE. He has authored or co-authored over 40 technical papers.

Anne O'Neill,
Executive Director,
SSCS

Process to Become a Petition Candidate for AdCom

Besides the 8 candidates put on the ballot by the Nominating Committee, additional candidates can be added to the ballot by petition. Interested society members can get on the AdCom election slate through a petition process managed by the IEEE Corporate Office. To begin this process, notify the SSCS Executive Office by email (a.oneill@ieee.org) no later than August 1st and include a statement verifying the nominee's agreement to be a candidate. Self-petitioning is acceptable. Once a petitioner's eligibility is verified, he/she is posted on the petition site until September 1, when the petition process closes. The Society offers no assistance or email lists to campaign groups for petition candidates; attracting members to the candidates petition is the responsibility of the candidate's supporters.

228 signatures of SSCS members in good standing are needed to qualify for the 2008 election slate. This number is defined by IEEE Bylaw I-308.16 as 2% of SSCS voting members as of 31 December, 2007. The signatures will be verified during the petition process (additional signatures above the minimum are recommended to provide a safety factor). Any voting member of the Society may sign such a petition in either of two ways: 1) via a link to the petition site provided on the Society's home page <www.sscs.org>, or 2) with an original signature on a hard copy petition.

There is no official IEEE hard copy petition form for society elections. Each handwritten petition form must include:

- the name of the candidate
- the title of the position the candidate is running for

For each person signing the petition:

- name (printed)
- IEEE member number
- signature

Hard copy petitions must be received by the SSCS Executive office by 1 September to be entered into the IEEE petition system.

If all the signatures on the petition are valid, active members with their dues paid up, the additional candidate's biography and photo will appear on the online and printed ballot.

Call for Nominations for Sensors Awards

Deadline for three awards is August 15

The IEEE Sensors Council sponsors two different awards for Technical Achievement, and Meritorious Service, and the IEEE Sensors Council Journal Best Paper Award. Please consider nominating a colleague for recognition by one of them.

The Technical Achievement Award honors a person for outstanding technical contributions within the scope of the IEEE Sensors Council as documented by publications, including patents. It is based on the general quality and originally of contributions. The award is a plaque and $2,000 check.

The Meritorious Service Award honors a person with outstanding long-term service to the welfare of the IEEE Sensors Council. It is based on dedication, effort and contributions. The award is a plaque and $2,000 check.

The IEEE Sensors Journal Best Paper Award recognizes the best paper published in the IEEE Sensors Journal. It is based on general quality, originality, contributions, subject matter and timeliness. The award is a certificate and $2,000 split equally among authors.

The 2007 awards will be presented during the 2008 IEEE Sensors Conference, October 26-29, 2008 in Lecce, Italy.

The Solid-State Circuits Society is a founding member of the Sensors Council. Councils are composed of Societies, not individuals, as members. The SSCS community has numerous technical experts aware of achievements in the Sensors field, many of whom achieve highpoints in this field, making them eligible for an award.

All nominations and supporting materials must be submitted by August 15, 2008, to the Award Committee Chair c.schober@computer.org

Information and forms are also available on the Sensor Council website under Society Awards: www.ewh.ieee.org/tc/sensors/SC%20awards.htm

Anne O'Neill,
Executive Director, SSCS

CEDA Currents

President's Message

The Council on Electronic Design Automation was formed in mid 2005 by its six member societies (the Antennas and Propagation Society, the Circuits and Systems Society, the Computer Society, the Electron Devices Society, the Microwave Theory and Techniques Society, and the Solid-State Circuits Society) to provide a focus on the field of electronic design automation. Since that time, CEDA has sponsored an impressive list of publications, conferences, workshops, and new activities, all focused on advancing the EDA profession. CEDA is sound financially, and successfully completed a review in November 2007 to become a permanent council of the IEEE. Much of the credit for getting CEDA so firmly established goes to Al Dunlop, CEDA's creator and former president, along with its officers and committee chairs.

As we go forward in 2008, our Executive Committee has some newly elected members:

- President: John Darringer
- President-Elect: Andreas Kuehlmann
- Past President: Al Dunlop
- Vice President of Activities: Soha Hassoun
- Vice President of Conferences: Bill Joyner
- Vice President of Finance: Donatella Sciuto
- Vice President of Publications: Rajesh Gupta
- Awards Committee Chair: William Joyner (acting)
- Nominations Committee Chair: Al Dunlop
- Secretary: David Atienza

The challenge in the coming year will be to continue to strengthen existing programs, find new ways to serve the changing profession, and reach more of the global EDA community. As the EDA field continues to evolve, CEDA will explore publications in emerging areas as well as alternative modes of communication, such as electronic editions, to improve communication within the EDA community while preserving the tradition of high quality. CEDA plans to strengthen its support for existing EDA conferences and begin streamlining the process for obtaining CEDA sponsorship, especially for smaller workshops in emerging areas.

Special events have been quite successful, including CEDA-sponsored sessions at the Design Automation Conference (DAC) and the International Conference on Computer-Aided Design (ICCAD) on ethics, and CEDA's Distinguished Lecture Series. We are planning more events like this in the future.

Over its short history, CEDA has explored different approaches for

improving the EDA profession. Some have worked, while others still need refinement. We have formed a committee to examine EDA awards, leading to collaborations with the Electronic Design Automation Consortium (EDAC) and ACM SIGDA to increase recognition for EDA contributions. Another committee is studying how EDA standards are created today and looking for ways to improve this process. More volunteers are needed for these and other CEDA activities, and new ideas are always welcome. If you'd like to get involved or have a proposal, please contact me (jad@us.ibm.com) or any member of the Executive Committee.

—John Darringer, CEDA president

New Dimensions in IC Design

3D ICs have emerged as an attractive option for overcoming barriers in interconnect scaling. The key benefits of 3D ICs over traditional 2D chips include reduction of global interconnects, higher packing density and smaller footprint, and support for mixed technology integration. To efficiently exploit the benefits of 3D technologies, design techniques and methodologies for supporting 3D designs are imperative. Design space exploration at the architectural level is also essential to fully take advantage of 3D integration technologies and build a high-performance microprocessor. A 3D tutorial organized by Yuan Xie of Penn State University and Gabe Loh of Georgia Tech was presented at the 35th International Symposium on Computer Architecture (ISCA 08) on 21-25 June in Beijing. For more information, please contact Yuan Xie (yuanxie@cse.psu.edu).

Best Paper Awards

Winners of best-paper awards at some of the outstanding events in 2007 and early 2008 include:

- Davare et al., "Period Optimization for Hard Real-Time Distributed Automotive Systems," 45th Design Automation Conference (DAC 2007).
- H. Inoue et al., "Dynamic Security Domain Scaling on Symmetric Multiprocessors for Future High-End Embedded Systems," International Conference on Hardware/Software Codesign and System Synthesis (CODES-ISSS 07).
- A. Singhee and R.A. Rutenbar, "Statistical Blockade: A Novel Method for Very Fast Monte Carlo Simulation of Rare Circuit Events and Its Application," Design, Automation and Test in Europe Conference (DATE 07).
- S. Watanabe et al., "Protocol Transducer Synthesis Using Divide and Conquer Approach," 12th Asian and South Pacific Design Automation Conference (ASP-DAC 07).
- Y. Zhou et al., "A New Methodology for Interconnect Parasitics Extraction Considering Photo-Lithography Effects," 17th ACM Great Lakes Symposium on VLSI (GLSVLSI 07).
- F. Wang, X. Wu, and Y. Xie, "Variability-Driven Module Selection with Joint Design Time Optimization and Post-Silicon Tuning," 13th Asian and South Pacific Design Automation Conference (ASP-DAC 08).

Upcoming CEDA Events

CEDA currently sponsors or cosponsors 10 conferences and workshops, and two additional conferences in which it is in technical cooperation with other societies. Our conferences provide excellent opportunities for those interested in learning about the latest technical trends in electronic design and automation, and in being engaged with a community of volunteers. If you are interested in participating or have an idea about new topics of interest for our conferences, please contact Bill Joyner (william.joyner@src.org), CEDA vice president of conferences.

CEDA Currents is a publication of the IEEE Council on Electronic Design Automation. Please send contributions to Jose Ayala (jayala@fdi.ucm.es) or Anand Raghunathan (anand@nec-labs.com).

Editor's Column *Continued from page 2*

Two additional papers in our next issue will comment further on the impact of Dr. Vittoz's work:

(6) "Advances in Ultra-Low-Voltage Design," by Joyce Kwong and Anantha Chandrakasan (MIT);

(7) "Gigasensors for an Attoscope," by Erik H. M. Heijne (CERN).

They are represented by Executive Summaries on pages 59-60 of this issue. Finally, the first page of one more original paper by Dr. Vittoz, which will be reprinted in full in the Fall, appears on page 66:

E. Vittoz, "Microwatt Switched Capacitor Circuit Design," Summer Course on Switched Capacitor Circuits, June 9-12, 1981, ESAT, Katholieke Universiteit Leuven, Heverlee, Belgium.

The Swatch Store at Grand Central Terminal, New York, NY, May 18, 2008.

SSCS EVENTS CALENDAR

Also posted on www.sscs.org/meetings

SSCS SPONSORED MEETINGS

2008 Organic Microelectronics Workshop
www.mrs.org/s_mrs/sec.asp?CID=13576&DID=207893
July 7-10, 2008
San Francisco, CA 94103

2008 Custom Integrated Circuits Conference
www.ieee-cicc.org/
21–24 September 2008
San Jose, CA, USA
Contact: Ms. Melissa Widerkehr,
Conference Manager *cicc@his.com*

2008 Asian Solid-State Circuits Conference
www.a-sscc.org/
3-5 November, 2008
Fukuoka, Japan
Contact: Secretariat of A-SSCC 2008
E-mail: *A-SSCC2008@ics-inc.co.jp*

2009 ISSCC International Solid-State Circuits Conference
www.isscc.org
8–12 February 2009
San Francisco, CA, USA
Paper deadline: 22 Sept. 2008
Contact: Courtesy Associates, *ISSCC@courtesyassoc.com*

2009 Symposium on VLSI Circuits
www.vlsisymposium.org
16-18 June, 2009
Contact: Phyllis Mahoney, *phyllism@widekehr.com*

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Hot Chips
www.hotchips.org
24-26 Aug 2008
Palo Alto, CA, USA
Paper deadline: Passed
Contact: John Sell, *info2007@hotchips.org*

ISLPED International Symposium on Low Power Electronics and Design
www.islped.org/ http://www.islped.org/
11-13 Aug 2008
Bangalore, India
Contact: Diana Marculescu, *dianam@ece.cmu.edu*

ESSCIRC/ESSDERC 2008 - 38th European Solid State Circuits/Device Research Conferences
www.esscirc2007.org
15 - 19 Sep 2008
Edinburgh, Scotland
Paper deadline: Passed.
Contact: Bill Redman-White, ESSCIRC Chair
bill.redman-white@nxp.com

2008 IEEE Integrated Circuit Ultra-Wide Band ICUWB
www.icuwb2007.org
10-12 Sep 2008
Hannover, Germany
Paper deadline: Passed.
Contact: Michael Y.W. Chia, *chiamichael@i2r.a-star.edu.sg*

2008 IEEE Bipolar/BiCMOS Circuits and Technology Meeting - BCTM
www.ieee-bctm.orgA
14-16 Oct 2008
Monterey, CA
Paper deadline: Passed
Contact: Ms. Janice Jopke *ccs@mn.rr.com*

2008 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)
www.csics.org
12 - 15 Oct 2008
Monterey CA
Paper due date: Passed
Contact: William Peatman *wpeatman@anadigics.com*

Sensors Conference
www.ieee-sensors2008.org
26-29 October 2008
Lecce, Puglia, Italy
Paper due date : Passed
Contact *Info@ieee-sensors2008.org*

2008 International Conference on Computer Aided Design (ICCAD)
www.iccad.com/
9-13 November 2008
San Jose, CA
Contact: Kathy MacLennan, Conference Manager
kathy@mpassociates.com

Conference on VLSI Design
http://vlsiconference.com/vlsi2009/
5-9 January 2009
New Delhi, India
Paper Deadline: July 17, 2008

IEEE International Conference on Microelectronic Test Structures
www.see.ed.ac.uk/ICMTS/
30 Mar – 2 Apr 2009
Oxnard, CA
Paper Deadline: 15 Sept 2008
Technical Chairman: Richard Allen
richard.allen@nist.gov

Design Automation and Test in Europe (DATE) 2009
www.biztradeshows.com/trade-events/date.html
20-24 April 2009
Nice, Alpes-Maritime, France

VLSI -TSA/DAT
vlsitsa.itri.org.tw/2009/General/
27-30 April 2009
Hsinchu, Taiwan
VLSI-TSA Contact : Clara Wu
vlsitsa@itri.org.tw
VLSI-DAT Contact: Ms. Elodie HO
vlsidat@itri.org.tw

SSCS IEEE SOLID-STATE CIRCUITS SOCIETY NEWS is published quarterly by the Solid-State Circuits Society of The Institute of Electrical and Electronics Engineers, Inc. Headquarters: 3 Park Avenue, 17th Floor, New York, NY 10016-5997. $1 per member per year (included in society fee) for each member of the Solid-State Circuits Society. This newsletter is printed in the U.S.A and mailed Periodicals Postage Paid at New York, NY and at additional mailing offices.
Postmaster: Send address changes to SSCS IEEE Solid-State Circuits Society News, IEEE, 445 Hoes Lane, Piscataway, NJ 08854.

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