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# SOLID-STATE CIRCUITS

IEEE Solid-State Circuits Society Quarterly Newsletter

IEEE

## ISSCC Focuses on Embedded Systems

ISSCC is the foremost global forum for presentation and discussion of new developments in the integrated circuit industry. The theme for 2004 is "Embedded systems for a connected world." The intelligence in integrated circuits is attributable to their embedded microprocessors, and now they are used for every aspect of computing and control, including their own efficiency and performance. Memories (SRAM, DRAM, and Nonvolatile) are integrated in order to achieve higher performance, and/or lower power. Other imbedded functions include analog circuits, such as A/D and D/A converters, DSPs, RF CMOS and CMOS image sensors, and wireline communication interfaces. ISSCC 2004 will introduce major progress in embedded systems for wireless, wireline, and mobile applications.

Over 200 papers will be presented in twenty-seven sessions during the three days of the conference. What follows are a few highlights of eight major topics the conference covers.

To register for the 15–19 February conference in San Francisco California, or for a more detailed view of all the presentations in the Advance Program, go to *www.isscc.org/isscc*. Articles from the ISSCC 2004 Digest will be available in IEEE *Xplore*™ by summer.

### Analog

2004 may be the year of the converter at ISSCC; this year will feature four sessions dedicated to new A/D and D/A converters! These papers will establish many new benchmarks for converter state-of-the-art in speed, resolution, power, and area efficiency.

Converters form the critical interface between "real world" analog signals and the digital signals processed by computers. As signal-processing systems become more sophisticated, the converters can become the bottleneck that ultimately limits system performance. Conversely, in some cases, converter advances can actually enable fundamentally new architectures.

In Monday afternoon's Session 4 Philips Research (4.1) and ETH Zurich (4.2) will present converters that push sigma-delta-converter bandwidths to 10 MHz and beyond to handle next-generation broadband communication requirements. In Tuesday afternoon's Session 14 National Semiconductor (14.1), will describe high-speed A/D converters that bring 1 GS/s performance into the mainstream. In Wednesday morning's Session 20, Analog Devices will describe an IC that extends 14-bit D/A converters to sample rates beyond 1 GS/s to simplify multicarrier radio processing (20.1). This is another important step towards "software radio." Multiple sessions will feature converter papers that wrestle with the challenges of

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**SSCS Elects Five AdCom Members page 10**

# ISSCC Focuses on Embedded Systems

*Continued from page 1*

## ISSCC Plenary Speakers Monday Morning

**Nicholas M. Donofrio**, Senior Vice President, Technology and Manufacturing, IBM, Armonk, NY, USA
"Processors and memory: The drivers of embedded systems toward the networked world."

**Nicky C. Lu**, President and CEO, Etron Technology, Hsinchu, Taiwan
"Emerging technology and business solutions for system chips."

**Yrjö Neuvo Professor**, Executive Vice President, CTO, Member of Nokia Group Executive Board, Nokia Mobile Phones, Finland
"Cellular phones as embedded systems."

integrating converters onto digital circuits implemented in deep-submicron CMOS technology (4.5, 14.5, 14.3).

In Wednesday afternoon's Session 25 all the papers will highlight new algorithms to allow digital calibration of analog non-idealities in ADCs. Although calibration techniques have been used for more than twenty years, this session will feature the recent flurry of new development that helps lower power dissipation and enables operation at significantly reduced supply voltages.

Both foreground and background calibration techniques will be explored in various papers. In foreground calibration, the normal operation of the A/D converter is stopped while the converter goes through a "calibration cycle." In background calibration, techniques are used to detect and correct converter errors during the normal operation of the converter. In some cases, techniques common to some of today's spread-spectrum communications systems are applied to separate converter errors from the signal being processed by the converters. The result is a number of new high-performance A/D converters that can be efficiently realized in deep-submicron processes.

## Digital

The past year has seen a number of microprocessor companies leverage their large investment in existing designs by shifting fabrication to faster, smaller-featured manufacturing processes. These provide millions of extra transistors, leaving microprocessor designers with the question of how to use these extra devices while avoiding significant redesign costs and escalating power concerns. Intel (3.4) will present design techniques to improve design productivity and reduce the cost of redesign.

IBM (3.1) and Sun (3.2) integrate multiple independent processor cores on one chip. Many important server applications, including Web hosting and databases, are already designed to divide their workloads into independent tasks, enabling these chip-scale multiprocessors to provide greater throughput by running multiple tasks simultaneously.

Designers must also address the static leakage of these extra transistors. IBM (3.7) and Sony (3.5) will present aggressive circuits that dynamically adjust voltage levels and frequency to lower power, while Sun (3.2) will introduce a novel circuit to offset a new reliability issue caused by advanced transistor technologies.

Session 8 on Tuesday morning will feature computing at ultra-low voltages. Lower power supply voltage typically requires lower voltage to turn on a transistor, called threshold voltage (Vt). Lowering voltage

| ISSCC 2004 Schedule of Topics by Session Number | Monday afternoon | Tuesday morning | Tuesday afternoon | Wednesday morning | Wednesday afternoon |
|---|---|---|---|---|---|
| Analog | 4 | | 14 | 20 | 25 |
| Digital | 3 | 8 | | 19 | |
| Imagers, Displays, and MEMS | 6 | | 12 | 17 | |
| Memory | 2 | 11 | | | 27 |
| Signal Processing | | | | 18 | 23 |
| Technology Directions | | 7 | 16 | | 24 |
| Wireless Communications | 5 | 10 | 15 | 21 | |
| Wireline Communications | | 9 | 13 | | 22 & 26 |

saves power consumption, but ultra-low voltage leaves processors vulnerable to increased noise sensitivity and lower computation speeds. Intel (8.4) will present a new technique that automatically reduces the (Vt) with supply voltage to provide better performance at very low power. STARAC (8.6) will show that the increase in noise problems for circuits at lower voltages can actually be actively suppressed by innovative circuits.

Wednesday morning's Session 19 will focuse on multi-GHz clocking. Clocking generation and distribution with minimal differences in clock arrival times (skew) across the chip is difficult yet essential for state-of-the-art integrated circuits. However, clocking generation also consumes a large portion of the total power. Columbia University and IBM (19.1) have used on-chip spiral inductors that resonate with the clock capacitance and achieve a 35% reduction in clock power dissipation.

NEC (19.5) and IBM (19.7) provide on-chip skew-measurement circuitry to show a more realistic view of the clock-skew variation under normal operating conditions, minimizing future over-design.

## Imagers, Displays, and MEMS

During Monday afternoon's Session 6, Canon (6.1), Matsushita (6.2), and Sony (6.3) will introduce three developments in high-density CMOS imagers that increase pixel density on a sensor, decreasing sensor cost, and reducing the size and cost of the lens needed in the end application. Each design uses intelligent sharing of components and operation functions. All three use buried pinned photodiode structures to increase efficiency. One of the designs will report pixel pitch only nine times the minimum device dimension. Overall, these three papers will highlight significant trends in imaging for expanding low-cost consumer-product applications.

Tuesday afternoon's Session 12 will introduce a neural prosthesis device for the restoration of sight to the blind (12.1). The group from UC Santa Cruz and USC has performed three human clinical trials with outstanding results. The blind patients were able to read large letters, count objects, and recognize and differentiate objects such as a cup and a plate. Next, researchers from Infineon (12.2) will describe DNA microchips with electronic readouts that offer potential competitive alternatives to optical detection of biochemical reactions.

On Wednesday morning researchers from Rockwell Scientific (17.1) will describe and display a microprocessor using micro-sized mechanical switches. Bulky discrete-circuit techniques are still required in ultra-high-frequency circuits; with MEMS devices operating within the integrated-circuit-scale environment, the situation has changed dramatically.

Later in the morning, researchers from St. Jude's Medical Center (17.5) will report the highest level of integration in an interface IC for implantable cardiac pacemakers, enabling smaller size and increased lifetime.

## Memory

Flash technology is now mature and is challenging the density leadership of DRAM technology. Samsung (2.7) uses chalocogenide technology characterized by the use of resistive heating of the material to change the resistive state of a cell. Hynix and

| Evening Discussion Sessions<br>Do not miss these sessions — they are not documented in the Conference Digest. | |
|---|---|
| Special Topic Session | Experts provide background and insight on a topic of current importance. |
| Panel Discussion | Experts debate an important topic and field audience questions in a semiformal atmosphere. |
| Sunday | |
| Topic Session | Architectures and Circuits for Ultra-Wideband Radio |
| Topic Session | CMOS Meets BIO |
| Topic Session | Highlights of DAC |
| Monday | |
| Panel Discussion | To UWB or Not To Be |
| Panel Discussion | Is the Golden Age of Analog Circuit Design Over? |
| Topic Session | Circuits and Applications for Organic Electronics |
| Tuesday | |
| Panel Discussion | Noise and Coupling in Mixed-Signal RF SOCs |
| Panel Discussion | Processors and Performance: When Do GHz Hurt? |
| Topic Session | What Is the Next Embedded Nonvolatile Memory Technology? |

Seoul National University (2.2) combine the features of Flash and DRAM, to produce DRAM characteristics during normal operations and nonvolatile behavior at power-down. Motorola (2.3) uses an innovative cell architecture to achieve the highest MRAM capacity reported of 1 Mb and the fastest reported cycle time for MRAM of 130 ns. It uses a novel toggle magnetic tunnel junction technology that will easily integrate into a standard CMOS process. Virage Logic (2.4) will report a new reference voltage scheme for ferroelectric memories to provide improved reliable operation at voltages as low as 0.9 V.

Tuesday morning's Session 11 on DRAM will introduce a low-power memory for extended battery life of handheld electronics. United Memories and Sony (11.1) employ an onboard macro to implement innovative transistor-biasing techniques, scaling the operating voltage to almost half of previously reported levels. Samsung (11.6) will describe a DDR-SDRAM graphics application that will translate into a more realistic video-gaming experience. The part utilizes a wave-pipelined control system to support a wide frequency operating range, from 300 to 800 MHz.

Wednesday afternoon's Session 27 will feature an SRAM that achieves a breakthrough in low-power mobile operation. Hitachi, SuperH, and Renesas Technology (27.2) will report on an on-chip SRMA with a standby mode consuming only 30 microwatts, and an active power of 0.4 miliwatts at 300 MHz. Intel (27.3) will report a record-breaking cache on a microprocessor chip for server and CPU applications. It has a 54-Gb/s read-write bandwidth. At 533 million transistors, the SRAM cache uses 90% of the total number of transistors on a 432-mm$^2$ chip.

## Signal Processing

With only two sessions during ISSCC, the significant results in signal processing are a few fabulous consumer applications.

Real-time encoding of motion pictures has been limited to broadcast TV quality because of a lack of computation power. The potential high-definition (HD) compression standard (JPEG 2000) for recording, playback, and transmission of full-motion movies would require tens of billions of operations. During Wednesday morning's Session 18, Sanyo (18.1) will describe the world's first single-chip codec for real-time compression of full-motion movies and HDTV signals. It will enable Web-based movie distribution and real-time recording, such as HD digital cameras and surveillance applications.

With no fully integrated support for multimedia, Bluetooth, GPS, and modem on a current cellular baseband chip, the industry would enhance consumer multimedia experience with such a solution. Qualcomm (23.3) will present the first cellular baseband chip with fully integrated support for multimedia, Bluetooth, GPS, and modem on Wednesday afternoon. It is the highest level of integration published for cellular baseband chips.

## Technology Directions

In Session 7 on Tuesday morning, Mark Horowitz of Stanford University will focus on how interconnect-centric tiled architectures can overcome wire delay limitations. Local communications schemes will replace global schemes to enable future technology scaling. Heterogeneous machines will have different modules tuned for specific applications.

The University of Twente (7.2) will introduce ways to circumvent the dramatic scaling of voltage and power consumption for analog circuits by exploiting available thin- and thick-oxide transistors. Special circuit techniques allow higher supply voltages to be used for analog than for digital circuits.

In Session 16 on Tuesday afternoon, Seiko-Epson (16.1) will present a cost-effective fabrication method for organic transistors using the inkjet printing technique. This paper illustrates the successful development and operation of an active-matrix backplane in applications such as smart clothing, plastic displays, and biomedical. The University of Tokyo (16.2) will present

### Tutorials, Forums and Short Courses

**Sunday Tutorials**

Attendees may register for a maximum of three tutorials. Taught by experts from the Program Committee, these 90-minute sessions are aimed at meeting attendees' needs for introductory material in the respective topics. Register early on the website for these sessions, as they fill up fast.

- Tuning of Analog Parameters
- Wireless-LAN Radio Design
- Electronic Circuits in an Automotive Environment
- Introduction to PLL and DLL Design for Digital Systems
- Noise in Solid-State Imagers: Basics and Specsmanship
- Design for Testability of Embedded Memories
- The Reality and Promise of Reconfiguring Computing in Digital Signal

**Sunday Forums**

Forums are targeted at designers experienced in the technical field.

- Gigahertz Radio Front Ends: RF Power Amplifiers
- Memory Design: Non-Volatile Memories – Technology and Design

**Thursday Advanced Circuits Forums**

- Analog Telecom ASIC and Circuit Concepts: A/D and D/A Building Blocks for Telecom Transceiver Applications
- Microprocessor Design: Managing Variability in Sub-100-nm Designs

**Thursday Short Course**

- Deep Sub-Micron Analog and RF Circuit Design

the use of plastic transistors for artificial skin. This flexible sensor can be used as artificial skin for robots. A simple cut-and-paste approach is proposed to customize the size of these circuits.

For more on the challenges and opportunities of organic transistors see Sodini and Bulovic's report on the Application-Driven Organic Electronics Workshop, page 8.

Session 24 on Wednesday afternoon will feature three extremely low-power, low-rate communication devices. The circuits must be optimized for low duty-cycle operation, and energy consumption is the primary design metric. A gas-chromatographer fabricated in less than a few cc by the University of Michigan (24.1) integrates digital compensation, self-test, and distributed power management on a wireless sensing platform. AnSem NV and Phonak Communications (24.2) will describe a very-low-power programmable FM receiver for hearing aids in less than 1 cc.

A flyspeck RFID by Infineon (24.3) is aimed at replacing barcodes. The small size and low cost (projected under one cent in large volume) of the chip is a direct consequence of a collection of cunning circuit innovations. It is powered directly from an interrogating RF supply without AC-to-DC conversion. Such AC operation of logic circuits eliminates the need for both rectification and filtering, providing considerable space savings. The RFID requires an on-product printed antenna loop.

Wednesday afternoon's Session 24 will continue with a number of 60-GHz circuit devices, spurred in part by opening 7 GHz of a previously unlicensed bandwidth around 60GHz, and featuring aggressively scaled CMOS and Si Ge technologies

## Wireless Communications

Monday afternoon's Session 5 will feature five papers from Spirea (5.2), New Logic (5.3), Atheros (5.5), IRF Semiconductor, and Stanford University (5.4) that describe transceivers for 802.11a/b/g. Each strives to reduce cost by using low-cost CMOS technology and architectures that minimize external components. Each implements transceivers for all three standards that will enable seamless universal connectivity. Atheros (5.50), Seoul National University, and GCT Semiconductor (5.6) will describe efficient generation of the LO signals, essential for WLAN. Developers from Universita di Pavia (5.7) will describe a receiver front end in SiGe that addresses performance issues. Researchers at the University of Tokyo (5.8) will describe a 4.3-GHz frequency divider that consumes just 44 microwatts, important for a mobile application.

During Tuesday morning's Session 10, eight papers will feature radio on chips with varied integration levels, from an entire multimode GSM transmitter implemented in a 0.13-µm CMOS technology to an individual GSM power amplifier realized in a Si-LDMOS. A novel radio architecture presentation will explore the appropriate distribution of both the analog and digital blocks to realize the most efficient implementation from a performance and die-area perspective. Examples of digital and analog functions swapping traditional roles will be highlighted.

During Tuesday afternoon's Session 15, two teams from TI (15.1 and 15.3) will describe cell phones and other small handheld devices that can exchange information over a short range, while using very little power and having ultra-long battery life. Sharp (15.6) will show that they also will be able to receive television signals, including new interactive services that combine the best of broadcast television with the interconnectedness of the internet, while maintaining very long battery lifetimes.

Wednesday morning's Session 21 will focuse on silicon reaching for millimeter-wave frequencies. Today, we use a small fraction of the available radio spectrum. This is due to the limitations of existing radio architectures and semiconductor technologies. Ultra-wideband (UWB) systems (a new radio architecture) harness additional unused radio frequency bandwidth and increase data rates, but impose unusual demands on circuit design. The-California Institute of Technology (21.1) and Harvard University (21.2) will present creative ways to improve oscillator performance. University of Padova (21.3), Skyworks, and UCLA (21.4) will describe low-noise amplifiers for operation in the UWB band spanning 3.1 to 10 GHz. Silicon's suitability for operation beyond 10 GHz will be well-demonstrated by several papers describing circuits with excellent performance at frequencies approaching 40 GHz.

## Wireline Communications

Tuesday morning's Session 9 will feature significant cost reductions in 10-Gb/s and SONET systems in highly integrated CMOS transceivers. These reports by Hitachi (9.1) and Aeluros (9.2) will mean faster, cheaper network connections to desktops and servers.

System integration and complexity create an ever-increasing need for I/O bandwidth. During Tuesday afternoon's Session 13, a combination of faster process and new latch design from NEC (13.1) will achieve multiplexers at 120 Gb/s and demultiplexers at 110 Gb/s. Current standards had been limited to 40 Gb/s. IBM (13.3) will describe multiplexing with good jitter and lower power achieved at 108 Gb/s using half-rate clocking. These high-speed Mux and deMux chips enable the next generation of test equipment. The number of cables, connectors, and fibers can be minimized by sending data at the fastest possible serial data rates.

Helpful to telecom companies in competition with cable and satellite TV providers are practical lower-cost, lower-power, and higher-data

rate ADSL2+ and VDSL. Described by Infineon (22.1) and TI (22.2) during Wednesday afternoon's Session 22, these solutions will allow even high-quality video over twisted pair.

Wednesday afternoon's Session 26 will feature many innovations for optical, and electrical-communication systems operating up to 40 Gb/s in silicon processes. They use on-chip electrical equalizers to extend the bandwidth of the integrated CMOS photodetector. The University of Twente (26.2), Netherlands, will describe a novel 3 Gb/s photodector that is about five times faster than previous designs. The University of California Irvine and Stanford University (26.7) will describe a novel detection of transition edge rate to provide adaptive equalization for copper cables between 1 and 5 meters at 10 Gb/s.


**Try browsing some of the best examples of ISSCC papers in the past. *sscs.org/pubs/ISSCC-Awards.htm***

The links launch IEEE *Xplore*. Member authentication will be requested. If you come in through an institutional subscriber, the connection may be direct. All members can read abstracts. A member subscription to the SSC Conference Digital Library costs $75 and includes the ISSCC, CICC, Symposium on VLIS Circuits, and, beginning 2003, ESSCIRC. Purchase of individual articles through IEEE Xplore also is enabled.

# Call for Nominees for SSCS Administrative Committee Election

In accordance with its Constitution, the IEEE Solid-State Circuits Society invites members of our Society to nominate candidates for the Society's Administrative Committee (AdCom). The election is held in the September–October time frame.

## Nominees by Petition

Nominees will be automatically placed on the ballot provided:

- The nominee is presently a member of the IEEE Solid-State Circuits Society.
- The petition is supported by at least ten identifiable signatures of present members of the Society other than the nominee.
- The nominee is both aware of and agrees to the petition.
- The petition is received by the Chair of the Nominations Committee by 1 May 2004.

## Term of Office

- The term of office is three years beginning 1 January 2005.
- AdCom members may be reelected to a second consecutive term.
- The five nominees receiving the highest number of votes from the Society membership will be elected.

## Scope and Responsibilities

Elected AdCom members are expected to attend the two yearly meetings of the AdCom. In addition, much of the Committee work is carried on by email, telephone, and fax throughout the year. The Solid-State Circuits Society currently sponsors the *Journal of Solid-State Circuits*, the International Solid-State Circuits Conference, the Custom Integrated Circuits Conference, and the Symposium on VLSI Circuits. In addition, the Society cosponsors or technically cosponsors a number of other conferences and meetings.

The AdCom has responsibility for overseeing these and other potential future technical activities within the Society's field of interest, as well as the overall operation of the Society.

## Mailing Petitions

All petitions should be accompanied by a personal photograph and a short biography (200 words), including the nominee's technical areas of interest. Petitions must be received by 1 May 2004. Petitions are to be mailed to:

Chair of the Nominations Committee
IEEE SSCS Executive Office
445 Hoes Lane
Piscataway, NJ 08854

# Call to Nominate Candidates for the IEEE Solid-State Circuits Award

### On Whose Shoulders Do You Stand?

How can so many engineers design million-transistor circuits with confidence and get reliable products to market on time? What technical advances and what algorithms are almost intuitive in our design and software processes? How do we know where to start, where it is still too risky invest time, or what is too risky to tweak? If you can remember a decade or more ago when you dreamed about the work your team accomplishes today, you can remember the seminal ideas that have allowed circuits to evolve a hundredfold. You could be a nominator for the IEEE Solid-State Circuits Technical Field Award, the Institute's highest honor for outstanding contributions in our field.

Since its establishment in the 1980s this award has reflected the progress of the technology. The history of the field is the textbook for tomorrow's engineers. How is it that engineers can design faster, smaller, and denser circuitry every year? Look back, look around. Most of the ideas and authors were probably published in the *Journal of Solid-State Circuits*.

The Solid-State Circuits Technical Field Award, presented at ISSCC, consists of a bronze medal, a certificate, and a cash prize. It honors an individual, or team of up to three, for outstanding contributions in the field of solid-state circuits, as exemplified by enhancement to technology, benefit to society, and professional leadership. The nomination form is available to download online: *www.ieee.org/about/awards/noms/solidnom.htm*.

Guidelines, also available online, emphasize the importance of the nominee's accomplishments, the quality of the nomination itself, and the quality of the supporting endorsement letters. The true merits of a candidate need to be conveyed through the nomination and endorsement paperwork. The deadline for receipt of nomination materials (including the nomination form and the supporting letters) is 31 January 2004.

For further information, to coordinate your efforts with others, or to determine if a nomination is already in progress, please contact Richard C. Jaeger, the Chair of the SSCS Awards Committee, at: jaeger@eng.auburn.edu.

# IEEE Lunch at ISSCC Offers Clues to More Successful Patents

In a dramatic shift from just twenty years ago, when patents issued in information technology cited only previous patents, today's patents are increasingly based on fundamental sources such as scientific and technical literature. A recent study by a nationally recognized research firm, CHI Research, analyzed the relationship of valuable corporate patent portfolios and IEEE literature They found that technology built on IEEE science is more likely to be more valuable than peer technology not built on IEEE science. The study also found that IEEE publications are cited in high-tech patents more than any other scientific-technical publisher. In addition, the publications of the IEEE Society sponsoring this newsletter are cited in patents more than any other IEEE publication.

To find out more about this study, institutional users of online information are invited to a luncheon hosted by IEEE at the IEEE International Solid-State Circuits Conference (ISSCC), 17 February 2004 in San Francisco. ISSCC attendees and staff from corporations in the Bay Area are welcome to attend.

The presentation at the luncheon will focus on the value of IEEE information in the development of circuits and related technologies and in the development of new patents. This luncheon also will include guidance in the use of IEEE technical content, tips on gathering competitive intelligence, and information on how IEEE online resources can drive corporate patents in the solid-state circuits industry.

Anyone interested in attending should RSVP by 19 January to Beverly Banks at b.bank@ieee.org. Space is limited.

Event: IEEE Lunch and Presentation (in conjunction with ISSCC 2004)
Date: 17 February 2004
Time: Noon–1:30
Place: Club Room, San Francisco Marriott

For more about IEEE information and patents, please visit *www.ieee.org/patentcitation*.

# Application-Driven Organic Electronics Workshop

The IEEE Solid-State Circuit Society's Long-Range Planning Committee has launched an effort to explore profound changes in circuit and system design in the post-Moore era and their potential implications on applications, interdisciplinary collaboration, and the role of the society as a service organization. As a member of that committee, Professor Hugo DeMan has stated that the biggest challenge to this ambitious goal is "to bring visionary people together who are willing to start a dialogue on what future microsystems will look like and how we will join forces to make progress in this new field of 'super circuit' design." The Solid-State Circuit Society has the right combination of long-term vision coupled with the practical realities of commercial design to play a major role in stimulating creative thinking. A major challenge in this effort is to determine the mechanisms that are best suited to stimulate a dialogue among disciplines that we envision will become well-connected.

To stimulate development of working research relationships we replaced the traditional workshop format of a packed one- or two-day schedule of several talks with a workgroup approach. We assembled a small gathering in a setting conducive to creativity, with ample time to brainstorm and discuss the possibilities among a few visionary individuals from relevant disciplines. The first such workshop, "Application-Driven Organic Electronics," was held in late June at the MIT Endicott House.

Active organic electronic components such as organic transistors, solar cells, photodetectors, and LEDs likely will be the enabling blocks of future low-cost flexible electronics and integrated large-area optoelectronic circuits. The organic materials break the paradigms of silicon technologies in that their unconventional processing methods enable integration with flexible conformal substrates from centimeters to meters in size. However, this technology is compromised by the lower charge carrier mobility of organic solids and the unproven reliability of devices made with organic materials. Nevertheless, the utility of organic materials in display applications has already been demonstrated. Their use in low-performance integrated electronic circuits, driven by the potential for low-cost organic electronic systems, is being explored.

***The Application-Driven Organic Electronics Workshop was held in late June at the MIT Endicott House. Hear more about the results of this workshop in a special evening session, Sunday, 15 February at ISSCC 2004.***

In the late 1960s, silicon MOS technologies were at a stage similar to organic electronics today. DRAM served as the driver for MOS devices from approximately 1970 to 1985, encompassing DRAM generations from 1 kb to 1 Mb. The DRAM application was not exclusive but helped to focus research in silicon process technology as well as device and circuit design.

Current research in organic electronics is focused primarily on the improvement of discrete devices. This focus is expected, considering that the physical processes within organic devices are still being discovered. In the near future it is expected that the integration of organic light-emitting diodes (OLEDs), organic photodetectors (OPDs), and organic field-effect transistors (OFETs) will be integrated into circuits that control electrical and optical signals. The challenge for the workshop was: What application platform will best drive this integration?

It would be folly for organic electronics to try to replace silicon digital processing and memory applications since its strengths are not suitable for these functions. Instead, workshop participants suggested that successful commercial applications will take advantage of the inherent attributes of organic material: low cost, mechanical flexibility, chemical sensitivity, optical properties, and the potential for integrated large-area optoelectronic circuits. Identifying the commercially viable organic electronics application drivers and outlining the research necessary to demonstrate these practical applications was the challenge posed to the workshop participants.

To start, we asked ourselves what proven organic technologies have reached the marketplace. Applications that take advantage of the optical properties of organic devices already have been extremely successful in optical recording, liquid crystal displays, and photoconductors—generating approximately a $100 billion business. Up to this point we have not seen many commercially viable electronic or optoelectronic systems based on organic technology because moving charges is not an inherent advantage of organic devices. It is clear that the application drivers for organic electronics should leverage the excellent optical properties and require minimum performance from associated electronics.

Although many researchers are publishing results for discrete OLEDs, OFETs, and OPDs, little work has been done on developing a process flow for the integration of these devices. It is clear that one of the major challenges to move organic electronics from the research lab to commercial viability is the convergence on a single process flow. The fact that different active materials and different dielectrics are being employed to fabricate devices has made the convergence on a single process flow extremely difficult. In addition, there are no standard characterization techniques to fairly compare performance metrics between different device structures. So what are the applications that will drive us to develop a standard integrated all-

organic process?

Three possible application drivers were discussed during the workshop. The first is a digital X-ray detector using OPDs. This detector could be used in medical applications, diagnostics, failure analysis, security, and a variety of scientific equipment. It was suggested that a large array of applications are possible since the detector may be fabricated on a nonplanar substrate. This application is attractive since it takes advantage of several attributes of organic technology. However, it is not without challenges. Near the top of the list is the requirement for a large on-to-off current ratio for the OFET and small dark current in the OPD to insure high sensitivity for the detector.

The second application discussed was large-area displays. To relax the initial requirements on the OFETs, it was suggested to start with displays showing fixed format graphics and then moving to full motion video. To reduce the effect of OLED degradation over time one could use OPDs to sense the light intensity at each pixel and use off-display silicon circuits to feed the corrected information back to the OFET drivers. This application would take advantage of all three devices in an integrated process flow.

The last application centered on distributed sensors that would make use of the chemical sensitivity of organic technology. These sensors could be applied to environmental monitoring, threat detection, and a variety of medical applications. The addition of RF communication on these sensors will certainly challenge the device characteristics of OFETs.

One of the main results of this workshop was a clear understanding among the participants of the progress that has been made and the challenges in applying this new technology. We are hoping to see the formation of new networks of researchers who can continue the dialogue as this technology emerges. We are aiming to develop strong interactions between organic technologists and circuit designers to enable large-scale integration of organic components for targeted applications. At the 2004 ISSCC Professor Vladimir Bulovic will present more of the results of this workshop in a special evening session on organic electronics. In addition to Bulovic's talk attendees will also hear from researchers at Sarnoff Labs, Infineon Corporation, and Sony Corporation. Please join us for this special session and join in the dialogue in driving organic electronics to a commercially viable technology.

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# Another IEEE Membership Bennefit, Online Access to *Transactions on Device and Materials Reliability*

Started in 2001, this IEEE transaction (*T-DMR*) focuses on component reliability and documents the search for the root cause of failure in increasingly more complex devices and in the materials used to make these devices. The physics of failure, a watchword in the semiconductor industry, reveals new phenomenon that show up as weakness in design, process, material, or application. The determination and elimination of the root cause of failure invariably involves a multidisciplined effort. Electrical engineering, physics, materials, chemistry, processing, and packaging mix to generate a cost-effective solution.

This archival quarterly provides a new forum for information that has long been scattered as niche articles in publications and conference digests only partly aligned with one particular field or crossing the boundaries between disciplines. The scope covers the reliability of electronic, optical, magnetic, and MEMS devices, together with associated microsystems and packages. Because rapid dissemination of information is critical to the creation of high-reliability products, this transaction is available exclusively online and is free to all members to browse or read complete articles. *T-DMR* is sponsored by the IEEE Electron Devices Society and the IEEE Reliability Society (*www.ieee.org/xploretdmr*).

The December 2003 special issue focused on interface reliability. The March 2004 special issue will include selected and expanded papers from the 10th IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA 2003). The September 2004 special issue will focus on Nonvolatile Memory Reliability. For more information concerning *T-DMR* and its EIC and editors, see *www.ieee.org/tdmr/*.

# Congratulations to New SSCS Senior Members

Jack B. Andersen
Douglas C. Burger
Ross M. Carlton
Toby J. Cumberbatch
Izzat Z. Darwazeh
John S. Fairbanks
Douglas J. Fouts
Francis B. Grosz, Jr.
Scott K. Herrington
Yeun Cheul Jeung
John R. Jones
Murari L. Kejariwal
Vladimir Koifman
Kim M. Lau
Heng-Chih Lin
Michael Moyal
Joseph Nahas
Steven R. Norsworthy
Joel W. Page
Alessandro Piovaccari
Harry Q. Pon
Andrzej Pradzynski
Kenneth L. Shepard
Fernando Silveira
Jaime Velasco Medina
Rajan Walia
Lars G. Wanhammar
Eiji Watanabe

# SSCS Elects Five AdCom Members

Five new members will join the IEEE SSCS Administrative Committee when it meets 15 February 2004. The SSCS membership elected Bryan Ackland, Gary Baldwin, Tom Lee, Jan M. Rabaey, and Jan Van der Spiegel last fall. The AdCom is responsible for overseeing conferences, publications, and other potential technical activities within the Society's field of interest. Each AdCom member serves a three-year term. Terms are staggered so there are always some experienced members and some new members. The Nominating Committee puts together a ballot of candidates each summer. A member can petition to be included on the ballot. See details online at *sscs.org/nomelec.htm*.


Bryan Ackland

**Bryan Ackland** received his BSc in physics from Flinders University, Australia, in 1972 and his BE and PhD in electrical engineering from the University of Adelaide, Australia, in 1975 and 1979, respectively.

In 1978 he joined Bell Laboratories as a member of the technical staff in the Image Processing and Display Research Department, where he worked on MULGA —the first successful symbolic layout and compaction tool suite. In 1986 he was appointed director of the DSP and VLSI Systems Research Department where he led research programs in video coding VLSI, multiprocessor DSP architectures, low-power DSP, high-speed optical transceivers, and CMOS imaging.

In 2000 he was appointed vice president of Communications Systems Research at Agere, where he led a team of seventy in a broad range of research topics. He is currently vice president of Advanced Technology at Agere Systems with research interests in novel hardware and software architectures for network and signal processing.

Dr. Ackland is the author of over sixty conference and journal publications and holds eleven U.S. patents. He received Best Paper Awards at ICCD in 1985 and 1990, at DAC in 1986, and in *JSSC* in 1998. He was an editor of *IEEE Transactions on Computers* from 1987 to 1994. He served on the Program Committee for the IEEE International Conference on Computer Design from 1988 to 1994 and has been a member of the CICC Program Committee since 2001. He has been a member of the IEEE/ACM Design Automation Conference Executive Committee since 1997 and a member of the ISSCC Executive Committee since 2001. He served on the IEEE SCCS Nominating Committee from 1998 to 1999.

Dr. Ackland was elected an IEEE Fellow in 1992 for contributions to the design of custom integrated circuits for signal-processing applications. He became a Bell Laboratories Fellow in 1993 for leadership in VLSI tools and circuits.


Gary L. Baldwin

**Gary L. Baldwin** received his BS, MS, and PhD degrees in electrical engineering in 1966, 1967, and 1970, respectively, all from the University of California, Berkeley.

Dr. Baldwin was an acting assistant professor of electrical engineering at the University of California, Berkeley, during 1969 and 1970. He was a member of the technical staff at Bell Telephone Laboratories, Holmdel, New Jersey, from 1970 to 1978. He joined Hewlett-Packard Laboratories, Palo Alto, California, in 1978. He was director of the Solid-State Technology Laboratory at Hewlett-Packard from 1987 until 1999. Since November 1999 he has been at the University of California, Berkeley, as the executive director of the Gigascale Silicon Research Center. As of February 2003, he is the executive director of the Center for Information Technology Research in the Interest of Society (CITRIS). He is also an associate dean for Industrial Relations in the College of Engineering at Berkeley.

Dr. Baldwin was a member of the Program Committee of the International Solid-State Circuits Conference from 1974 to 1982 and served as the secretary of the conference from 1977 to 1980. He was an associate editor and editor of the *IEEE Journal of Solid-State Circuits* from 1977 to 1982. He also served as secretary of the IEEE Solid-State Circuits Council from 1982 to 1984, was vice president of the council from 1984 to 1986, and was its president from 1986 to 1988. He was the program co-chair of the International Conference on Semiconductor and Integrated Circuit Technology in Beijing, China, in 1995, and is a member of the AdCom of the IEEE Solid-State Circuits Society.

Dr. Baldwin is a member of Eta Kappa Nu and Sigma Xi, is a Fellow of the IEEE, and was a recipient of the IEEE Third Millennium Medal.


Tom Lee

**Tom Lee** received his degrees in electrical engineering from the Massachusetts Institute of Technology, escaping with an ScD in 1990. He then joined Analog Devices where he was primarily engaged in the design of high-speed clock recovery devices. In 1992 he joined Rambus Inc. in Mountain View, California, where he developed high-speed analog circuitry for 500-megabyte/s CMOS DRAMs.

He has also contributed to the development of PLLs in the StrongARM, Alpha, and AMD K6/K7/K8 microprocessors. Since 1994, he has been with the electrical engineering faculty at Stanford University, where his research focus has been on gigahertz-speed wireline

and wireless integrated circuits built in conventional silicon technologies, particularly CMOS.

Lee has twice received the Best Paper Award at the International Solid-State Circuits Conference, co-authored a Best Student Paper at ISSCC, received the Best Paper Award at CICC, and was awarded a Packard Foundation Fellowship in 1998.

He is an IEEE Distinguished Lecturer of both the Solid-State Circuits and Microwave Societies. He holds twenty-five U.S. patents, authored *The Design of CMOS Radio-Frequency Integrated Circuits* (Cambridge Press, 1998), and co-authored three books on RF circuit design. Lee cofounded Matrix Semiconductor in 1998 and maintains an active interest in chamber music as a violinist and tenor.

Jan M. Rabaey

**Jan M. Rabaey** received his EE and PhD degrees in applied sciences from the Katholieke Universiteit Leuven, Belgium. From 1983 to 1985 he was at the University of California, Berkeley, as a visiting research engineer. From 1985 to1987 he was a research manager at IMEC, Belgium, and in 1987 he joined the faculty of the Electrical Engineering and Computer Science Department of the University of California, Berkeley, where he holds the Donald O. Pederson Distinguished Professorship. He has been a visiting professor at the University of Pavia (Italy), Waseda University (Japan), and Victoria University (Australia).

From 1999 until 2002 he was the associate chair of the EECS Department at Berkeley. He is currently the scientific co-director of the Berkeley Wireless Research Center (BWRC), as well as the director of the MARCO GigaScale Systems Research Center (GSRC).

Professor Rabaey received numerous scientific awards, including the 1985 *IEEE Transactions on Computer-Aided Design* Best Paper Award (CAS), the 1989 Presidential Young Investigator Award, the 1994 Signal-Processing Society Senior Award, and the 2002 ISSCC Jack Raper Award. He is an IEEE Fellow and has served as associate editor for the IEEE *Journal of Solid State Circuits* and the *TODAES ACM Journal*. He is past chair of the VLSI Signal Processing Technical Committee of the Signal Processing Society, and chaired the International Symposium on Low-Power Electronics and the IFIP Conference on Mobile Computing in 1996. From 1994 until 2002 he served on the Executive Committee of the Design Automation Conference, of which he was both technical program chair and general chair.

His current research interests include the conception and implementation of next-generation integrated wireless systems. This includes the analysis and optimization of communication algorithms and networking protocols, the study of low-energy implementation architectures and circuits, and the supporting design automation environments.

Jan Van der Spiegel

**Jan Van der Spiegel** received his Masters and PhD degrees in electrical engineering from the University of Leuven, Belgium, in 1974 and 1979, respectively. He joined the University of Pennsylvania in 1981 where he is currently the interim chair of the Department of Electrical and Systems Engineering and the director of the Center for Sensor Technologies. His research interests are in mixed-mode VLSI design, biologically based sensors and sensory information processing systems, microsensor technology, and analog-to-digital converters. He is the author of over 150 journal and conference papers and holds four patents. He is a Fellow of the IEEE (2002) and the recipient of the IEEE Third Millennium Medal, the UPS Foundation Distinguished Education Chair, and the Bicentennial Class of 1940 Term Chair. He received the Christian and Mary Lindback Foundation Award and the S. Reid Warren Award for Distinguished Teaching.

He has served on several IEEE program committees and is currently the program secretary of the International Solid-State Circuit Conference (ISSCC). He has also served on the Technology Directions Committee and the Executive Committee of the ISSCC. He has been the chapters chairs coordinator of the IEEE Solid-State Circuits Society (SSCS) for the past six years. Under his leadership, the SSCS chapters have grown from a few to over forty worldwide. He is also a member of the SSCS Membership Committee.

# Letter to the Editor—It Wasn't Madame Curie

I read with surprise in the October Newsletter in your summary of ferroelectric memory research that, "The ferroelectric phenomenon was first discovered and described by Madame Curie."

Marie Curie may be responsible for ferromagnetism. I have no references on hand which would settle this question. However, the ferroelectric phenomenon was first reported by Joseph Valasek in 1921 (at the University of Minnesota). The material was "Rochelle salt."

(References: J. Valasek, Physics Review 17, 1921, p.475 and Jona and Shirane, "Ferroelectric Crystals," Pergamon Press, 1962, p. 280.)

**John Shier**
*IEEE Senior Member*
(Retired and instructing at Normandale Community College, Bloomington, Minnesota)

# Solid-State Circuits Society Is Volunteer Powered—The CICC Case Study

**Phil Diodato, CICC General Chair**

**Doug Garrity, CICC Education Sessions Chair**

**Elliot Gould, CICC Technical Program Committee**

**Takayasu Sakurai, CICC Technical Program Committee**

**Jafar Savoj, CICC Panel Sessions Chair**

**Trudy Stetzler, Technical Program Chair 2003**

**Johan Van Der Tang, CICC Technical Program Committee**

SSCS and IEEE have uncovered, through member surveys this year, the fact that many members don't realize that volunteers really do most of the work in IEEE. And many members say they would like to volunteer but don't know how.

Conferences, chapters, and the *Journal* are all organized and produced with volunteer effort. This is the first in a series of SSCS newsletter articles about the volunteers behind the scenes; who they are, what they do, and how they got started. With these case studies readers may decide to seek places for themselves on these committed and engaged teams of technical professionals.

We'll begin with interviews of volunteers for the Custom Integrated Circuits Conference (CICC), an annual SSCS conference with attendance of approximately 400 and a Technical Program Committee (TPC) of 79 members. For its 25th year CICC changed its meeting to the fall after 24 years of being held in May. "CICC stands by a simple mode of operation that is defined by 'Innovation, Education, and Communication,'" points out General Chair, Phil Diodato.

**Two-thirds of members who volunteer with IEEE answered survey questions indicating they are either satisfied or highly satisfied with their volunteer experience. But 85% of our members haven't ever had a volunteer job. And 65% of our members don't understand the structure of SSCS enough to know how to volunteer if they want to.**

**(From the IEEE All Society Research Project 2003, research coordinated by the IEEE Research, Corporate Strategy and Communications.)**

## How CICC Volunteers Got Started

Johan Van Der Tang used to visit several circuit conferences but until 2000 he hadn't visited the IEEE CICC yet. "In that year I had a paper presentation on tunable filters and, if I recall it accurately, before and after the session members of the Technical Program Committee mentioned that they were looking for some new TPC members. I had just moved from Philips Research Eindhoven to Eindhoven University of Technology and thought it would be rewarding if I could join the TPC. Obviously, I enjoyed the high technical level of the conference. It is a wonderful opportunity to broaden one's technical horizon. And this has a lot of synergy with being an assistant professor. Hence during one of the author interviews, I approached one of the TPC members, and after that I got an invitation to send in a CV and ended up being one of the freshmen of TPC 2001."

Takayasu Sakurai of the University of Tokyo recalls his beginning involvement with the conference as a replacement for Dr. Susumu Kohyama from Toshiba "who nominated me to the CICC Steering Committee when he retired from the TPC of the CICC about fifteen years ago."

Doug Garrity of Motorola, Education Sessions Chair in 2003, recalls that a friend of his, Allen Barlow, was serving as the Technical Program Chair in 1993. Garrity was attending the conference and talking with Barlow and just offered to help. "I knew that his was an incredibly difficult job and said if you need help with this, I'd be happy to help. And the next thing, I was busy."

Trudy Stetzler of Texas Instruments, the 2003 Technical Program Chair, "attended CICC for several years, and had presented some educational sessions. I discussed with one of my friends who was on the TPC what it was like, and the responsibilities involved, and thought it would be an interesting experience. He introduced me to several of the steering team members, who asked me to send a resume for their review. The steering team invited me to join the CICC TPC."

## What Volunteers Do

Garrity points out, "Everybody has two CICC jobs. On the CICC TPC everyone serves on a topical subcommittee for paper review as well as being involved in one of the organizational committees, such as Educational Sessions or Publicity."

Elliot Gould of Motorola says that, for most, "reviewing the papers is

the biggest job." Van Der Tang sees his primary task as being a member of the wired subcommittee. "The biggest part is encouraging people to send in papers and reviewing papers of your subcommittee. You rely on your network of people in the industry and colleagues you know from other universities. For example, I've spent five years at Philips Research and know a lot of people and their work within Philips. Hence I was successful several times in getting some submissions from Philips."

Sakurai describes one of his rolls is "to promote public relations and to enhance visibility to attract more people to the conference." He does this though his own "e-mail list, recommending information and sending it to NIKKEI and other press media." He recruits papers simply by calling people and talking to them. The biggest part of his job is "reading papers and selecting good papers to make a technically attractive program."

Stetzler describes how the conference comes together with each TPC member playing these double roles. "The conference TPC has two meetings, TPC-1 in January and TPC-2 in May prior to the conference. They are one day each. TPC-1 is mostly a planning meeting—identifying papers to invite and authors/companies to solicit for papers. The organizational committees also set their plans at this meeting, such as potential exhibiters and events, educational session tracks, potential speakers, panel topics, and potential panelists." TPC-2 in May is primarily dedicated to paper selection.

## What Happens in the Panel and Education Committees

Jafar Savoj from UCLA says the biggest job of the Panel Sessions Chair is "to come up with a comprehensive list of panel topics, and to help find good panelists to speak on the selected panels. Most of the ideas are collected from the surveys that go to the TPC members before our first meeting. On some occasions, unanswered questions in one panel give rise to new panel topics. Also, some suggestions come from individuals or companies who want to introduce a new trend in IC technology."

From a list of 100 suggestions, the Panel Committee members select their top ten and narrow the list. Then Savoj presents the top picks to the TPC and collects their vote. "We pick the three panels with the highest number of votes to be presented at the conference. Then we invite the individuals who have either established a reputation for their contributions to the topic or work for the companies that lead the related technologies. The panel moderators and the panel committee members try to identify these experts. We invite people who have published on the topic and people who are responsible for making strategic decisions."

"We are looking for volunteers who give us new ideas for the panels, like to present their strong opinion as a panelist, or put us in touch with people who are excellent candidates to sit on a panel. The primary job of a panel member is to educate the audience. He or she should be able to present an in-depth analysis of the topic and provide a very clear vision. The panelist should be able to respond to the questions from the audience and defend his or her ideas," Savoj points out.

Garrity, as Education Committee Chair, cautions that "We rarely take somebody who just comes in and says here's an idea for an Ed session that we can give and we'll do a great job. It has to be somebody we know is technically proficient and who also is an excellent speaker. There is an Education Subcommittee of fifteen people where basically we come up with topics and speakers and we focus on those choices. There is always a mix between getting the right speakers and getting all the right topics we want. There are some people that could come and talk about whatever they wanted because they're excellent speakers and are a big draw."

The Steering Committee asks a member of the TPC to serve as an organizational or session chair. The job of an organizational chair for any of the committees is a two-year commitment.

## What Happens in the Paper Review Committees

Stetzler describes the process. "The reviewers receive the papers submitted to the conference about three weeks before the second TPC meeting in late May. They then must read all the papers for their subcommittee and evaluate them for technical merit, originality, clarity, and significance. Some of the subcommittees get quite a few papers, so this is usually a busy time for the reviewers. They must send their scores to the subcommittee chair usually a couple of days before TPC-2 so the chair can combine them all into one spreadsheet for review at TPC-2. TPC-2 is the final discussion and selection of the papers. This is the meeting where the entire technical program is put together—number of sessions, total papers per session, which sessions are on which day—everything needed for the advanced program."

The number of papers per topical subcommittee ranges from 45 to about 65. Paper submissions increased by 50% for the 2003 conference but even the Wireless subcommittee, with the high of 68 papers, was "still manageable." Stetzler points out that "The number of papers is something we watch …if it does get too high, we may need to rethink how the committees are partitioned and perhaps change the partitioning."

Gould offers more insights into the paper selection process. "The majority of the papers that are rejected simply fall short in one or more of the scoring categories (technical merit, clarity, originality, and significance) making them, by definition, not very interesting pieces of work. Some good papers are rejected because there may be a lot of very good papers that year, and they simply missed the cut. Other papers that are good may be off topic from

the themes that develop as the conference program is created. Most of the time though, if the paper is good, we find a way to include it in the conference," Gould observed.

"All the reviews are unbiased," Stetlzer continues. "For example, if the paper is from TI, I don't vote on the paper and I leave the room for all the discussions (to allow an unbiased discussion)." Gould agrees, "Everyone who I have interacted with at the CICC has been nothing but very professional about conflicts of interest. Everyone goes out of their way to ensure they cannot be accused of favoring their allegiances." Van Der Tang continues, "For me region is irrelevant. Technical content, merit, and, hopefully, some incremental or stepwise advancement of science is of importance."

## Why Volunteers Enjoy Volunteering

All agree that it is the people they work with on CICC that provide the most satisfaction. Garrity is pleased to have "gotten to rub shoulders with all of the top analog design people in the world at one time or another from being associated with this conference." Van der Tang quotes Newton, "'We are standing on the shoulders of a giant.' Open literature and knowledge, conferences like the CICC contribute to that and it is nice to be part of that."

Garrity also resonates with some fundamental organizational choices of the conference. "CICC gets four pages for digest submission, not one page of text and one page of illustrations like some other conferences. The CICC tagline says it is about education. It is the place to learn how to do your job better, versus other conferences that are a place companies go to say this is what we do."

Savoj credits organizing panels as helping him "to learn about what people think will come up in the industry, and how research and development in the fast-paced solid-state circuits society may evolve in the coming years."

## Real Jobs and Volunteer Jobs

Stetzler's employer views her CICC activity as "a useful career growth opportunity for me, as well as a benefit to TI to have someone from the company invited to be a part of the Technical Program Committee. The conference itself is a useful learning and educational event. They support the travel to the meetings and the conference as well as that time away from my 'real' job. Of course, there are still many additional hours required outside of this time away that are a commitment on my part to help make CICC a successful conference. TI does get some recognition out of having a person on the technical program committee."

Gould's management requires him to annually justify why his participation is useful enough to the employer to support him. Gould prefers "to think of this work as falling into the general 'education' category. The CICC provides a unique educational opportunity in many dimensions. First, it has wonderful educational sessions before the conference. Second, the conference papers are very technical, typically containing circuit-level detail. And the EDA vendors always come exhibit, providing a close, intimate setting to interact with them versus DAC, which has a bigger exhibit." Personally, Gould enjoys "forcing" himself to "delve deeply into engineering subject matters that are outside my immediate area of expertise through the paper review process."

Sakurai agrees that without CICC, his busy schedule would prevent him from sparing the time to read papers, accessing "their practical yet first-class technical achievements." Van der Tang credits the in-depth reading of the papers required for the selection process as providing him an opportunity to "acquire a lot of insight and new 'circuit tricks'."

## How Should a Newcomer Get Started?

During the CICC all committee members wear white ribbons. If you are interested, "just make your interest clear to one of those persons. I think the contact info on the Web page of the CICC (*www.ieee.cicc.org*) is also a possibility," Van Der Tang advises. Stetzler agrees, "contact any member of the steering team to find out what the responsibilities are and the commitment that they are required to make. We usually ask for a resume to see how the individual would fit in with the current technical program committee."

Sakurai is interested in nominating more participants from his region who would increase the papers and attendance at CICC. For the Far East region, he relies on the local custom of semiconductor companies recommending a representative.

The best time for volunteering to join the TPC is during and immediately after the conference occurs. For the 2004 conference, Diodato reports that the committee staffing was almost done by mid-November. Certainly suggesting panel topics after the advance program has gone out is too late. Savoj indicates those late summer "suggestions will be added to the list of topics for the following year. The topics of our panels are selected in January and the list of panelists is finalized by June of every year."

Van der Tang concludes about his involvement in CICC TCP that, "the benefits outweigh the invested time by an order of a magnitude."

**Anne O'Neill**
*SSCS Executive Director*
a.oneill@ieee.org

See a slice of what CICC volunteers work to bring you. Links to CICC outstanding papers are listed at *sscs.org/pubs/CICCoutstnd.htm*.

IEEE members have access to abstracts through IEEE *Xplore*™. Access to full conference articles in pdf may be through your employer's account, a subscription to the SSC Conference Digital Library, or the IEEE Member Digital Library. Individual article purchase is also an option in IEEE *Xplore*.

# Books of Interest to SSCS

This selection of technical books published in 2003 covers topics that may be of interest to our members. The descriptions are provided by the publishers.

**Analysis and Design of Digital Integrated Circuits**
by David Hodges, Horace Jackson, and Resve Saleh, published by McGraw-Hill, July 2003, $128.12, ISBN 0-072-28365-3.

The third edition of Hodges and Jackson's *Analysis and Design of Digital Integrated Circuits* has been thoroughly revised and updated by a new co-author, Resve Saleh of the University of British Columbia. The new edition combines the approachability and conciseness of the Hodges and Jackson classic with a complete overhaul to bring the book into the 21st century.

The new edition has replaced the emphasis on bipolar with an emphasis on CMOS. The outdated MOS transistor model used throughout the book is replaced with the now standard deep submicron model. The material on memory has been expanded and updated. The book now includes more on SPICE simulation and new problems that reflect recent technologies.

The emphasis of the book is on design, but it does not neglect analysis; it provides enough information for a student to carry out analysis or design a circuit. This book provides an excellent and balanced introduction to digital circuit design for both students and professionals.

**CMOS Digital Integrated Circuits: Analysis and Design**
by Sung-Mo (Steve) Kang and Yusuf Leblebici, published by McGraw-Hill, October 2003, $109.06, ISBN 0-072-46053-9.

*CMOS Digital Integrated Circuits: Analysis and Design* is the most complete book on the market for CMOS circuits. Appropriate for electrical engineering and computer science, this book starts with CMOS processing, and then covers MOS transistor models, basic CMOS gates, interconnect effects, dynamic circuits, memory circuits, BiCMOS circuits, I/O circuits, VLSI design methodologies, low-power design techniques, design for manufacturability, and design for testability.

The book's rigorous treatment of basic design concepts with detailed examples addresses both the computer-aided analysis issues and the design issues for most of the circuit examples. Numerous SPICE simulation results also are provided for illustration of basic concepts. Through analysis of CMOS circuits in this text, students will be able to learn the fundamentals of CMOS VLSI design, which is the driving force behind the development of advanced computer hardware.

**Design Through Verilog HDL**
by T. R. Padmanabhan and B. Bala Tripura Sundari, published by John Wiely & Sons, October 2003, $79.95, ISBN 0-471-44148-1.

Verilog provides platforms for describing designs at different layers of complexity, combining them in a seamless manner, testing them at every stage, and building a bug-free design. This book enables readers to master Verilog as an HDL for design. *Design Through Verilog HDL* engages readers at every stage through the variety and number of examples.

**Digital Audio Broadcasting: Principles and Applications of Digital Radio**
by Wolfgang Hoeg and Thomas Lauterbach, published by John Wiley & Sons, October 2003, $98.00, ISBN 0-470-85013-2.

An innovative and universal multimedia broadcast system, the new digital radio system, Digital Audio Broadcasting (DAB), is sure to replace existing AM and FM broadcast service in much of the world in the near future. Combining the knowledge of leading experts in the field, this fully updated new edition introduces the recent international standards, applications, and technical issues of the Eureka 147 DAB system.

**Device Modeling for Analog and RF CMOS Circuit Design**
by Trond Ytterdal, Yuhua Cheng, and Tor A. Fjeldly, published by John Wiley & Sons, May 2003, $99.95, ISBN 0-471-49869-6.

Bridging the gap between modeling and analog circuit design, *Device Modeling for Analog and RF CMOS Circuit Design* will appeal to practicing microelectronics engineers and senior- and graduate-level students taking courses in analog integrated circuit design. In order to keep up with global demand, microelectronics engineers are continually challenged to produce increasingly complex, high-performance integrated circuits. The steady downscaling of MOSFET/CMOS technology has highlighted the need for a thorough understanding of the properties, potentials, and limitations of the latest device models and technology. Presenting state-of-the-art MOSFET models, this book will prove a valuable reference and text for engineers striving to achieve first-time right, reduced time-to-market silicon products. Two software packages, AIM-Spice and MOSCalc, are available via the internet.

**Lab on the Web: Running Real Electronics Experiments Via the Internet**
by Tor A. Fjeldly and Michael S. Shur, published by John Wiley & Sons (IEEE Press), September 2003, $74.95, ISBN 0-471-41375-5.

*Lab on the Web: Running Real Electronics Experiments Via the Internet* is a groundbreaking resource for remote study of interactive electronics applications. The widespread use of the internet as a communication medium has opened up a broad range of possibilities for extending its use into new areas. One such area is remote education, a rapidly growing part of today's university

curricula. Using the internet and Web technology, courses can be offered to students anywhere in the world with no more technical requirements than a personal computer and an internet connection. Until recently however, lab courses have been considered impractical for remote access. But thanks to technical advances of the past decade, even these courses with their often-complex interactive techniques have been made accessible to remote students.

This is the first text to present, in detail, experiments that can be run over the Web, specifically in the area of electronics. The authors present detailed descriptions of approximately 100 experiments in solid-state electronics that can be used by engineering and science students at all levels, anywhere in the world, as well as by researchers working on semiconductor devices.

The book's widespread collaboration will enable universities around the world to participate in these remote access experiments. Enhanced by interactive Web sites, which will accommodate a growing array of experimental modules from participating institutions, the text opens up a virtual Pandora's box of possibilities for students to access a wide variety of real experiments, and for institutions (jointly or individually) to establish their own remote laboratory sites.

**Microelectronic Circuits**
by Adel S. Sedra and K. C. Smith, published by Oxford University Press, November 2003, $112.00, ISBN 0-195-14251-9.

The fifth edition of *Microelectronic Circuits* provides a framework to develop a student's ability to analyze and design all kinds of electronic circuits. Thoroughly updated and revised, this edition features changes that are evident from the condensed table of contents, and a great many more that are included in the chapters. All the revisions, organization, and topical coverage reflect changes in technology—CMOS technology in particular—by far the most significant development in the world of mainstream electrical engineering.

**Microelectronic Circuit Design with CD-ROM**
by Richard C. Jaeger and Travis Blalock, published by McGraw-Hill (Higher Education), July 2003, $144.85, ISBN 0-07-250503-6.

*Microelectronic Circuit Design* is known as a technically excellent text. The new edition has been revised to make the material more motivating and accessible to students. A new co-author, Travis Blalock, has joined Jaeger to assist in providing a student-friendly approach. A pedagogical framework has been added that includes chapter opening vignettes, chapter objectives, "Electronics in Action" boxes, a problem-solving methodology, and "Design Note" boxes.

The number of examples, including new design examples, has been increased, giving students more opportunities to see problems worked out. Additionally, some of the less fundamental mathematical material has been moved to the Web site.

**Multi-Carrier and Spread Spectrum Systems**
by Khaled Fazel and Stefan Kaiser, published by John Wiley & Sons, October 2003, $89.95, ISBN 0-470-84899-5.

This highly accessible work describes and analyzes the basic concepts of the combination of multicarrier transmission with spread spectrum (MC-SS).

**Operation and Modeling of the MOS Transistor (Second Edition)**
by Yannis Tsividis, published by Oxford University Press, November 2003, $110.00, ISBN 0-195-17014-8.

Extensively revised and updated, this is the second edition of the highly praised text that has become a standard in academia and industry. The book provides a unified, careful treatment of the MOS transistor with in-depth development of many important models, ranging from the simple to the sophisticated, with the connection between models clearly identified. Many aspects of modeling are covered, including: DC, AC, small-signal, large-signal transient, quasi-static, nonquasi-static, and noise. New material on charge-sheet models, small-dimension effects, noise, and modeling for RF applications is included. A new chapter on modeling for CAD discusses the context, considerations, and pitfalls associated with the development of models for computer-aided design, and describes ways to evaluate them.

**Phase-Locked Loops**
by Roland Best, published by McGraw-Hill, June 2003, $79.95, ISBN 0-071-41201-8.

The communications industry's big move into wireless in the past two years has made this mature topic red hot again. Phase-locked loops (PLLs) are electronic circuits used for frequency control. Anything using radio waves, from simple radios and cell phones to sophisticated military communications gear, uses PLLs.

The fifth edition of this classic circuit reference comes with valuable PLL design software written by Dr. Best. The software alone is worth many times the price of the book. The new edition also includes new chapters on frequency synthesis, CAD for PLLs, mixed-signal PLLs, and a new collection of sample communications applications.

**Signal Integrity—Simplified**
by Eric Bogatin, published by Prentice Hall, September 2003, $89.00, ISBN 0-130-66946-6.

Suitable for even non-specialists, *Signal Integrity—Simplified* offers a comprehensive, easy-to-follow look at how physical interconnects affect electrical performance. World-class engineer Eric Bogatin reviews the root causes of the four families of signal integrity problems and offers solutions to design them out early in the design cycle. Unlike related books that concentrate on theoretical derivation and mathematical rigor, this book emphasizes intuitive understanding, practical tools, and engineering discipline. Specially designed for everyone in the electronics industry, from electrical engineers to product managers,

*Signal Integrity—Simplified* will prove itself a valuable resource for helping you find and fix signal integrity problems before they become problems.

**ULSI Semiconductor Technology Atlas**
by Chi-Hang Tung, George T. Sheng, and Chih-Yuan Lu, published by John Wiley & Sons, September 2003, $125.00, ISBN 0-471-45772-8.

*ULSI Semiconductor Technology Atlas* uses examples and TEM (Transmission Electron Microscopy) micrographs to explain and illustrate ULSI process technologies and their associated problems. The natural outgrowth of VLSI (Very Large Scale Integration), Ultra Large Scale Integration (ULSI) refers to semiconductor chips with more than 10 million devices per chip. Written by three renowned pioneers in their field, this book provides a historical introduction to the technology as well as coverage of the evolution of basic ULSI process problems and issues. Additional advanced microelectronics devices and materials, such as flash memories, SOI, SiGe devices, MEMS, and CD-ROMs, are also explained and illustrated with TEM.

# Chapters Make SSCS Vital Around the World

**Bulgaria Chapter**—Albert Wang, of the Illinois Institute of Technology and SSCS Distinguished Lecturer visited the SSC/ED chapters in Sofia and Varna, Bulgaria, in early August 2003. Marin Hristov of the Technical University of Sofia, Chapter Chair of the SSC Sofia Chapter, organized the visit in Sofia, which included general discussion of IEEE chapter activities and issues, as well as lab visits. In the afternoon, Wang delivered a Distinguished Lecture at Melexis, a major microelectronics company in Bulgaria. The lecture was very well received by an audience of approximately forty. Technical discussions followed the lecture. The next day Jordan Kolev of the Technical University at Varna hosted a chapter meeting with Wang presenting another Distinguished Lecture on ESD protection.

**Minsk Chapter**—Wang also visited the SSC Belarus–Minsk Chapter 7–8 July 2003, and was hosted by the Minsk Chapter Chair, Sergei Malyshev, of the National Academy of Sciences of Belarus. On 7 July, Wang delivered a Distinguished Lecture at Integral (a regional microelectronics giant) on advanced ESD protection for ICs, which was well


**Albert Wang, SSCS Distinguished Lecturer, visiting with Chapter Chair Martin Hristov of the Technical University of Sofia, Bulgaria.**


**SSC/ED Varna, Bulgaria, Chapter Meeting 2 August 2003. On the left is Chapter Chair Jordan Kolev; Albert Wang, SSCS Distinguished Lecturer, is fifth from the left.**


**Albert Wang, SSCS Distinguished Lecturer, visiting with Minsk Chapter Chair Sergei Malyshev of the National Academy of Sciences of Belarus.**

accepted by the audience of about forty. Discussion followed the lecture, including reviews of some related recent designs by members of the National Academy. Mutual interests in future collaboration on related IC designs were discussed. On 8 July Wang visited the Institute of Electronics of the National Academy of Sciences.

Professor Malyshev expressed appreciation of society financial support for IEEE membership (membership fee subsidies) as critical to maintaining local chapters. The Minsk SSCS and EDS chapters have been doing quite well with many organized activities. However, other IEEE society chapters have stopped functioning due to the membership drain caused by the fee, which is a burden to local members with lower incomes. Wang reported that, overall, this was a very fruitful visit.

**West Ukraine**—The West Ukraine Chapter organized the 8th International Seminar/Workshop on Direct and Inverse Problems of Electromagnetic and Acoustic Wave Theory (DIPED-2003) 22–25, September 2003. The Republic of Georgia Chapter was co-organizer of this event. The Electron Devices Society provided technical co-sponsorship and inclusion of the Seminar Proceedings into the IEEE Book Broker Program. The MTT-S, AP-S, CPMT-S, SSC-S, and Ukraine Section were among the supporting IEEE institutions. The Seminar/Workshop was held at the Pidstryhach Institute of Applied Problems of Mechanics and Mathematics, NASU, Lviv, Ukraine.

Forty-eight papers of participants from Georgia, Germany, China, Lebanon, Poland, Russia, UK, and Ukraine were presented in the 6 oral sessions:

- Theoretical aspects of electrodynamics
- Complex media
- Diffraction and numerical methods
- Antennas and transmission lines,
- Mobile antenna radiation
- Acoustics and field measurement

The paper topics covered the traditional scientific areas: propagation, diffraction and scattering of waves in homogeneous and non-homogeneous media, synthesis of radiating systems and field transformers, restoring the shape of radiating and scattering bodies, as well as the novel problems such as study and simulation of electromagnetic field in the complete vehicle structure, development and modeling the new antenna system for mobile phones, and decreasing the interaction of electromagnetic field of mobile phones on the human body.

**The participants of the Direct and Inverse Problems of Electromagnetic and Acoustic Wave Theory (DIPED-2003) held at the Pidstryhach Institute of Applied Problems of Mechanics and Mathematics, NASU, Lviv, Ukraine.**

## 2003 Outstanding Chapter

**The SSCS Bangalore Chapter will be recognized as the SSCS Outstanding Chapter during the ISSCC Plenary Session, 16 February 2004. Look for more details about their activities in the April issue of the newsletter. The Bangalore Chapter is chaired by Navakanta Bhat and is joint with Electron Devices Society.**

# The Denver Chapter Celebrates Its First Anniversary

The SSCS Denver Chapter recently celebrated its first anniversary, having hosted regular monthly technical seminars and occasional social meetings throughout its inaugural year. Attendance regularly exceeded 20 to 35 people, especially positive considering that the meetings were scheduled for Friday afternoons! So far, seminars have been held at Colorado State University in Fort Collins, Colorado, thanks to the assistance of Professor Derek Lile of the EE Department.


**Newly elected officers from left to right: Alvin Loke, Vice Chair; Don McGrath, Chair; Bob Barnes, Treasurer; Tin Tin Wee, Secretary/Webmaster.**

The Denver Chapter was founded by Dr. Randy Rannow of Hewlett-Packard and kicked off its inaugural meeting on 27 September 2002 with a much-anticipated Distinguished Lecture on phase noise in LC oscillators by UCLA EE Professor Asad Abidi. Since then, invited speakers have covered topics ranging from circuit techniques and systems to device technology trends and innovations. Following Professor Abidi's talk, Dr. Stan Williams of HP Labs, Palo Alto, California, gave an inspiring presentation on molecular electronics and quantum computing. The following month, Peter O'Neill of Agilent Labs, Fort Collins, Colorado, shared his perspectives and insights on IC technology trends. Chapter founder, Dr. Rannow, was soon transferred to another HP site—many thanks to him for his initiative and efforts.

Chapter activities were continued by Dr. Don McGrath of LSI Logic and Dr. Alvin Loke and Bob Barnes, both of Agilent Technologies. The first technical activity in 2003 was an editorial of ISSCC 2003 papers and trends, presented by Jay Ackerman and Steve Burnham of LSI Logic and Bob Barnes of Agilent Technologies. That was followed by two Distinguished Lecturer seminars—the first by Professor Albert Wang of the Illinois Institute of Technology, Chicago, Illinois, who presented novel ESD techniques, and the second by Dr. Dick Hester of Texas Instruments, Dallas, Texas, who taught an insightful forum on techniques and challenges of analog front-end design for ADSL. In the next month, Chapter Chair, Dr. Don McGrath, presented a well-received tutorial on sigma-delta A/D converters and summarized his PhD. findings on applying genetic algorithms to optimize sigma-delta designs. Next, Professors Dragan Maksimovic and Regan Zane from the University of Colorado, Boulder, Colorado, delivered an informative lecture on digital control of switching power converters and pulse-width modulators.

The Chapter's most recent activity was another well-received tutorial, this time conducted by Dr. Alvin Loke, Chapter Secretary/Webmaster, who lectured on copper/low-K interconnects and electromigration fundamentals and shared his perspectives on technology trends. Within the year, two well-attended social events were hosted at a local clubhouse. Members of the local SSCS chapter and interested non-members are discovering that Fort Collins and its vicinity are home to a large community of friendly designers engaged in many exciting circuit activities. We have just conducted annual elections for 2004 at which time Tin Tin Wee joined the existing officer team. Here's to a successful chapter start!

Please visit our Web site at *ewh.ieee.org/r5/denver/sscs/* for more information (including past presentation slides) about our chapter events.

**Alvin Loke**
*Denver Chapter Vice Chair*
alvin.loke@ieee.org

# SSCS EVENTS CALENDAR

**Also posted on *www.sscs.org/meetings***

## SSCS SPONSORED MEETINGS

### 2004 ISSCC International Solid-State Circuits Conference

*www.isscc.org* 15–19 February 2004
San Francisco Marriott Hotel, San Francisco, CA, USA
Contact: Courtesy Associates, ISSCC@courtesyassoc.com

### 2004 Symposium on VLSI Circuits

*www.vlsisymposium.org* 17–19 June 2004
Hilton Hawaiian Village, Honolulu, HI, USA
Paper deadline: 7 January 2004
Contact: Phyllis Mahoney, vlsi@vlsisymposium.org or
Business Center for Academic Societies, Japan
vlsisymp@bcasj.or.jp

### 2004 CICC Custom Integrated Circuits Conference

*www.ieee-cicc.org* 3–6 October 2004
Caribe Royale Resort Suites, Orlando, FL, USA
Paper deadline: 5 April 2004
Contact: Ms. Melissa Widerkehr, cicc@his.com

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## TECHNICALLY CO-SPONSORED MEETINGS

### 2004 Radio Frequency Integrated Circuits Symposium

*www.rfic2004.org* 6–8 June 2004
Fort Worth, TX, USA
Paper deadline: passed

### 2004 European Solid-State Circuits Conference

*www.esscirc.org/* 20–24 September 2004
Leuven, Belgium
Paper deadline: 22 March 2004

### 2004 International Symposium on Low-Power Electronics and Design

Web site: www.islped.org 9–11 August 2004
Newport Beach, CA, USA
Paper deadline: 5 February 2004

### 2004 Symposium on VLSI Technology

*www.vlsisymposium.org* 15–17 June 2004
Hilton Hawaiian Village, Honolulu, HI, USA
Paper deadline: 7 January 2004

## SSCS COOPERATES TO BRING TO YOUR ATTENTION

### 2004 IEEE Microelectronics in Communications Workshop

*www.imicw.org* 19–21 April 2004
Beautiful Resort, Georgia, USA
Paper deadline: 10 January 2004

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