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SOLID-STATE CIRCUITS

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IEEE

Hu and Ko to Receive 2002 IEEE Solid-State Circuits Award

The 2002 IEEE Solid-State Circuits Award recipients, Chenming Hu and Ping K. Ko, are being honored for their development of device models used for IC design. The award citation is "for BSIM3 modeling and development work."

Hu and Ko's remarkable research partnership systematically produced physical models for nearly all features of the electrical behavior of modern MOSFETs. The series of MOSFET models they developed for IC simulation are known as BSIM (Berkeley Short-channel IGFET Model).

After a decade of progressive improvement, BSIM3v3 was acknowledged as the world's first and only industry-standard public-domain device model.

In the 1980s and early 1990s Hu and Ko's BSIM1 and BSIM2 models were widely used for IC design. Advanced devices designed and fabricated in the course of their modeling research set MOSFET speed records in 1987 and 1992. The BSIM3 model released in 1995 incorporated more than a dozen physical models and was ground breaking in its accuracy. Its ease of parameter extraction gave users the ability to predict the effect of technology changes and manufacturing variations on MOSFET characteristics.

The BSIM model is almost universal today. Since 1997 all silicon foundry companies, most fabless companies, and most integrated device manufacturers have converted to BSIM. By providing the industry with a standard model, BSIM has streamlined the interactions between corporate partners, and foundries and their clients. Its benefit to industry will make a significant impact for years to come.

Chenming Hu

Ping K. Ko

Model based on device physics, not curve fitting

A device-compact model should capture and make available to circuit designers all the manifestations of device design and manufacturing variations that may affect circuit performance. The compact model is the principal communication link between technology/manufacturing and design and products. BSIM3

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Charles Sodini Elected Society President
Steve Lewis elected Vice President

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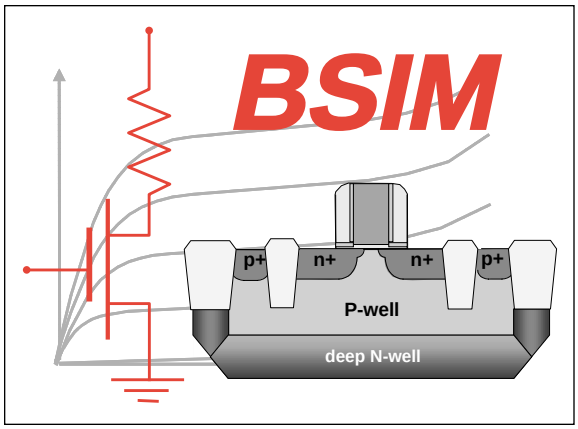
and BSIM4 provide the strong link that IC technology scaling requires.

Hu and Ko, with their students, developed models for velocity saturation, velocity overshoot, mobility degradation, channel electric field, substrate current, gate-induced drain current, output conductance, V_t roll-off, reverse short-channel effect, short-channel intrinsic capacitances, non-quasi-static transient currents, and more. They also co-authored about 200 papers on the physical models of MOSFETs.

Because BSIM3 incorporates many original physical models developed by Hu and Ko, it changed compact modeling from a curve-fitting exercise to sound device physics. For example, it includes the models of three different mechanisms responsible for the output conductance, bias-dependent thickness of the inversion layer, universal mobility, a flicker noise model unifying the carrier and mobility fluctuations, and the non-quasi-static effect, among other effects. BSIM4, released in October 1999, is accurate up to the MOSFET cutoff frequency. This model can be used to design both digital processors and RF circuits. It also introduced the first major new thermal noise model in 20 years.



Their research with others also led to the co-invention of several novel MOS devices, including the Dynamic Threshold MOSFET (DTMOS). In a DTMOS 0.5 V forward bias is applied to the source and body by the gate turn-on signal to lower V_t, increasing circuit speed at very low V_{dd}. Teaming more broadly provided another co-invention: the source-side-injection flash memory, which uses 1,000 times less programming current and power. Both are used in commercial products.

Their source code is in the public domain

Hu and Ko have provided the source codes of all their models including BSIM3, BSIM4, and BSIM-SOI to all users at no cost. The Web site for downloading the codes, test results, benchmark model parameters, and manuals is available for public use. Users do not have to be paid members of an industry trade association or consortium of manufacturers.

In 1996 BSIM3v3 was selected by the Compact Model Council of EIA as the world's first industry standard compact model for IC simulation. The Council promotes the standard model and its members are leading semiconductor and CAD companies such as Intel, IBM, TI, Motorola, HP, AMD, Lucent, Cadence, Mentor Graphics, Sematech, Hitachi, Infineon, Philips, and TSMC. BSIM3v3 also won a 1997 R&D 100 award as one of the year's most significant R&D products.

As the industry need grew, Hu and Ko provided quarterly fixes and annual new releases. Basic technical support for users is provided through an email network of 500 users comprised of numerous simulator vendors that distribute BSIM by embedding it in their simulators.

Hu and Ko continue to update BSIM to serve industry needs. BSIM4 is accurate for RF circuit design for the growing wireless market. Their BSIMSOI model serves another emerging technology and recently has been chosen by IBM for future SOI product design.

Hu was recognized earlier with the IEEE Jack A. Morton Award "For outstanding contributions to the physics and modeling of MOS device reliability." This year's Solid-State Circuit Award recognizes the broad contributions to circuit models. Both Hu and Ko are widely known by their teaching through the University of California Extension and televised National Technological University courses that have reached thousands of engineers over the past 15 years.

In May 2001, Chenming Hu was appointed the first Chief Technology Officer for Taiwan Semiconductor Manufacturing Company. Born in China, Hu holds a B.S. degree in EE from National Taiwan University, and M.S. and Ph.D. degrees in EECS from the UC Berkeley. Before joining the UC Berkeley in 1976, he was an assistant professor at the Massachusetts Institute of Technology.

In addition to Hu's teaching role, he has been involved in many activities with related industries. He is the co-founder and Co-Chairman of the Board of Celestry Design Technologies, Inc. and was the Nonvolatile Memory Development Manager of National Semiconductor. In addition, he has acted as a consultant to IBM, TI, AMD, Philips, and TSMC. He is a member of the U.S. National Academy of Engineering, an IEEE Fellow, and a Life Honorary Professor of the Chinese Academy of Science.

Ping K. Ko is Vice-Chairman and Chief Strategy Officer of Authosis, Inc. a venture capital firm he co-founded to focus on investment in IC fabless design companies, targeting the Chinese market. Born in Hong Kong, Ko holds a BS in physics from Hong Kong University, and a PhD in EECS from UC Berkeley. Ko holds six patents and has authored or coauthored one book and over 200 research papers. He is on leave as the Dean of Engineering and Director of

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Call for Nominations and Suggestions for the IEEE Solid-State Circuits Award and Other IEEE Technical Field Awards

Nominations and nominee suggestions are sought for the IEEE Solid-State Circuits Award and other IEEE Technical Field Awards (TFAs). The 22 IEEE TFAs are institute wide and are awarded annually to recognize outstanding contributors to the art and science of electro- and information technologies. Deadline for submission of nominees for TFAs is 31 January of each year.

The Solid-State Circuits Technical Field Award is the most relevant to SSCS members. It is awarded for outstanding contributions in the field of solid-state circuits to an individual or team of not more than three. The presentation includes a Bronze medal, certificate and $10,000.

Other TFAs in areas relevant to the SSCS include:

The **Kiyo Tomiyasu Award** for contributions to technologies holding the promise of innovative applications during the early to mid-career of an individual or team (presented for the first time in 2002).

The **Cledo Brunetti Award** for outstanding contributions in miniaturization in the electronic arts

The **IEEE Masaru Ibuka Consumer Electronics Award** for outstanding contributions to the field of consumer electronics

The **IEEE Morris N. Liebmann Memorial Award** for important contributions to emerging technologies recognized within recent years

The **IEEE Frederik Philips Award** for outstanding accomplishments in the management of R&D resulting in effective innovation

The **IEEE David Sarnoff Award** for outstanding contribution in electronics, with preference given to an individual for achievement in the past ten years.

It is acceptable to nominate an individual or team for more than one TFA for the same work (if the work falls within the scope of the respective TFAs). However, the nominee(s) cannot receive more than one TFA for the same work. A complete list of IEEE Technical Field Awards is available on the IEEE Web site: *www.ieee.org/about/awards/tfalst.htm*. The SSCS Awards Committee welcomes suggestions for nominations for any or all of these awards. Any person may nominate a candidate for an IEEE medal or award; self-nomination, however, is not allowed. The SSCS Awards Committee will help in the nomination process and will undertake finding appropriate nominators if necessary; the Committee can be contacted through the Chair.

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Call for IEEE Fellow Nominations

What do Paul Gray, Mark Horowitz, Stephen Lewis, Nicky Lu, Toshiaki Masuhara, Rudy van de Plassche, and Ian Young and have in common? They are but a few of the many SSCS members that have been elected to the grade of IEEE Fellow through the nomination and support of SSCS members.

The grade of IEEE Fellow recognizes exceptional accomplishment and is conferred by the IEEE Board of Directors on members who have significantly contributed to their technical field. The number of nominations evaluated by our Society is below that of other IEEE societies of comparable size. As a Society, we simply are not doing an adequate job of recognizing the very significant contributions our members have made to our profession. We must reverse this trend.

The Fellow nomination process is relatively straightforward but does require some forethought and planning. The Fellow nomination form is four pages long. It is not difficult to complete and should focus on the technical achievements of the nominated candidate. It is usually completed in collaboration with the nominee.

The deadline for receipt of the nomination form and reference letters is 15 March 2002. The nominator does not have to be an IEEE Fellow or even an IEEE member; self-nomination, however, is not allowed. A minimum of five and a maximum of eight references are required from current IEEE Fellows, who are listed alphabetically at the beginning of the IEEE Membership Directory.

If the nominee is not an IEEE Senior Member, that application and its three supporting references must be submitted no later than 4 February 2002. Senior Member forms and references can be emailed or completed online: Senior-member-forms@ieee.org; URL: www.ieee.org/organizations/rab/md/smforms.htm. Snail mail is also acceptable.

Fellow kits can be requested in hard copy format (Fax: +1 732 981 9019) or downloaded from the Web (email: fellow-kit@ieee.org; URL: www.ieee.org/about/awards/fellows/forms.htm). The Society welcomes suggestions of members who should be nominated for Fellow.

Richard C. Jaeger
Publications Chair

IEEE Solid-State Circuits Society
jaeger@eng.auburn.edu

Congratulations to Our New Senior Members

The Solid-State Circuits Society congratulates its 42 new Senior Members and thanks the nominators and references for their time and effort. The Senior Member grade is a professional recognition by peers for technical and professional excellence. The IEEE provides a wood and bronze engraved Senior Member plaque to display and a gift certificate for $25.00 toward one new Society membership. Upon the request of the newly elected Senior Member, an announcement letter can be sent to his or her employer, to Section publications, and to local newspapers.

Application forms and details are available on the Web site: *www.ieee.org/membership/upgrade.htm*. The qualifications are straightforward: a completed application and the references of three IEEE Senior Members or Fellows. Asking peers and superiors for recommendations may be difficult; however, reaching out for such professional support and advice is an important part of an engineer's career and should be a welcome challenge.

Other requirements for Senior Member grade include ten years in the profession (though not ten years of IEEE membership). The highest degree is counted toward this ten-year requirement as follows: three years for a BS degree, four years for an MS degree and five years for a Ph.D.

Five years of significant performance is required, which can include one or more of the following:

a. Substantial engineering responsibility or achievement
b. Publication of engineering or scientific papers, books or inventions
c. Technical or management of scientific or engineering work
d. Recognized contributions to the welfare of the profession
e. Development or expansion of courses taught at an accredited educational institution
f. Equivalent contributions in areas such as technical editing, patent prosecution, or patent law.

More details can be found on the Senior Member Web pages. Members are advised to plan for this professional advancement. Senior level membership is just one of the requisites to qualify for the distinct recognition of elevation as an IEEE Fellow. Many qualified Fellow applicants have elevation delayed because of failure to plan ahead for this step.

New Solid-State Circuit Senior Members

Andrea Baschirotto
Olga Boric-Lubecke
Mansun Chan
Won-Jae Choi
Anthony G. Dunne
Milos D. Ercegovac
Adel Ghazel
Joseph P. Heck
Yin Hu
Koichiro Ishibashi
Takamaro Kikkawa
Wolfgang Kraus
Chun-Lim Lau
Francois Le Chevalier
Jong Ho Lee
Mankoo Lee
Yong-Hyun Lee
Mark W. Maloney
Akira Matsuzawa
James T. May
Donald P. Monroe
Robert A. Mullen
S. S. Narayanan
Sreedhar Natarajan
William E. Nehrer
Hiroshi Nozawa
Ernesto Perea
J. N. Roy
Takayasu Sakurai
Hyungsoon Shin
Jai-Hoon Sim
Vipul Surlekar
Christer Svensson
Jeremy A. Theil
Surya Veeraraghavan
Steven H. Voldman
Roger Woods
Adam S. Wyszynski
Yong Ping Xu
Orly Yadid-Pecht
Choh-Fei Yeap
David C. Yeh

Hu and Ko Receive 2002 SSC Award *continued*

Institute for Microsystems at Hong Kong University of Science and Technology where he served from May 1994 to July 1999. During his tenure there, Ko built up the School of Engineering to 2,000 undergraduates, 600 post-gradates and a faculty of 180 PhDs, in six disciplines. He has been honored with an IBM Faculty Development Award and Semiconductor Research Corporation's Technical Excellence Award. He was chairman of the Hong Kong's Research Grants Council from 1993 to 2000 and received the Justice of Peace award from the Hong Kong Government.

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For more information:

BSIM3 and BSIM4 Official Site
www.device.eecs.berkeley.edu/~bsim3/

The Compact Model Council
www.eigroup.org/cmc/

R&D 100
www.rdmag.com/rd100/100win.htm

ISSCC panel says "yes… maybe" to 100-day hardware

A panel of experts gathered in San Francisco in February to ask, can 100 million transistors in a 100-square-millimeter die be designed in 100 days? And the answer was . . . maybe. The good news is that the notorious productivity gap is being closed by re-use and platform-based design, but only for digital and memory-intensive circuits, as industry is increasingly looking to integrate and re-use analog circuits. The gap exists between the slower growth in design productivity over manufacturing productivity, and analog circuits are proving resistant to design automation and still require — and get — much handcrafting. These were the observations of the panel of EDA and System-On-Chip experts gathered at International Solid-State Circuits Conference.

Moderated by Jan Rabaey from the University of California, Berkeley, the panel concluded on a generally optimistic note — that in the digital domain and with heavy re-use of previously designed circuit blocks, it would be possible to design such chips in close to 100 days. "I think we can end on a positive note," said Rabaey. "If you stick to certain methods you can do the back end. But there are lot of issues at the front end."

The academic community was represented by Asad Abidi, a professor at the UC Los Angeles; Hugo De Man, from Catholic University of Leuven (Belgium); and Alberto Sangiovanni-Vincentelli from the UC Berkeley. The industrial experts were Raul Camposano, Chief Technology Officer of Synopsys Inc. (Mountain View, California); Andrea Cuomo, Vice President of Advanced Systems Technology at STMicroelectronics (Geneva, Switzerland); Mehdi Hatamian, Director of DSP Technology at Broadcom Corp. (Irvine, California); and Harry Veendrick, Philips Research (Eindhoven, Netherlands).

Hatamian gave the answer "yes, maybe," adding, "It depends on how much memory there is, what it's going to do, and does it only have to work once to allow an ISSCC paper to be written." He then stressed that the best chance of success came with the right people. Sangiovanni-Vincentelli argued that ASICs are now going to disappear rapidly in favor of platforms of parameterizable hardware and software such as the Nexperia platform from Philips, aimed at different applications.

Abidi repeatedly stressed the special role of analog and why it could thwart attempts to design complex chips at speed. "So ban the analog and RF to an island in multichip module package," was De Man's response. Sangiovanni-Vincentelli interjected, "If we want to step up to the system level, we must solve the analog problem. We must learn how to re-use it, and then you can spend a long time on it. I believe you can trade off performance versus reusability." However, Abidi pointed out, "The one thing the customer wants is more performance — we seldom find the opportunity for re-use."

It was left to De Man to raise the specter of software. His point was that while larger on-chip memories might make hardware design easier and faster, this implied megabytes of embedded processor code. De Man pointed out there was insufficient software productivity to write the code without throwing hundreds of software engineers at the problem.

"600 Mbytes of software is about 600,000 lines of C++ code," he said, before adding that a software engineer's typical productivity is 20 to 30 lines a day.

So as with the doors of opportunity, as the design productivity gap closes, another gap opens.

Peter Clarke
EETimes

Events of Topical and Regional Interest to Our Members

DCAS-02: High-Performance Analog and Digital ICs 2002 IEEE Dallas CAS/SSC Workshop
25-26 March 2002, Dallas, TX
Deadline: 16 November 2001
ewh.ieee.org/soc/cas/dallas/wks3

MIEL 2002: 23rd International Conference on Microelectronics
12–15 May 2002,
University of Nis, Yugoslavia
Deadline: 30 September 2001
www.europa.elfak.ni.ac.yu/miel
SSCS Cooperative sponsorship

EDM 2002: 3rd Siberian Russian Workshop and Tutorial on Electron Devices and Materials
5–9 July 2002, Novisibirsk State Technical University, Russia
Deadline: 30 March 2002
www.ref.nstu.ru/ieeesb/edm
SSCS Cooperative sponsorship

GaAs IC Symposium in Baltimore 21-24 October

The 2001 IEEE GaAs IC Symposium will be held 21-24 October in Baltimore, Maryland, at the Renaissance Harborplace Hotel. This year's program continues to demonstrate the developments in commercial wireless and optical communications technology. Major areas of focus are: wireless and broadband communications, very high-speed optical communications, highly efficient linear power amplifiers, optoelectronics, and millimeter-wave systems.

The technical sessions will highlight all aspects of technology: device development and fabrication, characterization and modeling, IC design and testing, high-volume manufacturing, reliability, system applications, and a technology roadmap for III-V compound semiconductor ICs.

There will be five panel sessions spread over the three days of the technical sessions covering the topics: CAD software, 40 Gb/s ICs, OEICs, and PAs.

Both a Short Course and a Primer Course will be held on Sunday, 21 October. The Short Course is titled "Optical fiber systems." The course includes an overview of fiber systems, IC design issues including various amplifiers, modulators, drivers, serializers, deserializers (SERDES — multiplexers and demultiplexers) and clock and data recovery (CDR) designs and finally, packaging issues. The Primer Course is a tutorial on compound semiconductor electronics, presented within the topical context of the symposium.

The symposium includes the GaAs IC Technology Exhibition with some 40 exhibitors. The Vendor Product Forum, with a focus on power amplifiers, will highlight the latest commercial products available from industry.

The 2001 IEEE GaAs IC Symposium is sponsored by the IEEE the Electron Devices Society with technical co-sponsorship by the Solid-State Circuits Society, and the Microwave Theory and Techniques Society. For the last 23 years, the IEEE GaAs IC Symposium has been the preeminent international forum on developments in integrated circuits using GaAs, InP, SiGe, GaN, and SiC as well as other compound semiconductor devices. In 2001 the Symposium continues its tradition of presenting the best from around the world in high-frequency microelectronics.

See the Web site for the Advance Program with the schedule of speakers, topics and registration information. *www.gaasic.org/.*

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Custom Integrated Circuits Conference 2001 Retrospective

San Diego, California, a hotbed of telecommunications activities, was the site of this year's Custom Integrated Circuits Conference (CICC), held 6–9 May. The CICC (*http://www.ieee-cicc.org/*) upheld its tradition as a first-class international forum for circuit designers to discuss practical aspects of integrated-circuit design. Conference highlights included: four parallel educational sessions organized in a one-day program with four invited speakers per session, 122 technical paper presentations organized in a three-day program with four parallel sessions each day, three spirited panel discussions (one in the afternoon and two in the evening), and an exhibit hall packed with semiconductor and EDA industry leaders.

Specifically, the analog, wired and wireless sessions, the educational sessions, and the luncheon speaker made this year's attendees rate CICC 2001 as the best ever for technical content and social interactions!

Educational Sessions

The CICC is well known for the high quality of its educational sessions, and this year featured some of the best presentations of the past ten years. The topics in the educational sessions included: Advanced Data Converter Design and Test Techniques, IC Design for Wireless Applications, Circuit Design for Optical Fiber Communications, and Digital Image Processing.

Each of the educational sessions contained four two-hour presentations, giving attendees insight into emergent circuit techniques as well as the opportunity to brush up on established design principles. Two outstanding tutorials were presented, the first by Thomas Lee from Stanford University on "The design of low-phase noise oscillators" and the other by Hans-Martin Rein from Ruhr University on "Basic SiGe bipolar ICs for 40 Gb/s optical-fiber links design and realization."

Keynote Presentation

The keynote address was given by Dr. Alauddin Javed, Chief Technology Officer, Wireless Internet, at Nortel Networks, and was titled: "Global wireless Internet momentum." Dr. Javed's thought-provoking, insightful presentation focused on ubiquitous access to the Internet. He explained why wireless telecommunication and the Internet are the two enabling technologies of the new millenium, projected to service one billion information subscribers in the year 2003. Javed never lost sight of core issues, such as the optical communication technologies that supply the backbone for many advances and the intellectual property competency of the industry.

Luncheon Speaker

One of the most entertaining presentations ever seen in an IEEE conference was given this year by Dr. Michael Workman, Vice President of Storage Subsystems Development at IBM. Titled "Storage technology: trends, enabling and enabled technologies," Dr. Workmen's talk explained how IBM produces rotating disk storage devices with a form factor as small as a bird's egg. Using entertaining music clips and humorous graphics, Dr. Workman described the two decades of technological hurdles that he and his staff encountered en route to a successful disk drive business. Particularly interesting were his observations on how this storage medium is used in our practical world.

Technical Program

Throughout its 23 years, the CICC technical program has always been of great breadth, including issues from semiconductor device fabrication to completely packaged systems. This year was no exception, with sessions on process technology, test and reliability, temporal interfaces, power management, embedded memory, analog design (such as Nyquist-rate data converters and filtering techniques), and wired and wireless communications. Digital signal processing, field-programmable gate arrays, computer-aided modeling (for high-performance digital, analog and RF circuits) and System On A Chip (SOC) were all presented in sessions. This year 258 technical papers were submitted, from which 122 were selected. (Thirteen of the papers were specific topics from invited speakers including, the keynote address.) Several of the significant papers are discussed below.

The hallmark sessions of the CICC are those devoted to analog circuit design principles. This year the analog sessions included classic papers on filters and data converters, as well as innovative papers on analog design in the wired and wireless applications. In one analog session circuit theory involving sub-1-V power-supply levels was discussed by J. Sauerbrey and R. Thewes, in their paper titled "Ultra low voltages switch op amp sigma-delta modulator for portable applications." In another analog session, circuit techniques that allow 7-V stress-free operation with 2.5-V transistors were described by V. Prodanov and V. Boccuzzi in a paper titled "7-V tri-state-capable output buffer implemented in standard 2.5-V CMOS process."

Advances in high-level modeling issues were described by A. Abidi in an invited presentation titled "Behavioral modeling of analog and mixed-signal ICs." Other filter circuits demonstrating extremely linear behavior were discussed by A. Yoshizawa and Y. Tsividis in "An anti-blocker structure MOSFET-C filter for a direct converter receiver." Very well understood in the analog design community are those secondary effects associated with electrostatic discharge devices. Such discussions took place in the invited presentation by C. Duvvury titled "ESD protection device issues for IC designs" and in a circuit-oriented explanation of electrostatic events by H. Feng, K. Gong and A. Wang called "An ESD protection circuit for mixed-signal ICs."

Also found in the analog sessions dedicated to broadband wired transceivers were papers dedicated to highly integrated, cost-effective systems. Two examples of these papers are "A low-power CMOS 155-Mb/s transceiver for SONET/SDH over coax & fibre" by M. Altmann et al. and "An 800-mW, full-rate ADSL-RT analog front-end IC with integrated line driver" by H. Weinberger et al. An excellent invited tutorial by B. Razavi titled "Design of high-speed circuits for optical communication systems" touched upon nearly every circuit topology known to the optical design community.

Frequency synthesizers and voltage-controlled oscillators were documented in one concise session that emphasized modest levels of integration, on-chip inductors, and multi-mode operation for wireless applications. "A –94-dBc/Hz @ 100 kHz, fully-integrated, 5-Ghz, CMOS VCO with 18% tuning range for Bluetooth applications" by C. Samori, S. Levantino, and V. Boccuzzi, and an invited paper by K. Azadet et al. titled "DSP techniques for optical transceivers" were highlighted in the session devoted to digital signal processing.

Another mainstay of the CICC has been its ability to attract the best in computer-aided design and modeling papers. Modeling and other design tools for application-specific problem solving in the area of analog, mixed-signal and RF were all found in sessions of the CICC this year. Many papers concerning fundamental numerical challenges were also documented. Systematic variations within one die appeared as an invited paper by S. Nassif titled "Modeling and analysis of manufacturing variations." Circuit sensitivities resulting from clock frequency variations by K. Bowman and J. Meindel in "Impact of within-die parameter fluctuations on future maximum clock frequency distributions" is another classic example of the practical nature of CICC authors. A paper describing temperature gradients across a single die by A. Ajami, M. Pedram, and K. Banerjee titled "Effects of non-uniform substrate temperature on the clock signal integrity in high-performance designs" and a paper describing inductive effects by H. Hu and S. Sapatnekar titled "Circuit-aware on-chip inductance extraction" are two examples of the excellent work documented by three well-known universities.

Two emergent areas of publication that have recently become a part of the CICC are those involving embedded memory and System On A Chip (SOC). This year in the embedded memory session, everything from novel materials with unusual current-voltage characteristics by H. Toyoshima et al. in "FeRAM device and circuit technologies fully compatible with advanced CMOS" to clever fuse

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SSCS Officer Elections: Sodini Elected President, Lewis Elected Vice President

Charles G. Sodini was elected Society President for 2002-2003 and Steven H. Lewis was elected Society Vice President for 2002-2003 at the 27 August SSCS Administrative Committee Meeting. The President and Vice President are elected at the last AdCom meeting of odd-numbered years. Sodini's and Lewis's terms begin on January 1 and last for two years.

Charles G. Sodini
President
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Sodini has just completed two years as Vice President of the Society (2000-2001). Lewis has been Editor-in-chief of the *Journal of Solid-State Circuits* (1999-2001). Bruce Wooley now assumes the office of SSCS Past President.

Charles G. Sodini received his BS in EE from Purdue University, Lafayette, Indiana, in 1974, and his MS and Ph.D. in EE from the University of California, Berkeley, in 1981 and 1982, respectively. He was a member of the technical staff at Hewlett-Packard Laboratories from 1974 to 1982, where he worked on the design of MOS memory and later on the development of MOS devices with very thin-gate dielectrics. He joined the faculty of the Massachusetts Institute of Technology, Cambridge, in 1983, where he is currently a professor in the Department of Electrical Engineering and Computer Science. His research interests are focused on integrated circuit and system design with emphasis on analog, RF, and memory circuits and systems. With Professor Roger T. Howe, he is a co-author of an undergraduate text on integrated circuits and devices titled Microelectronics: *An Integrated Approach*. Sodini held the Analog Devices Career Development Professorship of the Massachusetts Institute of Technology's Department of Electrical Engineering and Computer Science and was awarded an IBM Faculty Development Award from 1985 to 1987.

An IEEE Fellow, Sodini has served on a variety of IEEE Conference committees, including the International Electron Device Meeting, where he was the 1989 General Chair. He was the Technical Program Co-Chair for the 1992 Symposium on VLSI Circuits and was the 1993-1994 Co-Chair of the Symposium. He served on the Electron Device Society Administrative Committee from 1988 to 1994 and was the 1998-1999 Meetings Committee Chair for the Solid-State Circuits Society.

Stephen H. Lewis received his BS from Rutgers University, New Brunswick, New Jersey, in 1979, his MS from Stanford University, Stanford, California, in 1980, and his Ph.D. from the UC Berkeley, in 1987, all in EE.

From 1980 to 1982 he was with Bell Laboratories, Whippany, New Jersey, where he was involved in circuit design for magnetic recording. In 1988, he rejoined Bell Laboratories, in Reading, Pennsylvania, where he concentrated on the design of analog-to-digital converters. In 1991, he joined the Department of Electrical and Computer Engineering, University of California, Davis, where he is now a professor. His research interests include data conversion, signal processing, and analog circuit design.

Stephen H. Lewis
Vice President
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Lewis, an IEEE Fellow, was an Associate Editor of the *IEEE Journal of Solid-State Circuits* from 1994 to 1997 and was its Editor from 1999-2001. Lewis also was a member of the Program Committee for the International Solid-State Circuits Conference from 1994 to 1998.

Editor's Correction

The article in the July issue announcing IEEE Fellows for 2001 listed incorrectly the citation of Krishna Shenai, University of Illinois, Chicago. Professor Shenai's correct Fellow citation reads:

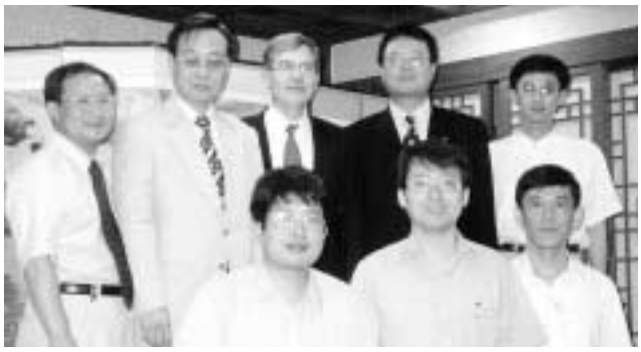
For contributions to the understanding, development and application of power semiconductor devices and circuits.

Seoul Chapter Receives Outstanding Chapter Award

The Seoul, Korea Chapter has been named an Outstanding Chapter of SSCS. This award is given to only one Chapter each year for consistently demonstrating outstanding leadership and initiative in its activities.

The Chapter will be recognized when the award is presented in February at the International Solid-State Circuits Conference (ISSCC).

Jan Van der Spiegel, the SSCS Chapters Coordinator, said of this well-deserved honor, "The Seoul Chapter's receipt of this year's SSCS Outstanding Chapter Award is a recognition of the excellent leadership and organizational qualities they have exhibited during the past 12 months. From sponsoring and co-sponsoring a series of highly successful conferences both at the local and regional level, to introducing a number of new initiatives to encourage and increase membership, Professor Lee and his colleagues have fully deserved the title of 'Outstanding Chapter'. My congratulations go out to them."



Picture taken with Jan Van der Spiegel, University of Pennsylvania after a distinguished lecturer seminar (19 July 2000). Back row from left to right: Kwang Sub Yoon (Secretary, Inha Univ.), Moon Key Lee (Chairman, Yonsei Univ.), J. Van der Spiegel (Distinguished Lecturer, Univ. of Pennsylvania), Chong Woo Park (Vice Chairman, Samsung Electronics), Chanho Lee (Publicity Chair, Soongsil Univ.) Front row from left to right: Jinwook Burm (Publicity Chair, Sogang Univ.), Jinku Kang (Student Activity Chair, Inha Univ.), Gunhee Han (Guest, Yonsei University)

The SSCS Outstanding Chapter Award

is offered annually to an outstanding Chapter, based on the quality and quantity of activities sponsored by the Chapter, benefits for Chapter members, successful outreach programs to the professional community, and growth of Chapter membership. Any member can nominate a Chapter and Chapter Chairs can nominate their own Chapters. Nominations close at the end of June each year. The Award consists of a check for $1,000 to be used for Chapter activities and a Certificate of Recognition for the Chapter.

When asked to name a key management practice of the Seoul Chapter that he would recommend to other Chapters, Moon Key Lee, Chair of the Seoul Chapter, said "It is the work of volunteers that is the basis of chapter activities. In the IEEE Seoul Chapter we have monthly officer's meetings; the agenda varies and sometimes we meet just to socialize and have a delicious dinner. The strong ties built during these regular meetings are a key to our management. It is extremely important to stimulate the academic interests of volunteer leaders, which motivates volunteer service. Hosting Distinguished Lecturer seminars and meeting with these lecturers attracts an interested audience. Having a chance to talk to and mingle with world-prominent scholars is certainly a privilege. Finally, getting financial sponsorships from industries is an essential part of managing a Chapter." The Seoul Chapter, a joint Chapter with the Electron Devices Society, typically invites two or three Distinguished Lecturers each year, alternating from the lists of both Societies.

Moon Key Lee
SSCS Chapter Chair
Seoul, Korea

When Chapter Chair Lee was asked how he finds effective people to help manage Chapter activities, he said, "Fortunately, the Seoul Chapter has many talented and capable SSCS members whom we draw on. The key is to find the people willing to become actively involved. A member who has actively participated in research projects is an excellent choice to work for the Chapter. Then we need to provide funding, responsibility and exact goals for the Chapter activities. We build good relations among our members through our local organizational meetings."

Jinwook Burm, the Chapter publicity officer, was instrumental in nominating the Seoul Chapter for the award. When asked how his participation in the Chapter helps his professional growth, he replied, "Participating in Chapter activities provides me with invaluable opportunities to get to know the people in the research field. I value especially the Distinguished Lecturer seminars and chances to meet lecturers personally, to discuss ideas. It's energizing and self motivating."

To view the activities of the Seoul Chapter, visit its Web site: *sscs-eds.ieee.org.kr*.

Congratulations to the Seoul Chapter on an outstanding year!

Seoul Chapter technical meeting in August featured an SSCS Distinguished Lecture on "Ultra low-power wireless sensors." left to right: Ilgu Yun, Chapter Educational Activities; Hee-Gook Lee, President, LG Elite; Charles Sodini, Distinguished Lecturer; Moon Key Lee, Chapter Chair; Hyun Chang Park, Chapter Awards; Jinwook Burm, Chapter Publicity.

reduction techniques by M. Quellette et al. in "Shared fuse macro for multiple embedded memory devices with redundancy" were presented. Hard-to-find material for content-addressable memories was also documented by T. Chadwick in "An ASIC-embedded content addressable memory with power savings and design for test features." A description of other ICs with large embedded memories was given in "A 99-mm2, 0.7-W, single-chip MPEG-2 422 @ ML video, audio, and system encoder with a 64-Mbit embedded DRAM for portable 422P @ HL encoder system" by S. Kumaki et al. A healthy portion of analog circuitry on the same chip with memory and high-performance digital circuits was given in "The first near zero-IF RX, 2-point modulation TX CMOS SOC Bluetooth solution" by C. Durdodt et al.

With IC technology diffusing into every aspect of human nature, it is not hard to imagine the importance of sensors and their interfaces. The CICC has always tried to document the novel interfaces of the industry and this year's discussion on modular technology deployment was so all-encompassing that it included microscopic silicon microphones (in an invited paper by W. T. Cochran titled "Successful modular process technology for System-On-A-Chip applications"), a skin-like fabric that emulates human skin (by M. Sergio et al. in the paper titled "A system-on-chip for pressure-sensitive fabric"), and a stress-sensitive device and interface worn in a person's mouth to monitor the force on teeth (by W. Claes, W. Sansen, and R. Puers in "A 40-µA/channel compensated 18-channel strain-gauge measurement system for stress monitoring in dental implants"). Other interesting papers in this area discussed magnetic field detectors and gas sensors.

Innovative programmable devices that embed such circuits as CPUs, RAMs, and custom logic constructs on the same chip as the FPGA fabric were showcased at the CICC. Pervasive use of the FPGA in an SOC environment was explained in a presentation by S. Wilton and R. Saleh in "Programmable logic IP cores in SOC design: opportunities and challenges." The ever-increasing demand for on-chip memory in the context of an FPGA was also discussed by S. Oldridge and S. Wilton in "A novel architecture supporting wide shallow memories."

These are just a few of the many excellent papers and presentations documented in the *CICC Digest* and CD ROM. The CICC program committee plans to attract the learned circuit engineer to the conference as an author and attendee so that the integrated-circuit industry can expand its knowledge base, document its intellectual property, and remain the respected profession that we know it to be.

JSSC to have Special Issue on CICC 2001

The *IEEE Journal of Solid State Circuits* will devote its March 2002 issue to the best papers from CICC 2001. In addition, full conference proceedings for CICC 2001 are available from IEEE Single Copy Sales, 1-800-678-4333, catalog number 01CH37169. Visit the CICC Web site at: *http://www.ieee-cicc.org/* for the latest conference details. Better yet, plan on attending CICC 2002 in Orlando, Florida, 12–15 May, 2002!

Philip Diodato
Technical Program Chair

CICC 2001
pwd@agere.com

Chapter Chairs Honored

Two SSCS Chapters honored their past Chairs this summer and fall.

Professor Chorng-Kuang Wang, the 1998-2000 Taipei Chapter Chair, was honored at the annual August meeting of the Chapter in Hsin-Chu County. Jieh-Tsorng Wu, the current Chapter Chair, thanked Professor C.K. Wang for his contributions and presented him with the IEEE pin for past Chapter Chair.

Professor Nikolai N. Voitovich was honored at the closing ceremony of DIPED. DIPED is the West Ukraine Chapter Seminar and Workshop on Direct and Inverse Problems of Electromagnetic and Acoustic Wave Theory held 18-20 September. Dr. Mykhaylo I. Andriychuk, the new Chair of the SSCS West Ukraine Chapter, presented a pin and certificate of appreciation to Professor Voitovich. Professor Voitovich was the organizer and the first Chair of the West Ukraine Chapter. Thanks to his efforts, the Chapter was recognized as the 1999 Outstanding Chapter by the IEEE Components, Packaging, and Manufacturing Technology Society. Voitovich continues to be involved in many of the Chapter's activities.

The Society encourages chapters to honor the volunteers who serve local Chapters. The job of a Chapter Chair includes organizing and publicizing local programs and guest speakers. Other SSCS Chapters interested in honoring past or outgoing Chairs may contact Linda Barankovich at the Society's Executive Office: *Lbaranko@ieee.org*.

Profile of the IEEE SSCS Greece Chapter

Thanos Skodras
Chapter Chair
skodras@cti.gr

The SSCS Greece Chapter has provided a plethora of activities during its first year of operation: seven lectures by engineers from the industry, one workshop, one career event, and one Distinguished Lecture (DL). All of the activities were very useful and well attended. The audience of the lectures was mainly from the University of Patras (faculty and students), while that of the Distinguished Lecture was from nearby companies. The University hosted all the Chapter events, except the Distinguished Lecture, which was hosted by the Patras Science Park, the local incubator of high-tech start-ups. The Chapter is grateful for the cooperation of the University and the Science Park for hosting these events. It is worth pointing out that the Chapter has helped bridge the gap between academia and industry by providing a bi-directional link for the flow of knowledge.

The Distinguished Lecture by Professor Jan Van der Spiegel on "Biologically inspired vision sensors," held on 18 June 2001, was the peak event before summer vacation. It was combined with a presentation of the research work carried out at the Electronics Laboratory and with an excursion to Ancient Olympia, the place where the Olympic games began.

After the Distinguished Lecture of Professor J. Van der Spiegel (left to right): S. Krommyda, C. Androulidakis, Professor A. Skodras (Chapter Chair), Professor J. Van der Spiegel, Professor T. Deliyannis, M. Chantzigeorgaki and, Professor P. Yannoulis.

All Chapter activities are coordinated by Athanassios (Thanos) Skodras, an associate professor at the Electronics Laboratory of the University of Patras, Greece. The Chapter was established three years ago as a Circuits and Systems Society, but was approved one year ago as a joint Chapter with the SSCS. Organizing the Chapter jointly with the interests of the older CAS Chapter has achieved a higher impact. There is also a continuous collaboration with the Signal Processing Chapter, which is chaired by A. Stouraitis, a professor of EE of the University of Patras.

Information and photos from these Chapter activities are available on the Chapter's Web site: *www.upatras.gr/ieee*. For the next academic year the activities will include more subjects; some will be less technical (e.g., project management and report writing), but equally important for engineers.

About the City and the University

Patras is the third largest city in Greece (after Athens and Thessalonica) with a population of about a quarter of a million. It is located 200

km west of Athens on the Peloponnese Peninsula and is the main port to Italy.

The University of Patras, with approximately 14,000 students and 800 faculty members, is internationally recognized as a major center for higher education and has an excellent reputation for high-technology development. Its orientation toward science and technology has encouraged a number of high-tech companies to establish research and development centers in Patras (e.g., INTEL, ATMEL and INTRACOM), proving the need for a successful course of the SSCS Greece Chapter.

West Ukraine Chapter Activities

Mykhaylo I. Andriychuk
Chapter Chair
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The West Ukraine Chapter in Lviv has sponsored two student technical conferences and one technical meeting this year, supporting the leadership of faculty and students at two academic institutions.

Thanks to the efforts of Telecommunication Department Chair Dr. Mykhaylo Klymash and West Ukraine Chapter Vice-Chair Dr. Bogdan Koval, the 59th Student Scientific Conference of Radioengineering Faculty, held in April, was a resounding success. Twenty-three reports were presented in the following scientific areas: mobile communications and networks design, signal processing and medical applications, and electromagnetic wave propagation in electronic devices. Technical and financial support was provided by the West Ukraine Chapter. Awards for the best presentations were given to O. O. Tomochko for "Modeling the system of base stations for BBS-mobile communication of the GSM-900 standard," to S. Zablotskyi for "C++ builder and technology of the database BDE-access," and to V. Romanchuk and O. Doliba for "Microprocessor devices for recording and reproduction of the vocal submissions."

The West Ukraine Chapter also sponsored the 16th Regional Conference of Young Scientists and Specialists. The conference, held in May at Karpenko Physiko-Mechanical Institute (PMI), National Academy of Sciences of Ukraine, Lviv, was organized by The Young Scientists Council of PMI. The West Ukraine Chapter provided the technical and financial support. Seventy-five papers of 106 authors from Ukraine and Poland were included in the Conference Program. Short abstracts of papers were published before the event. Two speakers from PMI were named by the Chapter as Best Young Speakers. They were A. I. Koval for "About estimation of the rate distortion function for generalized Gaussian distribution under mean square error criteria" and V. P. Tsisar for the "Peculiarities of oxide phase formation on the chromic steel surface contacting with oxygen content lead." The best papers were published in a post-conference special issue.

The West Ukraine Chapter's Technical Meeting was held 3 May 2001 and featured the presentation of "The radiation operator in the electromagnetics theory" by Dr. Mykhaylo I. Andriychuk, Institute for Applied Problems of Mechanics and Mathematics, NASU, Lviv, Ukraine. The West Ukraine Chapter added the Solid-State Circuits Society last year to its joint focus of interests in the many related Societies that gave birth to its original organization: Microwave Theory and Techniques, Electron Devices, Antennas and Propagation, and Components, Packaging, and Manufacturing Technology.

Emad Hegazi of UCLA Receives the 2001-2002 SSCS Predoctoral Fellowship

Emad Hegazi, a doctoral candidate at UCLA, has been selected to receive the IEEE Solid-State Circuits Society Predoctoral Fellowship for 2001-2002.

Hegazi (S'94) received both his BS and MS in electrical engineering from Ain Shams University, Cairo, Egypt, in 1995 and 1998 respectively. Since 1998 he has been with UCLA, where he is a candidate for a Ph.D. in integrated circuits and systems. His research area covers fractional-n synthesizer design, high-purity VCO design and optimization methods.

"The Awards Committee had an exceptional field of candidates, and the choice was extremely difficult," reports SSCS Awards Chair, Richard Jaeger. "Mr. Hegazi is to be commended for being selected for this prestigious award." A certificate for the award will be presented to Hegazi at the International Solid-State Circuits Conference (ISSCC) during the Monday morning Plenary session at the San Francisco Marriott on 4 February 2002.

Lewis Acknowledges Support Over Three Years as *Journal* Editor

After three years, I am completing my term as Editor-in-Chief of the *IEEE Journal of Solid-State Circuits*. I am grateful for the efforts of the Associate Editors, Guest Editors, and reviewers who have contributed over this time. Their expertise and tireless dedication sustain the high quality of the *Journal*. I am also grateful for the contributions of Mona Mittra and L. Elizabeth Stewart, the *Journal's* Managing and Associate Editors at IEEE, respectively. Their professionalism, skill, and close attention to detail allows the *Journal* to accurately publish over 2000 pages of technical literature each year. In addition, I am grateful to Anne O'Neill, Executive Director of the Solid-State Circuits Society, who helped in countless ways such as updating web pages and arranging for the printing of conference announcements. I am also grateful to Richard C. Jaeger, Chair of the Publications Committee and previous Editor-in-Chief, and Bruce A. Wooley, Society President, for their helpful advise. Finally, I am grateful to Barbara Allison Hurst, who handled all of the administrative jobs in the Editor's office with dedication, skill, and efficiency.

Beginning with the August issue, the next Editor-in-Chief of the *Journal* is Professor Bernhard E. Boser of the Electrical Engineering and Computer Science Department at the University of California, Berkeley. Professor Boser has been very active in the solid-state circuits community. He recently completed service as an Associate Editor of the *Journal* and did an outstanding job in that capacity. Under his leadership, we can be confident that the Journal will become yet stronger as the flagship publication of our discipline.

Stephen H. Lewis
Outgoing Editor
Journal of Solid-State Circuits
lewis@ece.ucdavis.edu

Boser Welcomes Challenge as New *Journal* Editor

The *Journal of Solid-State Circuits* continues to be regarded as the premier publication documenting the advances of the design of solid-state circuits. Over the last three years Professor Stephen H. Lewis has served as the Editor of the *Journal*, masterly balancing the high quality and rapid submission to publication cycle. The circuits community owes a debt of gratitude to Steve for his tireless efforts.

Following Dr. Lewis is a great honor and challenge for me. Fortunately, I can count on an extremely dedicated and qualified team of Associate Editors. I can also count on the *Journal's* reputation which continues to attract submissions from the most qualified circuit designers.

I believe that a very exciting time lies ahead for circuit design. Moore's Law defies all predictions of slowing-down, putting not only faster processes into our hands, but also raising challenging new opportunities for low-voltage circuits, new boundaries between analog and digital processing, and new means of interaction with the physical world, such as micro-mechanical systems, just to name a few examples. I am looking forward to a continuing stream of manuscripts describing new circuits and how to meet design challenges.

Bernhard E. Boser received the Diploma in Electrical Engineering from the Swiss Federal Institute of Technology in 1984 and an M.S. and Ph.D. from Stanford University in 1985 and 1988. From 1988 he was a Member of Technical Staff in the Adaptive Systems Department at AT&T Bell Laboratories. In 1992 he joined the faculty in the Department of Electrical Engineering and Computer Science at the University of California, Berkeley, where he also serves as a Director of the Berkeley Sensor & Actuator Center. His research is in the area of analog and mixed-signal circuits, with special emphasis on micromechanical sensors and actuators.

Dr. Boser is the recipient of the 1987 IEEE Solid-State Circuits Fellowship Award and a 1992 National Science Foundation Research Initiation Award. From 1997 to 2000 he was an Associate Editor of the *IEEE Journal of Solid-State Circuits*. He served on the program committee of several conferences, including the International Solid-State Circuits Conference from 1991 to 1996, the Transducers Conference in 1998, and the VLSI Symposium since 1999.

Bernhard E. Boser
Incoming Editor
Journal of Solid-State Circuits
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IEEE *Xplore*™: July Upgrades

The first major upgrade since the launch of the IEEE *Xplore*™ Web site in 2000 was implemented last July. The new features include:

Extensive Linking

Users can find hyperlinks within the reference section of select abstracts (published since 1996) to the corresponding source, provided the source is in the IEEE *Xplore* database. Now users can easily navigate between articles and papers to follow an author's research. Links cross society publications and conferences. Access to the referenced document is dependent upon the user's subscription rights. No other publisher has such depth of linking within its own content.

This linking is the same that SSCS members have available within the DVD of the new Solid-State Circuits Digital Archive 2000 (JD3755). The DVD includes all the articles in PDF for all issues of the JSSC since it began publication in 1966, and for the International Solid-State Circuits Conference from its inception in 1955.

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A redesign of the welcome page includes an article counter, contacts, links to product information, news, and *IEEE Spectrum Online*. Better formatting of the information allows easier understanding of access rules. Also, visitors now know the size of the database on a weekly updated basis. These revisions keep users informed of new updates to the site through the section of release notes. The IEEE *Xplore* development team uses member committees and institutional library focus groups to determine important areas for improvement as well as to test new user functions. Watch for continued release announcements with more improvements over the coming months at *www.ieeexplore.org*.

SSCS EVENTS CALENDAR

Also posted on *www.sscs.org/meetings*

SSCS Sponsored Meetings

2001 SSCTC Low Power Circuits Workshop
www.ieee.org/ssctc
11–12 October 2001
Key Bridge Marriott, Arlington, VA

2002 ISSCC International Solid-State Circuits Conference
www.isscc.org
5–7 February 2002
San Francisco Marriott Hotel, San Francisco, CA
Paper deadline: 5 September 2001
Contact: Courtesy Associates, ISSCC@courtesyassoc.com

2002 CICC Custom Integrated Circuits Conference
www.his.com/~cicc
12–15 May 2002
Caribe Royale Resort Suites, Orlando, FL
Paper deadline: 28 November 2001
Contact: Ms. Melissa Widerkehr, cicc@his.com

2002 Symposium on VLSI Circuits
www.vlsisymposium.org
13–15 June 2002
Hilton Hawaiian Village, Honolulu, HI
Deadline for receipt of summaries: 8 January 2002
Contact: Phyllis Mahoney, vlsi01@aol.com
or Business Center for Academic Societies Japan
Contact: Phyllis Mahoney, vlsi01@aol.com
vlsisymp@bcasj.or.jp

Technically Cosponsored Meetings

2001 GaAsIC
www.gaasic.org/
21–24 October 2001
Renaissance Harborplace Hotel, Baltimore, MD

2002 Radio Frequency Integrated Circuits Symposium
www.rfic2002.org/
2-4 June 2002
Seattle, WA
Deadline for Papers in .doc format: 26 November 2001
See website for additional deadlines dates for other formats.

2002 Symposium on VLSI Technology
www.vlsisymposium.org
11–13 June 2002
Hilton Hawaiian Village, Honolulu, HI
Deadline for receipt of summaries: 8 January 2002
Contact: Phyllis Mahoney, vlsi01@aol.com

2002 ACM/IEEE Design Automation Conference
www.dac.com/
10-14 June 2002
New Orleans, LA
Paper Deadline: 7 December 2001
vlsisymp@bcasj.or.jp

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