Call for Papers

IEEE Asian Solid-State Circuits Conference, A-SSCC 2014

Location: 85 Sky Tower Hotel, KaoHsiung, Taiwan

Date: November 10 – November 12, 2014

http://www.a-sscc.org

http://sscs.ieee.org

Sponsored by IEEE SSCS, IEEE Region-10 SSCS Chapters

Conference Theme: Integrated Circuits Enabling Big Data with Ubiquitous Computing

Mobile devices and social networks create exabytes of raw data. Using these data to enhance human cognition, solve problems, and make informed decisions relies on connecting computational resources from distributed embedded systems, mobile devices, and the cloud. Submitting papers on novel circuits for big data and ubiquitous computing is highly encouraged.

The IEEE A-SSCC 2014 (Asian Solid-State Circuits Conference) is an international forum for presenting the most updated and advanced chips and circuit designs in solid-state and semiconductor fields. The conference is supported by the IEEE Solid-State Circuits Society and will be held in Asia. Further details on the conference and paper submission guidelines and templates will be available at A-SSCC official website **http://www.a-sscc.org/** around the beginning of April 2014.

Paper Submission

Prospective authors are invited to submit full-length, four-page manuscripts, including figures, tables, and references, to the official A-SSCC 2014 website. All papers will be handled and reviewed electronically. Papers are solicited in the following categories:

Regular Session

1. **Analog Circuits & Systems:** Amplifiers; comparators; switch capacitor circuits; continuous-time & discrete-time filters; voltage/current references; DC-DC converters; power-control circuits; IF/baseband analog circuits; AGC/VGAs; display driver circuits; non-linear analog circuits.
2. **Data Converters**: Nyquist-rate and oversampling A/D and D/A converters; sub-circuits for data converters including sample-and-hold circuits and calibration circuits.
3. **Digital Circuits & Systems:** Design, fabrication, and test of digital VLSI systems; high-speed low-power digital circuits; power-reduction and management methods for digital VLSI; leakage reduction techniques; clock distribution; I/O circuits; reconfigurable logic-array circuits; supply/substrate noise measurement and cancellation for digital VLSI; variation and fault-tolerant circuits.
4. **SoC & Signal Processing Systems:** Systems-on-chip; microprocessors; network processors; baseband communication processing systems & architectures; low-power signal-processing systems; multimedia processors including video, image, audio, and voice processing systems; cryptographic and security-processing circuits and systems; bio-medical/neural signal processors.
5. **RF:** Receivers/transmitters/transceivers for wireless systems; narrowband RF; ultra-wideband and millimeter-wave circuits; circuits and sub-circuits for RF front-end, LNAs, mixers, power amplifiers, VCOs, frequency synthesizers, RF filters, RF switches, power detectors, and active antennas.
6. **Wireline & Mixed-Signal Circuits:** Receivers/transmitters/transceivers for wireline systems including (but not limited to) LAN, WAN, FDDI, Ethernet, token-ring, fiber channel, SONET, SDH, PON, ATM, ISDN, xDSL, and cable-modem; optical/electrical data links and backplane transceivers; power-line communication; clock generation circuits; PLLs; DLLs; spread-spectrum clock generation.
7. **Emerging Technologies and Applications:** Advanced circuit technologies and techniques; ultra-low-voltage and sub-threshold logic design; molecular-, organic-, and nano-electronics; flexible substrates and printable electronics; 3D-integration and novel packaging technologies; compound-semiconductor, superconductive, and micro-photonic technologies and circuits; energy sources and energy harvesting; ambient-intelligence; emerging applications and circuits; medical/bio-electronics/bio-inspired chip design; RFID; analog and optical processors; non-transistor-based analog and digital circuits and systems; advanced memory technologies; spintronics; quantum storage.
8. **Memory:** Static, dynamic, non-volatile, and read-only memory; magnetic and ferro-electric memory design and architecture; data storage and multi-bit-cell-based memory design; embedded memory architecture; cache-memory systems; multi-port memory; CAM design; nano-crystal, phase-change, and 3D memories; yield-enhancement redundancy and ECC techniques; memory testing and built-in self-test.

Special Session

1. **Industry Program:** This special category accepts only papers based on state-of-the-art products. The paper may cover specifications, applications, state-of-the-art points, chip photos, chip architecture/software, circuits (original or with significant improvement), live demo, characterization results, and packaging/testing results.
2. **Student Design Contest:** A student design contest is held among the accepted papers with system prototypes or measurement results for on-site poster demonstration. Refer to the web for further information.

Papers on low-power and/or low-voltage approaches, signal integrity, noise, test, and manufacturability for all the above categories are welcomed. Measurement results are highly recommended, especially for analog, and RF categories. Design methodologies for SiP, SoC, interconnect and statistical designs are included in the scope of the conference; papers describing only CAD tools and CAD algorithms are not considered. Dual submission to other conferences is not allowed. A special issue of the IEEE Journal of Solid-State Circuits will be prepared for publication of the outstanding papers of this conference.

Important dates		
	June 20, 2014, 20:00 (GMT)	**Paper submission deadline**
	August 18, 2014	**Acceptance notification**
	September 15, 2014	**Deadline for final paper submission**

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