ATTEMPT ON PSEUDO STATIC RAM

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A Self-Refreshing 4K RAM with Sub-mW Standby Power

CAYWOOD (INTEL) AND his coworkers presented a self refreshing DRAM paper in 1979. A 4K bit memory was designed with the SRAM pinout. This is one of the pioneering work for the development of pseudo static RAM. The innovative circuit techniques gave CMOS equivalent power (8 μ A standby

current and 5 mA active current) in an NMOS memory. The die size shown here is 2.9 mm x 5.2 mm. The cell and the architecture gave a full asynchronous refresh capability.

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