



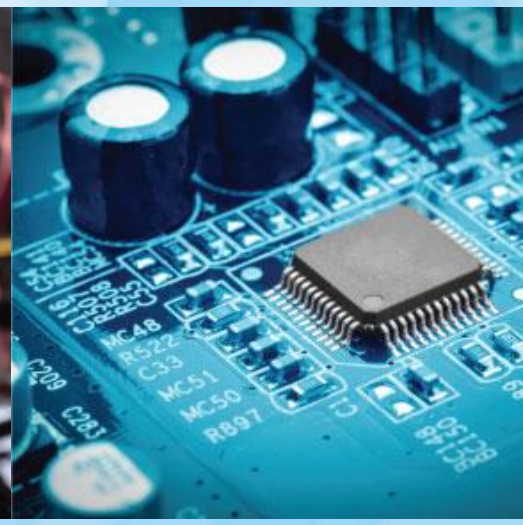

IEEE SOLID-STATE CIRCUITS SOCIETY™
IC Innovation

TC-OSE & SSCS PICO Program

Boris Murmann

September 21, 2022

IEEE Advancing Technology for Humanity

SSCS Technical Committee on Open Source Ecosystem

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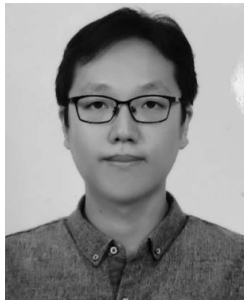
Stanford
USA

Thomas Brandtner
Infineon
Austria

Francisco Brito Filho
Fed. Univ. Semiarido
Brazil

J. Dhurga Devi
Anna Univ.
India



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Hanyang Univ.
Korea

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Apple
USA

Rana Muhammad
FAST National
Univ. Pakistan

Harald Pretl
Kepler Univ., Linz
Austria

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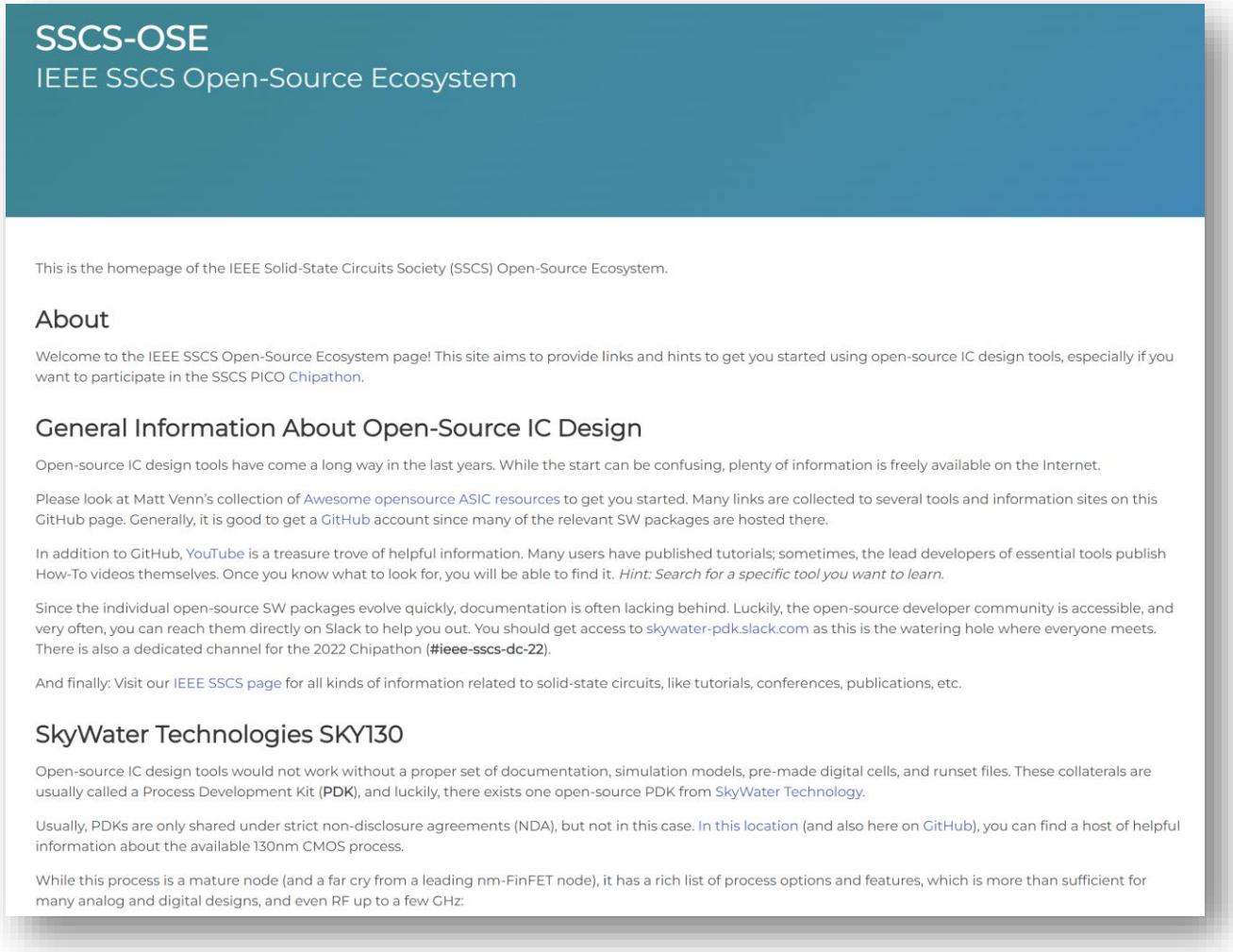
Stanford
USA

Mehdi Saligane
Univ. Michigan
USA

Mirjana Videnovic-Misic
Silicon Austria Labs
Austria

TC OSE Charter

- Organize PICO “Chipathon”
- External engagements
  - E.g., CHIPS Alliance
- **Engagement with SSCS chapters**
- Develop strategy for open-source publication venues
- Contributions to tool infrastructure, links to education materials
  - https://sscs-ose.github.io/



SSCS-OSE

IEEE SSCS Open-Source Ecosystem

This is the homepage of the IEEE Solid-State Circuits Society (SSCS) Open-Source Ecosystem.

About

Welcome to the IEEE SSCS Open-Source Ecosystem page! This site aims to provide links and hints to get you started using open-source IC design tools, especially if you want to participate in the SSCS PICO Chipathon.

General Information About Open-Source IC Design

Open-source IC design tools have come a long way in the last years. While the start can be confusing, plenty of information is freely available on the Internet.

Please look at Matt Venn's collection of Awesome opensource ASIC resources to get you started. Many links are collected to several tools and information sites on this GitHub page. Generally, it is good to get a GitHub account since many of the relevant SW packages are hosted there.

In addition to GitHub, YouTube is a treasure trove of helpful information. Many users have published tutorials; sometimes, the lead developers of essential tools publish How-To videos themselves. Once you know what to look for, you will be able to find it. *Hint: Search for a specific tool you want to learn.*

Since the individual open-source SW packages evolve quickly, documentation is often lacking behind. Luckily, the open-source developer community is accessible, and very often, you can reach them directly on Slack to help you out. You should get access to skywater-pdk.slack.com as this is the watering hole where everyone meets. There is also a dedicated channel for the 2022 Chipathon (**#ieee-sscs-dc-22**).

And finally: Visit our IEEE SSCS page for all kinds of information related to solid-state circuits, like tutorials, conferences, publications, etc.

SkyWater Technologies SKY130

Open-source IC design tools would not work without a proper set of documentation, simulation models, pre-made digital cells, and runset files. These collaterals are usually called a Process Development Kit (**PDK**), and luckily, there exists one open-source PDK from SkyWater Technology.

Usually, PDKs are only shared under strict non-disclosure agreements (NDA), but not in this case. In this location (and also here on GitHub), you can find a host of helpful information about the available 130nm CMOS process.

While this process is a mature node (and a far cry from a leading nm-FinFET node), it has a rich list of process options and features, which is more than sufficient for many analog and digital designs, and even RF up to a few GHz:

Key Event in 2020: First Open-Source PDK

Google Partners with SkyWater and Efabless to Enable Open Source Manufacturing of Custom ASICs

First open source foundry PDK enables full manufacturing chain for open hardware;

Google-sponsored MPW shuttle program now accepting design submissions

BLOOMINGTON, Minn. and SAN JOSE, Calif. – November 12, 2020 – SkyWater Technology, the trusted technology realization partner, and Efabless, a crowdsourcing design platform for custom silicon, today announced design submissions are now being accepted for a series of Google-sponsored open source Multi-Project Wafer (MPW) shuttles that will run at SkyWater. Through a partnership between Google, SkyWater and Efabless, open source designs selected by the program will be fabricated at no cost to the designers. The MPW program is enabled by the first foundry-supported open source process design kit (PDK) for 130 nm mixed-signal CMOS technologies (SKY130 process). The initiative will enable a complete open source manufacturing supply chain for custom application specific integrated circuits (ASICs) and has been discussed in a series of talks produced by the FOSSi (Free and Open Source Silicon) Foundation including presentations by Google and Efabless.

IEEE SOLID-STATE CIRCUITS SOCIETY™
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2022 SSCS "PICO" Open-Source Chipathon

Proposal Deadline: May 1, 2022

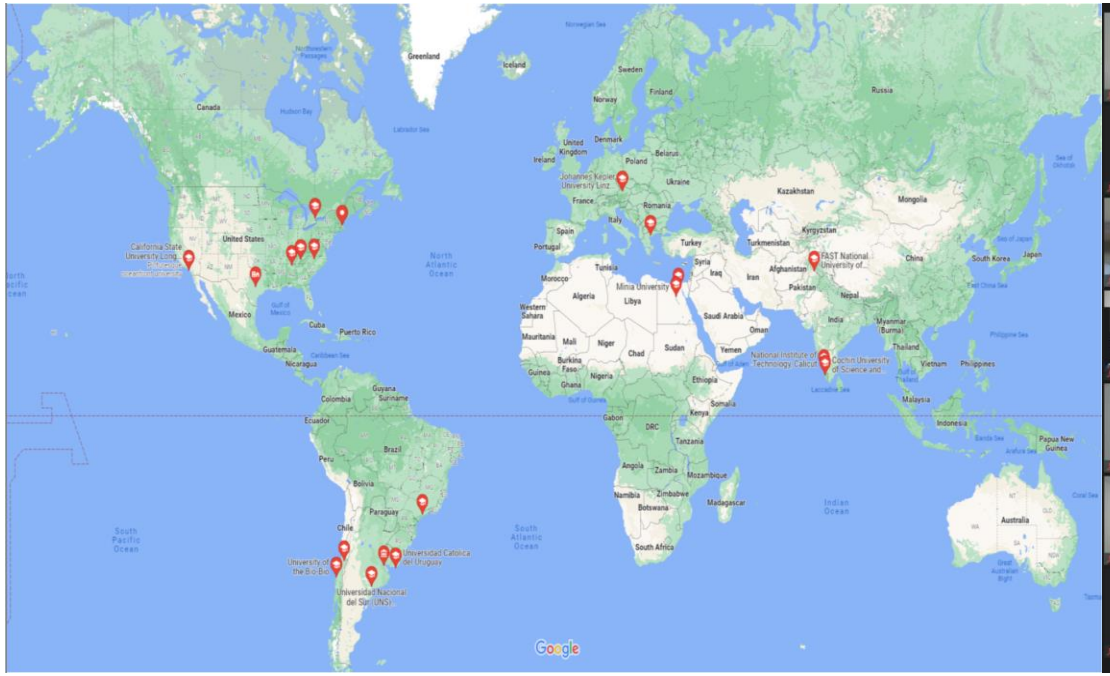
The IEEE Solid-State Circuits Society is pleased to announce its second open-source integrated circuit (IC) design contest under the umbrella of its **PICO** Program (Platform for IC Design Outreach). While this contest is open to any individual or team, we especially encourage the participation of pre-college students, undergraduates, and geographical regions that are underrepresented within the IC design community.

https://sscs.ieee.org/about/solid-state-circuits-directions/sscs-pico-design-contest

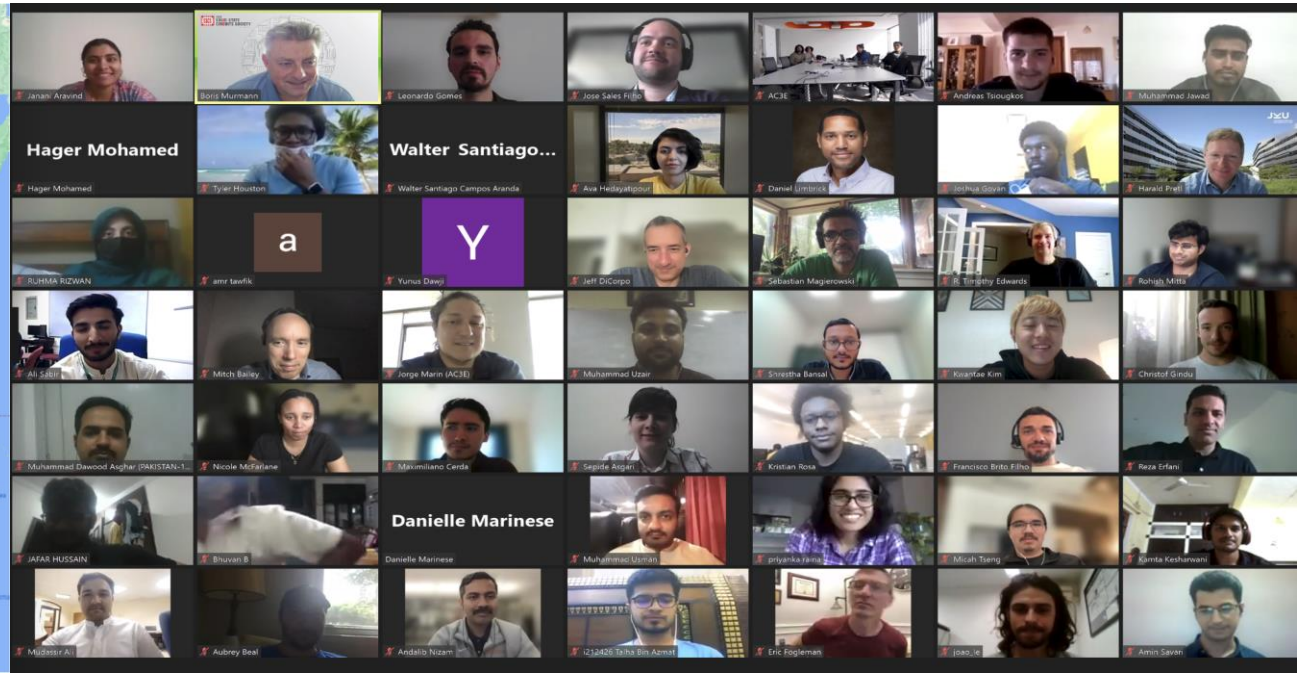
IEEE

Submission Statistics

- 2021: 61 submissions, 18 selected (11 taped out)
- 2022: 54 submissions, 22 selected



Selected teams spread across 10 countries, 5 continents



June 22 kick-off meetup with over 100 attendees

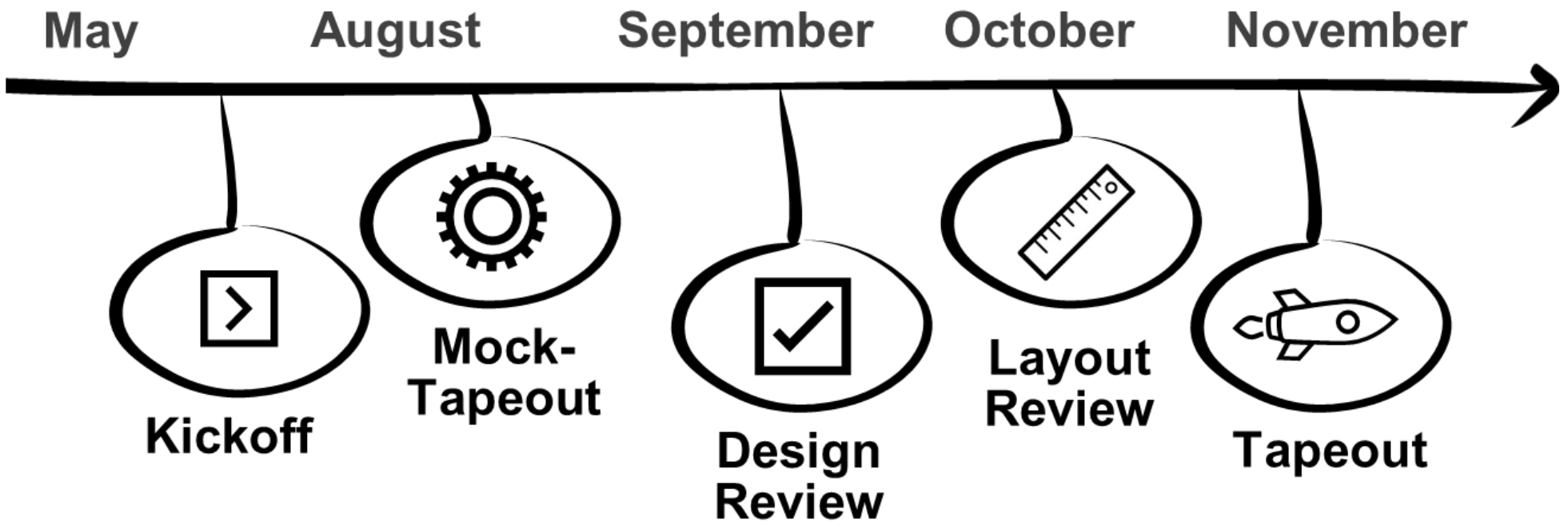
Selected Designs

- Low-power 130nm CMOS 10-bit SAR ADC, URL
- Analog Baseband Circuitry For 60GHz Receivers, URL
- Spatial SD ADC, URL
- Encrypted LSB Steganography with AES Accelerator, URL
- CMOS Bandgap Voltage Reference Design, URL
- On Chip DC-DC Converter with Fast Transient Response, URL
- DC-DC Buck Converter for efficient CubeSat EPS, URL
- CMOS Power Oscillator Test Chip, URL
- Subthreshold SRAM, URL
- Self-Interference Cancellation Low Noise Amplifier, URL
- Matrix Multiplier for AI on Edge Applications, URL

- ReRAM based DNN accelerator, URL
- Mix-Pix - A mixed signal circuit for smart imaging, URL
- 60 GHz demonstrator chip, URL
- A compact batteryless low-startup boost converter, URL
- Sub-Sampling PLL targeting SerDes Applications, URL
- Radiation-Hardened-By-Construction Microcontroller, URL
- Mixed-Signal SoC for Nanopore-Based DNA Sequencing, URL
- Digitally Enhanced PLL, URL
- Novel boost converter for battery-powered IoT uses, URL
- System on Chip for the Next Pandemic, URL
- Electrochemical Water Quality Monitoring, URL

https://sscs.ieee.org/about/solid-state-circuits-directions/sscs-pico-program

Chipathon Timeline



8 or 9 chips (~16-18 designs)

Chipathon Volunteers

- Sribooshan Srinivasan, Anna University (2021 participant)
- Shrestha Bansal, Washington State University (2021 volunteer)
- Tianyu Jia, Peking University (2021 volunteer)
- Kamala Hariharan, Dialog Semiconductor (2021 volunteer)
- Ignatius Bezzam, Rezonent (2021 volunteer)
- Reza Erfani, Case Western (2021 volunteer)
- Kwantae Kim, University of Zurich
- Mitch Bailey, Shuhari Systems, Japan
- Jørgen Kragh Jakobsen, IC Works
- Eric Fogleman, UC San Diego
- Sergio Bampi, Federal Univ. of Rio Grande do Sul
- Fábio Roberto Pereira, Ceitec, Brazil
- Jose Batista de Sales Filho, U Toronto

Looking for Additional Volunteers!

- Possible tasks
  - Evaluate proposals and milestone reports
  - Attend weekly online meet-ups (~June-November)
  - Give a short “how to” presentation during online meetup
  - Provide technical guidance during meet-ups and via Chipathon Slack channel
  - Prepare online tutorials, SSCS webinars
  - Help with open-source tool & utility development
  - **Chapter-level hackathons, invited talks on open source?**
- Minimum time commitment of 1-2 hours per week
- Sign up at https://sscs.ieee.org/volunteer-opportunities#SSCD

Reproducible IC Design?

- It is common to publish with code in other disciplines
  - Now also possible in IC design…

Get OpenLane

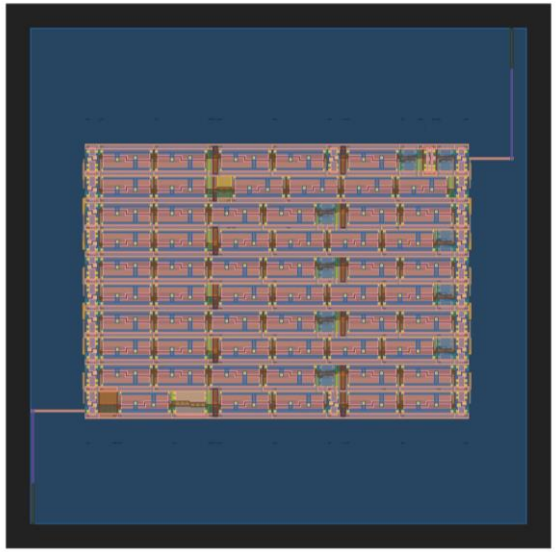
```
$ git clone --depth=1 https://github.com/The-OpenROAD-Project/OpenLane
```

Write verilog

```
%%writefile inverter.v
module inverter(input wire in, output wire out);
    assign out = !in;
endmodule
```

Run OpenLane Flow

```
import os
import pathlib
OPENLANE_ROOT=str(pathlib.Path('OpenLane').resolve())
PATH=os.environ['PATH']
%env PDK_ROOT={CONDA_PREFIX}/share/pdk
%env TCLLIBPATH={CONDA_PREFIX}/lib/tcllib1.20
%env OPENLANE_ROOT={OPENLANE_ROOT}
%env PATH={PATH}:{OPENLANE_ROOT}:{OPENLANE_ROOT}/scripts
%env OPENLANE_LOCAL_INSTALL=1
!flow.tcl -design .
```



https://developers.google.com/silicon/guides/digital-inverter-openlane

ISSCC “Code-a-Chip” Travel Grant Awards

SUBMISSION DEADLINE: NOVEMBER 15, 2022

The ISSCC 2023 Code-a-Chip Travel Grant Award was created to (1) promote reproducible chip design using open-source tools and notebook-driven design flows and (2) enable up-and-coming talents as well as seasoned open source enthusiasts to travel to the Conference and interact with the leading-edge chip design community. This program is made possible by a donation from the CHIPS Alliance, a non-profit organization hosted by The Linux Foundation.

Program rules

- The program is open to anyone (no restrictions). Teaming is encouraged, but each team must identify a leader who can travel to the ISSCC to receive the award. IEEE SSCS membership is encouraged, but not required.
- Applicants must submit an open-source Jupyter notebook detailing an innovative circuit design using open-source tools (examples: inverter, temperature sensor)
- Each submission must contain a suitable open source license (e.g., Apache 2.0).
- A jury will evaluate the submissions and award up to 12 designs within two main categories:
    - Category 1: Silicon-proven designs. The technology used in the original design can be different from the one used in the notebook. The objective is to disseminate the main ideas and design choices using open-source tools and PDKs in a reproducible manner. The temperature sensor example falls into this category.
    - Category 2: A new idea that could be the basis for a future tapeout, with the same objectives regarding open dissemination and reproducibility as in Category 1.